Pulse I-V Characterization of Non-Volatile Memory Technologies

APPLICATION NOTE

KEITHLEY
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Introduction

Until recently, floating gate (FG) NAND flash memory technology has successfully met the growing requirement for non-volatile memory (NVM) for digital cameras, MP3 players and smartphones. However, there is increasing concern in the consumer electronics industry that floating gate NVM may not be able to continue providing higher storage capacities at the ever-lower cost-per-bit requirements that drive the NVM market [1]. The potential for the floating gate approach to "hit the wall" means that research into alternative technologies has become increasingly critical.

This wide-ranging research into an expanding number of materials and technologies requires an electrical test system with wide dynamic range and flexible parameter control. This application note provides a brief history of NVM, an overview of the test parameters required for electrical characterization of NVM materials and devices, and an explanation of the capabilities of the 4225-PMU Ultra-Fast I-V Module with the 4225-RPM Remote Amplifier/Switch, two instrument options designed for use with Keithley's 4200A-SCS Parameter Analyzer. The 4225-PMU/4225-RPM combination has integrated simultaneous measurement of current and voltage on each channel, making investigating transient pulse responses much simpler than with previous hardware. With the system's multi-pulse waveform generation capability, the 4200A-SCS with the 4225-PMU may be used to characterize the memory device's switching mechanism in both the transient and I-V domains. After a discussion of emerging test requirements, this note provides an overview of the NVM projects, tests, and parameters for testing floating gate flash, phase-change cell, ferro-electric cell devices, and resistive memory.

Brief History of NVM

Scientists around the world are investigating NVM alternatives that can replace FG NAND technology, including phase-change memory (PCM/PRAM), charge trap flash (CTF/SONOS), resistive memory (ReRAM), ferro-electric memory (FeRAM), and magnetoresistive memory (MRAM) (**Figure 1**). These device technologies have been studied for years, and each is currently available in the market in some form. Other NVM technologies, including spin-transfer torque (STT) MRAM, floating body (FBRAM), and various types of carbon-nanotube-based memory (CNT RAM), are being actively researched to determine their suitability for memory product applications.

In addition to the traditional uses of NVM in portable consumer electronic devices, the success of FG NVM has created new product categories, such the ubiquitous "thumb" or USB drive and, more recently, the high performance Solid State Disk (SSD) products now being used as replacements for traditional computer hard drives in high performance applications. These products, as well as the possibility of a "universal" memory that would replace both existing flash and dynamic memory (DRAM), have justified ongoing research at universities and semiconductor organizations and companies [2].

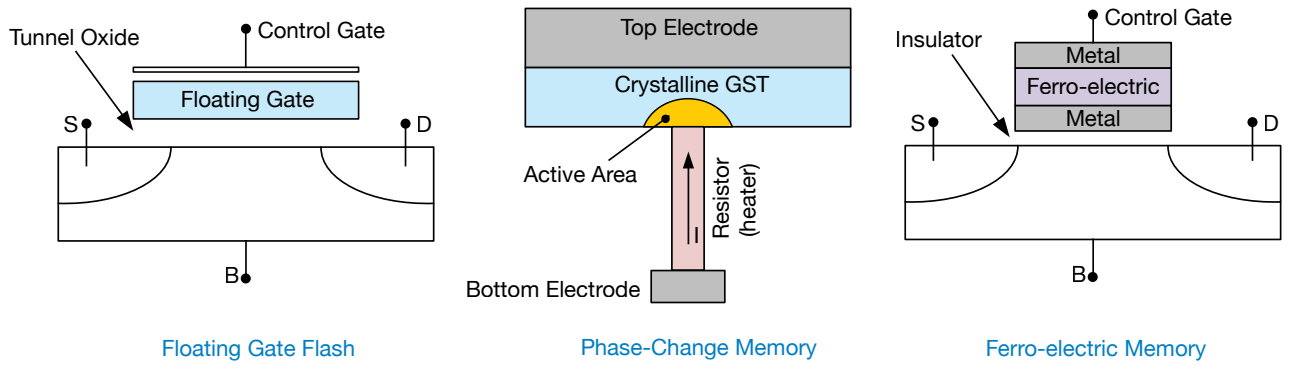

Figure 1. Various non-volatile memory devices.

The ideal memory should have characteristics of both dynamic and non-volatile memory:

- Increasingly low cost and high density based on predictable scalability
- Fast read/write (similar to or faster than existing DRAM speeds)
- High endurance (to address DRAM or SSD applications)
- Long retention
- Low power and voltage requirements
- Compatible with existing logic circuits and semiconductor processes

As the applications for FG NVM devices have increased, so too has the pressure on the FG technology. This has opened up the market to multiple technologies that may replace the FG approach. The future may have multiple NVM technologies addressing the different requirements for each product type or category. In fact, the 2010 International Technology Roadmap for Semiconductors (ITRS) just recommended two additional NVM technologies that should receive accelerated research and development leading to commercial NVM products: Spin Transfer Torque MRAM (STT-MRAM) and Redox RRAM [1].

NVM Test Requirement Evolution and Overview

With floating gate flash memory, electrical characterization was traditionally performed using DC instruments, such as source measure unit (SMU) instruments, after pulse generators had programmed and/or erased the memory cell. This requires some type of switch to apply the DC or pulse signal alternately to the test device. Occasionally, oscilloscopes were used to verify pulse fidelity (pulse width, overshoot, pulse voltage level, rise time, fall time) at the device under test (DUT). Measuring the pulse is important because the flash memory state is quite sensitive to the pulse voltage level. However, the use of oscilloscopes was relatively rare, even in research, because the required setup for oscilloscope measurements differed from that for the pulse-source/DC-measure approach. Even when scopes were used for flash characterization, the complexity of measuring the transient current meant that voltage was the only measurement taken while pulsing.

Recently, standard instrumentation has improved, and now it is possible to measure the current and voltage simultaneously with a single instrument while applying pulses to a memory device or material. Although this capability was possible earlier, it required a rack of instruments and involved making various tradeoffs related to cost, performance, and complexity. In addition, these custom systems were typically created and maintained by an in-house test instrumentation expert who had the wide-ranging skills, experience, and significant time necessary to integrate the various instruments into a system that provided pulse source and measure. These earlier systems were functional, but they were typically one-off creations with limited test envelopes and cumbersome test controls and required time-consuming data extraction. The measurement approach typically used a load or sense resistor with an oscilloscope or digitizer to measure the current. This is a proven technique, but the effect of the load resistor on the voltage delivered to the device has significant downsides for many pulse measurements. Also, correlation across multiple systems and obtaining traceable system-level calibration was effectively impossible.

The new instrumentation provides researchers with additional data to gain a better understanding of NVM material and device behavior in less time. Applying pulses while simultaneously measuring the voltage and current with high-speed sampling provides better insight into the electrical and physical mechanisms that provide the memory behavior. Adding this transient characterization capability to DC characterization provides fundamental data on intrinsic material properties and device response.

Many materials and technologies are currently under investigation for NVM, and each has unique aspects for the physical memory behavior. However, the overall electrical characterization of these various approaches share important test parameters and methods. This commonality means that a single test instrument is useful for characterizing a wide range of memory technologies and device types.

Electrical characterization is crucial to a better understanding of the physical aspects of the underlying technology. Regardless of the particular memory technology under investigation, pulsing is required to exercise the switching behavior. Pulsing with simultaneous measurement provides the data necessary to understand the dynamic behavior of the switching mechanism. Different materials use different

terms. For example, the terms ***program/erase***, ***set/reset***, and ***write/erase*** are used to indicate the fundamental storage of a 1 or 0 bit. These write/erase procedures are done in a pulse mode to provide the overall speed required for typical memory operations and simulate the final product environment. The next section addresses important test parameters that are common to a wide range of non-volatile memory technologies.

Common NVM Test Parameters

Pulse amplitude is the required pulse height used to program and erase the memory cell. Floating gate memory can require 15–20V, or even greater, during the write pulse. Most NVM candidates require 3–5V. The goal for replacement NVM technologies is lower pulse amplitudes, but early research prior to any dimensional scaling or material optimization can require 6–8V. Many technologies require bipolar pulses at these voltage levels, but some recent pulse I-V solutions do not provide these higher voltages when used in a bipolar sourcing mode.

Pulse amplitude fidelity is one of the most important parameters in NVM testing because memory state switching behaviors are non-linear (for example, Fowler-Nordheim current, phase transformation, filament creation/annihilation); therefore, these devices are sensitive to the amplitude of the voltage pulse. Pulse amplitude fidelity parameters are specified in terms of pulse level accuracy, **ringing**, **overshoot**, and **undershoot**. Minimizing the ringing, overshoot, and undershoot is critical to the design of the pulse instrument. Modern pulse I-V systems can provide overshoot and ringing specifications of 3% or less. However, it's important to be aware that pulse shape fidelity at the test device is significantly affected by the connection setup, cables, pulse parameters, device impedance, timing, and impedance mismatches.

In addition to accurate pulse levels, newer technologies require complicated and easily adjustable waveforms, not just a single standard square pulse. For example, testing of ReRAM devices often requires pulse sweep up/sweep down profiles while simultaneously measuring the current. FeRam testing requires the PUND (Positive, Up, Negative, Down) four-pulse sequence. PRAM (phase-change memory) testing requires the ability to do sweeps of virtually any pulse parameter, such as sweeping the fall time of one of the four pulses in the RESET-measure-SET-measure multi-pulse waveform. All of these memory technologies require the ability to output **multi-pulse waveforms** consisting of arbitrary segments, together with multiple measurements within each waveform. Endurance testing requires the ability to output complex arbitrary waveforms quickly without the need for additional setup time or overhead. This requirement further separates the capabilities of newer pulse instrumentation from those of the traditional two-level pulse generator.

Pulse timing parameters, such as ***rise time***, ***fall time***, and ***pulse width*** in test equipment will continue to be very important, especially with the general trend toward faster pulsing, with pulse widths trending from 100ns down to <10ns. For some technologies, such as PRAM, fall time is a critical parameter to define how the RESET operation takes place. This is important because traditional pulse generators typically have limited rise/fall timing ranges and do not permit, for example, a 20ns rise time combined with a 2ms fall time. In general, shorter pulse widths and faster transition times are preferred, but there are practical limitations due to typical interconnect impedances, measurement constraints, and instrumentation tradeoffs.

The need for dynamic, simultaneous **ultra-fast current and voltage measurement** is driven by emerging NVM technologies such as the phase-change and ferro-electric approaches discussed previously. The 4225-PMU/4225-RPM combination provides simultaneous voltage and current measurement, which is important when the dynamic resistance of the material represents the electrical manifestation of the physical mechanism of the bit storage.

The scaling trend leads to smaller and smaller devices. This trend requires measuring smaller currents while pulsing, which calls for some type of a pre-amplifier for the current measurement. To minimize parasitic effects of the cable capacitance and have better control of the amount of energy to the test device, a **remote pulse amplifier**, connected within 15–25cm (6–10 inches) of the DUT, presents a significant benefit. This is especially important for phase change memory (PCM) and ReRAM characterization.

Table 1. Summary of important test parameters for NVM technologies.

NVM Type	Pulse Level	Pulse Transition, Pulse Fidelity	Transient Measurement	Multi-Level Pulses	Multi-Channel Synch
Floating Gate Flash	15–20V+	Minimizing pulse overshoot is critical because of the non-linear nature of the tunneling current used to program or erase the cell.	Emerging need to increase understanding of charge transport.	Required for bipolar pulse waveform for write and erase. Also require high-speed control for solid state relay (high impedance) on source and drain during FN erase.	Emerging need
PRAM (PCRAM)	~±8V	Asymmetric rise and fall required: Fast fall time (≤20ns) for RESET pulse, slow fall time for crystallization (tens to hundreds of nanoseconds).	Critical to understand material and cell behavior.	Unipolar, multi-level pulsing for reset-measure-set-measure waveforms.	Necessary when transitioning to 1T1R[1] device
ReRAM	~±6V	Accurate pulse levels and transition control allow for the study of ion transport or filament formation.	Emerging requirement to help understand material and cell behavior, assist in search for lower-current variants.	Required for both unipolar and bipolar technologies.	Necessary for 1T1R[1] device structure
FeRAM	~±5V	Pulse transition control allows for polarization change characterization.	High speed charge measurements are critical to characterizing capacitive memory effect.	Bipolar pulsing for write and erase (PUND method).	Useful for 1T1C[2] device structure

1. 1T1R = memory cell consisting of one transistor and one resistor, with the transistor providing the control and access to the cell.
2. 1T1C = memory cell consisting of one transistor and one capacitor, with the transistor providing the control and access to the cell.

Current compliance or **current control** is important for testing some NVM technologies, such as ReRAM and PRAM. Usually, this is done using DC instruments and sometimes implemented in custom pulse setups. It is not clear if the current compliance in DC instrumentation is providing sufficiently fast control of the current to meet the typical requirements. For pulsing current control, it is desirable to install the current control device as close as possible to the test device to avoid the possibility of current discharging from the interconnect capacitance into the test device.

To simplify and speed up testing, **switching between pulse and DC instruments** is necessary. To float connections in flash program/erase cycles for endurance testing, switching has to be fast (10–100µs) because the switching must occur between the program and erase pulses to allow for a very large number of stress waveforms. This type of switch should be controlled directly by the pulse generator and located within the pulse instrument for fast control. Typically, this switching is performed by a solid state relay (SSR) for each pulse channel.

Channel synchronization is necessary for NVM testing that requires multiple pulse source and measure channels. Two channels are sufficient for PRAM and ReRAM characterization, to force and measure on both sides of two-terminal devices. For NVM that utilizes transistors as access devices, three or four channels of pulse I-V may be required. In flash memory, two or four channels are needed. Traditional pulse instruments are difficult to synchronize because there are a variety of trigger synchronization methods, each of which has different complexity/trigger performance tradeoffs associated with it. Modern pulse I-V instruments offer internal trigger routing and automatic synchronization in addition to the integrated measurement capability.

As mentioned previously, different NVM technologies have slightly different measurement needs. **Table 1** summarizes the important test parameters for a few memory technologies.

Capabilities of 4225-PMU and 4225-RPM for NVM Characterization

The 4225-PMU Ultra-Fast I-V Module (**Figure 2**) is a single-slot instrument card for the 4200A-SCS. It has two channels of voltage pulse sourcing with integrated, simultaneous real-time current and voltage measure for each channel. There are two types of measurements: sample and spot mean. The sample type is used to capture the time-based current and voltage waveforms critical for understanding transient or dynamic behaviors. The spot mean type provides DC-like current and voltage measurements for I-V characterization. The real-time sampling capability is critical to capture the

transient behavior of NVM materials in a single waveform, because applying repetitive waveforms will cause the memory switching behavior or even damage to the material itself.

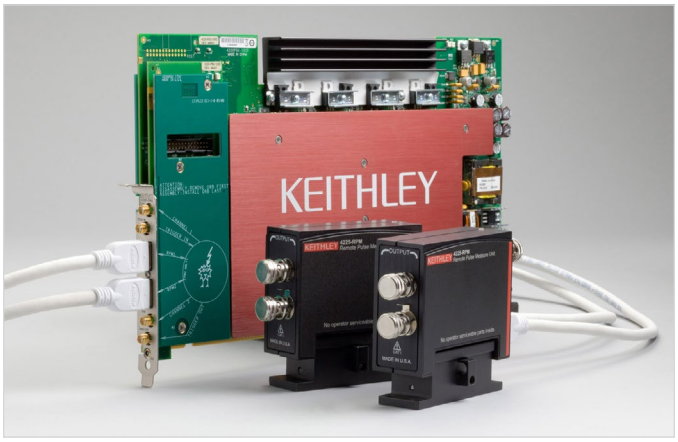

Figure 2. 4225-PMU Ultra-Fast I-V Module and two 4225-RPM Remote Amplifier/Switch Modules.

The 4225-RPM Remote Amplifier/Switch is an optional addition to the 4225-PMU. This small box is located near the DUT and provides the lower-current measurement ranges necessary for characterization of many NVM materials and technologies. In addition, the 4225-RPM provides switching for the 4200A-SCS's source measurement units (SMUs) and CVU signals to allow for high resolution DC measurements and C-V measurements. The 4225-RPM is a single-channel device, so two 4225-RPM modules are required to match the two channels from the 4225-PMU. The 4225-RPM module is designed to be located close to the test device (≤30cm or one foot), minimizing cabling effects to provide improved pulse shape and high speed measurements.

The PMU/RPM combination provides the test capabilities to characterize the existing and emerging NVM technologies described previously. **Figure 3** is a block diagram of the 4225-PMU. Note that both channels have both current and voltage measurement (two A/D converters per channel). Each channel can independently source ±10V or ±40V (into high impedance). **Figure 4** is a block diagram of the 4225-RPM: on the left side, note the inputs from the 4200A-SCS chassis; on the right side, note the output to the DUT. The top half (blue, red, and heavy green lines) is the switching part of the 4225-RPM. Note that the SMU and CVU pathways support four-wire connections throughout. The thinner green lines near the bottom represent the various pulse current measure ranges.

Pulse Level

Each 4225-PMU channel has two source ranges. The 10V source range can output from –10V to +10V (20V amplitude) into high impedance and covers most of the modern NVM candidates. For testing of existing floating gate flash or early non-optimized emerging materials that require higher voltages, the 4225-PMU also has a 40V range, outputting from –40V to +40V (80V amplitude) into high impedance.

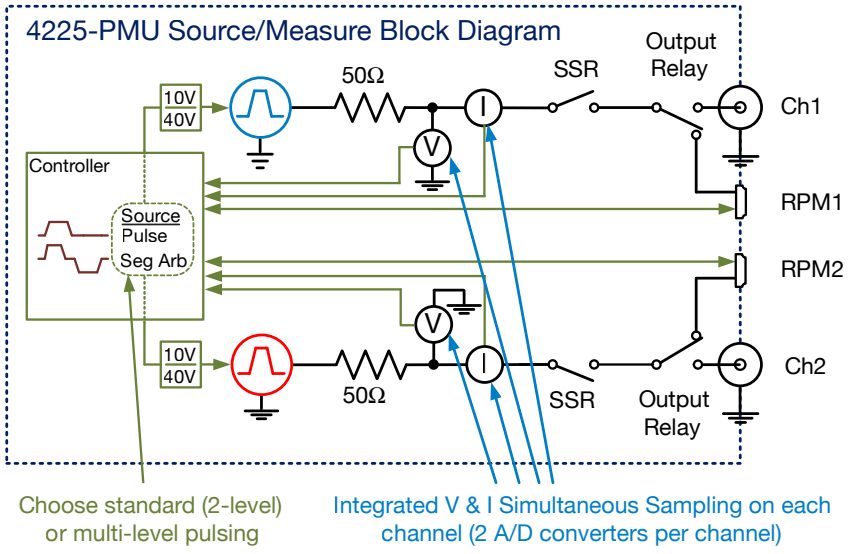

Figure 3. 4225-PMU Block Diagram. It is possible to use the 4225-PMU with two 4225-RPMs by using the RPM1 and RPM2 connections. The SSR shows the solid-state relay, which is useful for high impedance mode when performing program or erase on flash memory devices via Fowler-Nordheim tunneling.

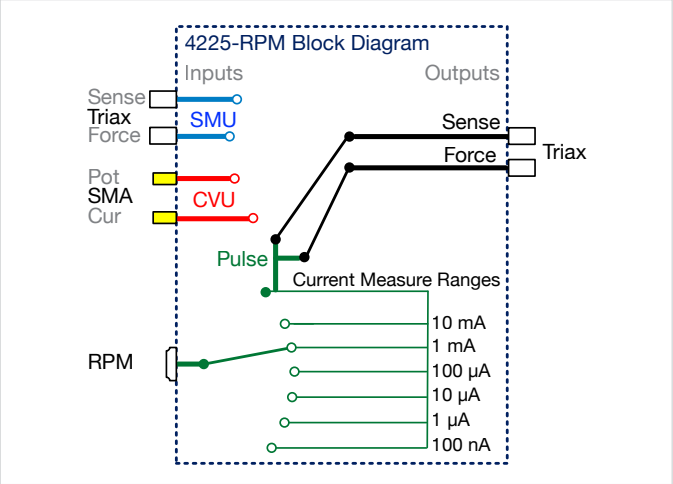

Figure 4. 4225-RPM Block Diagram. The 4225-RPM is both a current pre-amplifier for high speed current measure (in Pulse mode) and a switch for use in choosing between Pulse I-V, SMU, or C-V measurement modes for other instruments in the 4200A-SCS chassis.

Because both source ranges are bipolar, both unipolar and bipolar memory technologies can be characterized.

Transient Measurement and Multi-Channel Synch

The 4225-PMU has two channels, each of which has two A/D converters that sample the voltage and current simultaneously. With the two channels, both the gate and drain of a device may be synchronously pulsed while sampling the voltage and current on both channels to capture the dynamic response of the DUT. If more than two channels of pulse I-V are required, multiple 4225-PMU cards may be installed in a single chassis and all channels will be automatically synchronized to within ±2ns. This simultaneous, synchronous measurement is critical to understanding the switching behaviors of NVM materials and devices.

The 4225-RPM adds measure ranges from 10mA down to 100nA to permit transient analysis of the small currents that are characteristic of the switching states. In addition, the RPM has switching capability to permit routing SMU instrument or C-V signals to the test device.

Pulse Transition and Multi-Level Waveforms

The 4225-PMU has two independent channels, with timing parameters adjustable from 20ns to 40s. The shortest pulse possible is 40ns (FWHM, Full Width at Half Maximum of pulse amplitude), but wider pulses are required to measure smaller currents.

Multi-level or multi-pulse waveforms can be created by linking together linear segments (voltage vs. time) using the Segment ARB® feature. Each channel has a maximum of 2048 segments that may be used in a single sequence or used across multiple sequences. A sequence is a set of segments that allows for looping, typically to provide stresses from a looped sequence interspersed with a measure sequence.

Measurements are controlled on a segment-by-segment basis, so only the required data is collected, maximizing the use of the available sample storage memory, similar to the segmented memory feature available in high-end oscilloscopes. In addition, two measurement types are available: sample and mean. The sample type is used to capture time-based signals, useful for capturing transient behaviors and validating proper connections by evaluating the pulse shape behavior. The mean measurement type is used when measuring I-V characteristics. Both types can be applied to the entire segment, a partial segment, or all segments in the waveform on a channel-by-channel basis.

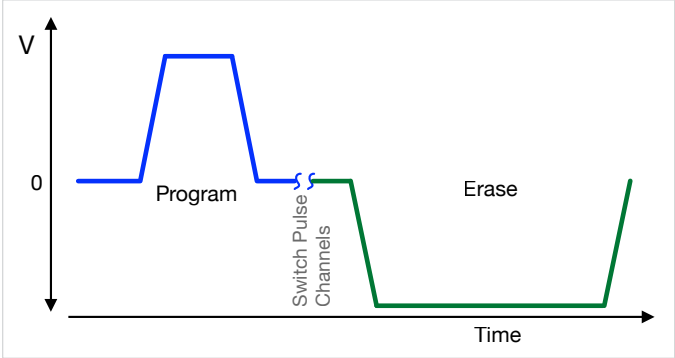

Figure 5. Flash memory Program and Erase waveform: two pulses, three levels. Traditional pulse generators can only output two level pulses, so flash testing required two pulse channels for each test pin and a time-costly switch to apply the second (negative) pulse to the test device. Note that this setup is only for one device terminal. For a typical pulsing on the gate and drain, this setup would have to be duplicated.

The ability to output dozens or hundreds of unique pulses within a single waveform decreases test time over that of traditional pulse instruments, which could only pulse between two pulse levels. Traditional floating gate flash used two pulse channels to create a two-pulse waveform of three voltage levels for a single test device terminal (**Figure 5**). In addition, it required an external switch between the pulse generators and the DUT to route each pulse alternately to the terminal. This external switch added complexity and cost, and most importantly, increased test time. Pulsing the gain and drain

simultaneously required four pulse channels and two sets of switches. **Figure 6** shows a more complicated waveform used for testing phase-change memory. The red boxes on the waveform represent measurements. Note that the entire waveform, consisting of four pulses of varying widths and heights, is output by a single 4225-PMU channel, using 16 segments out of a maximum of 2048.

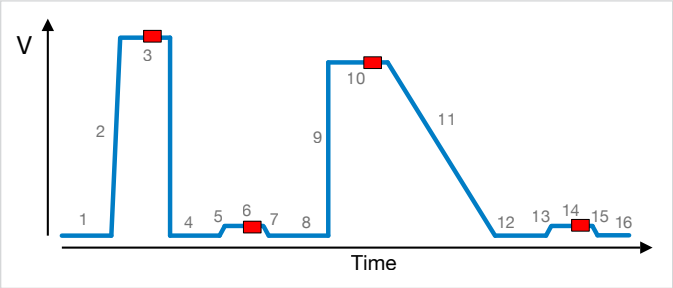

Figure 6. Multi-level pulse waveform consisting of 16 linear voltage segments (gray numbers) and four measurements (red boxes). New pulse source hardware allows creating multi-segment voltage waveforms to provide several pulses within a single waveform, as well as adding integrated V and I sampling (not shown).

Making Connections to the Device

Figure 7 shows the general method for connecting to a two-terminal device using two 4225-RPM Remote Amplifier/ Switches. The 4225-RPM is an optional item for the dual-channel 4225-PMU Ultra-Fast I-V Module and is necessary for NVM characterization. Specific interconnect diagrams are shown for the devices in the example nvm projects discussed later in this application note. Note that the ground connection for NVM devices, which is usually necessary on memory cells that use a transistor as the selection device, should be made to the local shield and the shields for each channel should be connected together (**Figure 8**). These shield connections are important to ensure the relatively high bandwidth required for the fast transitions and narrow pulses required for today's emerging NVM technologies.

It is possible to connect a two-terminal device using a single channel, with the low side of the device connected to the shield, or ground return, of the channel. This is the traditional way to test a simple two-terminal device and is reasonable for DC characterization. However, because of transient effects during the pulse, using two channels on a two-terminal device provides better results. See the "Optimizing Measurements" section for additional information.

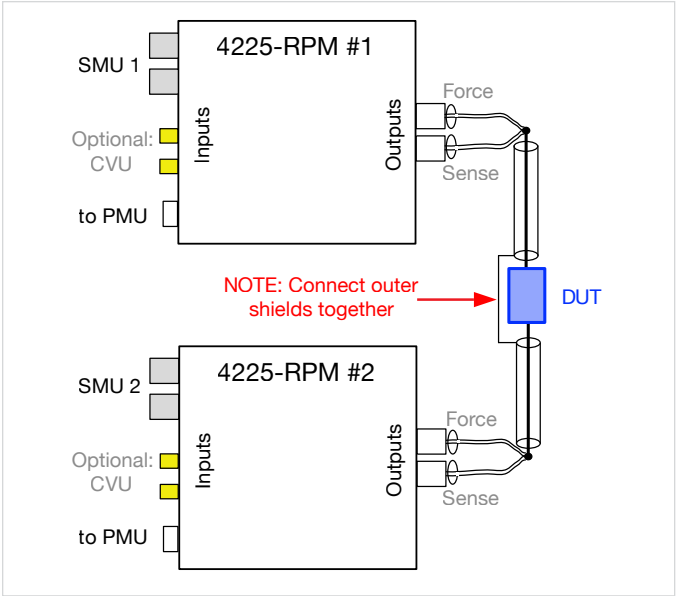

Figure 7. Connection to two-terminal test device.

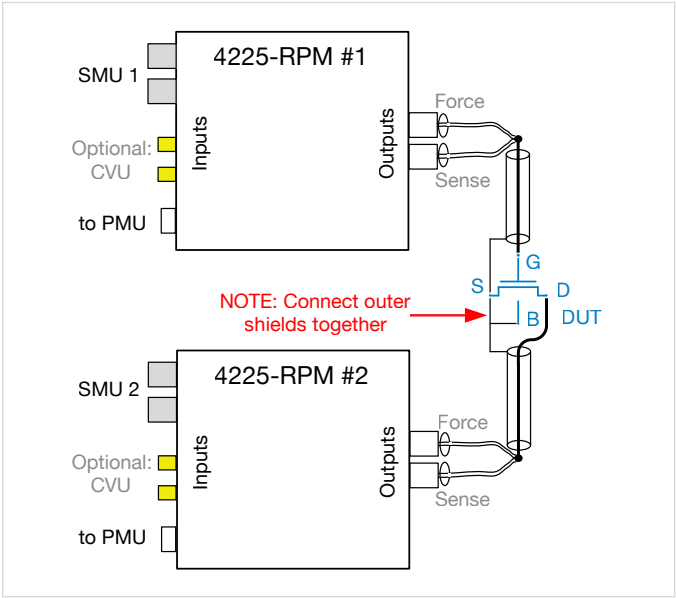

Figure 8. Connection to four-terminal test device with two 4225-RPMs.

Using the Clarius Software to Control the 4225-PMU and 4225-RPM for NVM Testing

A set of example projects for NVM characterization is included with the Clarius software. These four example projects can be found in the Project Library by using the Memory filter. **Figure 9** shows a screen capture of the flash device project, the ***Floating Gate Nonvolatile Memory Characterization Project***. The projects have tests and data for flash, PRAM, FeRAM, and ReRAM devices, and demonstrate the capabilities of the 4200A-SCS and particularly the 4225-PMU with the 4225-RPM. The 4225-PMU/4225-RPM combination provides the fundamental pulse and transient I-V test capabilities to investigate and characterize a wide range of NVM materials and devices. A brief explanation of the user modules follows.

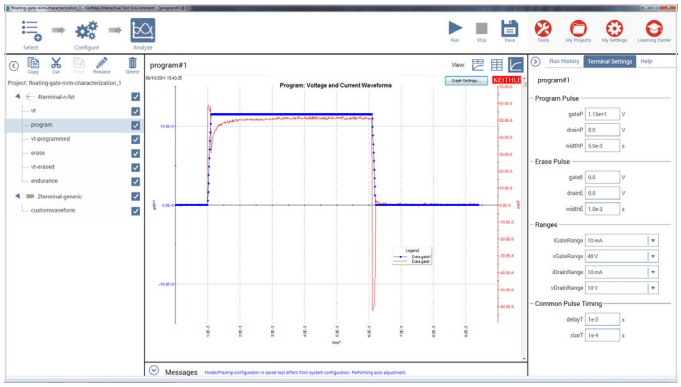

Figure 9. Screen capture of the ***Floating Gate Nonvolatile Memory Characterization Project.***

The tests in the example projects are customized for each memory type but share an underlying approach to minimize the effort required to accommodate additional NVM materials or device types. All of the tests used in the projects are contained in the ***nvm*** user library (**Table 2**). These modules are used in example projects, but they may also be added to another project. If additional capabilities or test types are required, the source code for the modules is included with the 4200A-SCS and may be modified by using the Keithley User Library Tool (KULT) with the optional compiler (order number: 4200-Compiler).

Flash Testing

Flash cells are the dominant type of NVM and because they are implemented on the foundation of MOSFET transistors, they have standard source, gate (actually, control gate or CG), drain, and bulk/substrate connections (**Figure 12**). Fowler-Nordheim current tunneling through gate oxide and hot carrier injection represent the two standard methods for storing and removing charge from the floating gate (**Figure 10**). These methods are degradation mechanisms of standard (non-NVM) MOSFET transistors, which also explains the limited endurance of flash memory. Because the majority of the NVM market is Flash, this is an active area for research and development [3, 4].

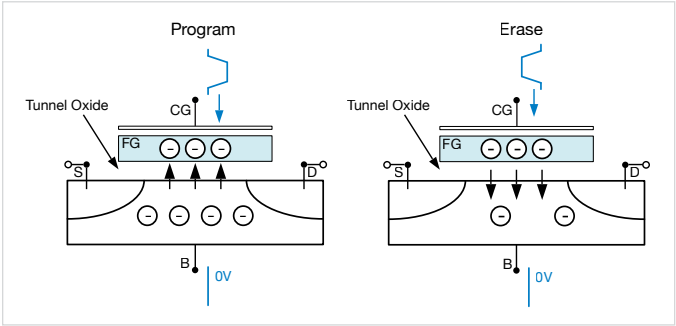

Figure 10. Flash memory structure, showing program and erase conditions for Fowler-Nordheim tunneling.

Initial flash memory characterization usually consists of determining the appropriate values for the voltage pulse height and the pulse width to provide the target threshold values for the program and erase states. Instead of the traditional one-bit (1/0) cell, most modern flash memory utilizes two or three bits per cell, which maps to four or eight unique V_T levels. The increasing number of V_T levels requires more precise pulse level performance and higher pulse voltages.

There are seven tests in the flash device project, ***Floating Gate Nonvolatile Memory Characterization Project*** (**Figure 11**). These tests support a stand-alone NAND or NOR cell. There are three tests that measure the V_T of the flash memory transistor, two that apply program or erase pulses, and one endurance test. The connection to a stand-alone flash memory cell is shown in **Figure 12**. In these tests, only two

Table 2. User modules in the ***nvm*** user library.

User Module	Used in	Description
doubleSweep.c	N/A	Outputs one or two V-shaped waveforms while sampling the voltage and current. Also calculates the accumulated charge. Requires one 4225-PMU with two 4225-RPMs.
doubleSweepSeg.c	PRAM, FeRAM	Similar to ***doublesweep*** but returns the waveform data split into segments used by the PRAM I-V sweep. Also calculates the accumulated charge, used in FeRAM hysteresis test. Requires one 4225-PMU with two 4225-RPMs.
flashEndurance.c	Flash	Performs the pulse stress and DC measure cycling. Applies the maximum number of requested waveforms while measuring every log10 waveform count. The stress waveform is the typical program and erase and the measurement is performed by the SMU instruments. Requires two SMU instruments and one 4225-PMU with two 4225-RPMs.
flashProgramErase.c	Flash	Applies the program and erase pulse waveform while sampling the voltage and current. Can choose to output both program and erase or just one pulse. Requires one 4225-PMU with two 4225-RPMs.
nvmDebug.c		This utility module does not test but saves intra-test status information to a file (C:\nvmlog.txt). This is useful for debugging test issues, especially when modifying existing test modules or writing new ones.
pramEndurance.c	PRAM	Performs the stress and measure cycling for phase-change memory. The test uses the RESET-SET waveform for stresses and every log10 count uses a RESET-measure-SET-measure to obtain the resistance measurements post-RESET and post-SET. Requires one 4225-PMU with two 4225-RPMs.
pramSweep.c	PRAM	This outputs the RESET-measure-SET-measure waveform while sampling the voltage and current. Requires one 4225-PMU with two 4225-RPMs.
pulse_test.c	Flash, PRAM, FeRAM	This is the underlying test routine used by all of the tests. Requires one 4225-PMU with two 4225-RPMs. For additional information, see the read_me.rtf file in C:\s4200\kiuser\usrlibs\nvm.
pundEndurance.c	FeRAM	Performs the stress and measure cycling for FeRAM. The stress waveform is output a maximum number of times and is interrupted on a log10 basis to obtain the PUND and Psw and Qsw extractions.The stress waveform is the PUND waveform and the measure is the two V-pulses controlled by ***doubleSweepSeg***. Requires one 4225-PMU with two 4225-RPMs.
pundTest.c	FeRAM	This test outputs the four-pulse PUND waveform while sampling voltage and current. The routine extracts the P, U, N, and D values from the waveform. Requires a 4225-PMU with two 4225-RPMs.
reramSweep.c	ReRAM	This test outputs 2 pulses, one pulse to be used for “SET” and another for “RESET”. Pulses can be generated by the SMU instrument or by the PMU. SMU instrument sweeps are slow (ms range and higher) and PMU sweeps are fast (ns to ms range). Both voltage sweeps (PMU and SMU instrument) can be used with current limit. Requires one PMU with 2 RPMs and 2 SMU instruments.
reramEndurance.c	ReRAM	Performs the stress and measure cycling for ReRAM memory. The test uses the RESET-SET waveform for stresses and every log10 count uses a RESET-measure-SET-measure waveform to obtain the resistance measurements for the post-RESET and post-SET states. Requires one PMU with 2 RPMs and two SMU instruments.
util.c		This utility module does not test but has support routines for the other tests, such as hardware initialization, calculation of total points, and calculation of maximum allowable sample rate.
vt_ext.c	Flash	Performs a V_G-I_D sweep and extracts the voltage threshold (V_T). Requires two SMU instruments.

pulse I-V channels are used, so both the source and bulk are connected to the 4225-RPM shields. These tests require the following hardware:

- 4200A-SCS
- Two or more SMU instruments, either medium-power 4200-SMUs or high-power 4210-SMUs
- One 4225-PMU with two 4225-RPMs

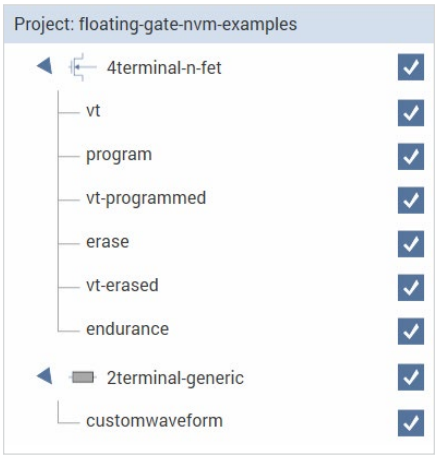

Figure 11. Tests for the flash device in the ***Floating Gate Nonvolatile Memory Characterization Project.***

The three V_T tests are the same and use two SMU instruments to measure the V_T of the flash transistor. The ***program*** and ***erase*** tests apply pulse waveforms to program and erase a stand-alone flash memory cell. Because the 4225-PMU has integrated high speed sampling, the ***program*** and ***erase*** tests also capture the voltage and current waveforms (**Figure 13**). Both of these tests use Fowler-Nordheim tunneling to perform the charge transfer, so the drain voltage = 0V and the graphs show the gate voltage and current only. However, both the gate and drain current and voltages are measured in each test, so they can be displayed if desired.

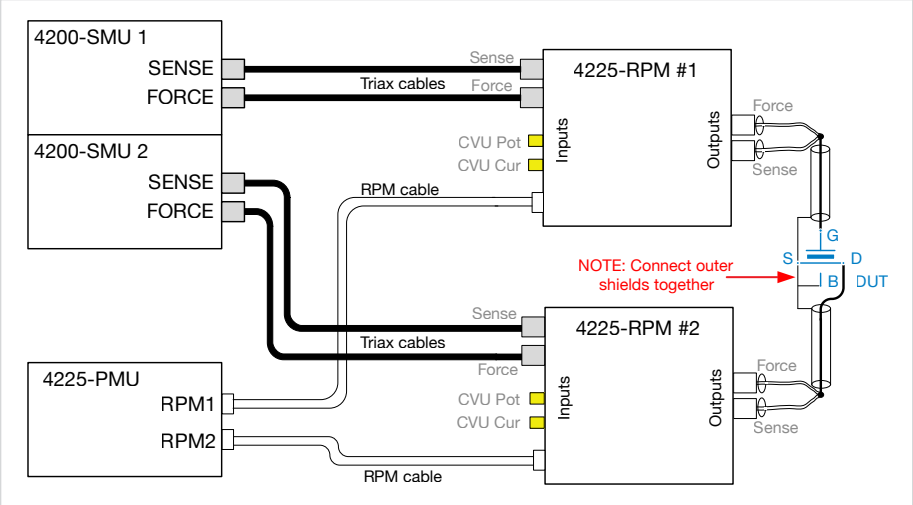

Figure 12. Connection to four-terminal floating gate flash device.

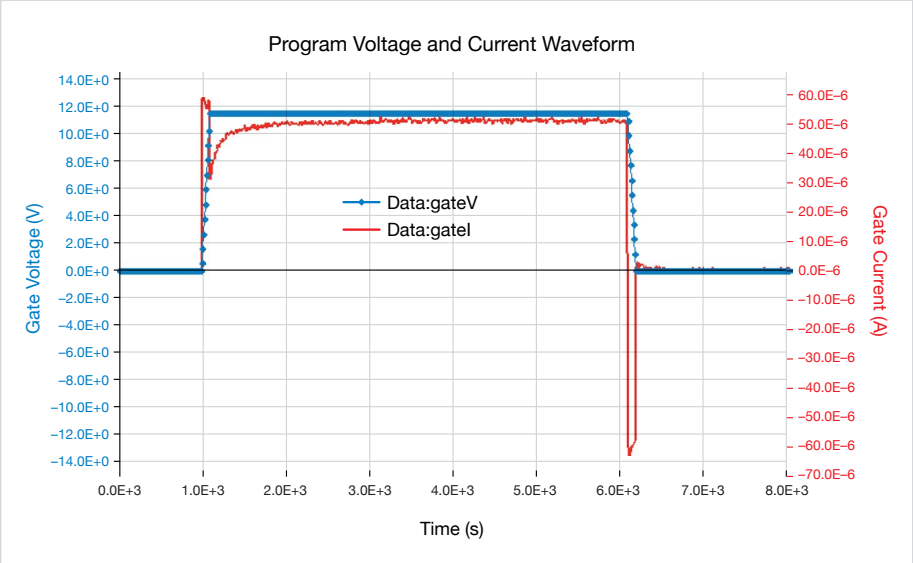

Figure 13. Pulse current and voltage waveforms for a ***Program*** pulse on a NAND cell using a 4225-PMU with 4225-RPMs. Note the capacitive charging and discharging current during the pulse transitions (see "Optimizing Measurements" for an explanation). This graph is from the ***Flash program*** test (user module ***flashProgramErase***).

Measuring the current while pulsing was not previously practical. Because the tunneling current is non-linear with the applied voltage, the measured current provides additional information on how close the voltage is to providing a sufficient electrical field for programming or erasing. The transient current provides information on the dynamic current flow and overall charge transfer. The use of the transient current and voltage information can be correlated to the DC-based V_T results to provide additional understanding of the program and erase processes, which may be unique for different structures, dimensions, and materials. The results of the program and erase pulses are in the ***vt-programmed*** and ***vt-erased*** tests (**Figure 14**).

The last test is ***endurance***, where the program+erase waveform is applied in increasing log intervals and then the program and erase V_T are measured and plotted (**Figure 15**).

Flash Test Modules

There are three modules for testing of either NAND or NOR floating gate devices: ***flashProgramErase***, ***vt_ext***, and ***flashEndurance***. The ***flashProgramErase*** module applies a pulse waveform of either the program pulse, the erase pulse, or both. The ***vt_ext*** module performs a V_G-I_D sweep, using the SMU instruments, and extracts the threshold voltage. The ***flashEndurance*** module applies an increasing number of program+erase waveforms while periodically measuring (on a log interval of the number of waveforms applied) the program and erase voltage thresholds and plotting them.

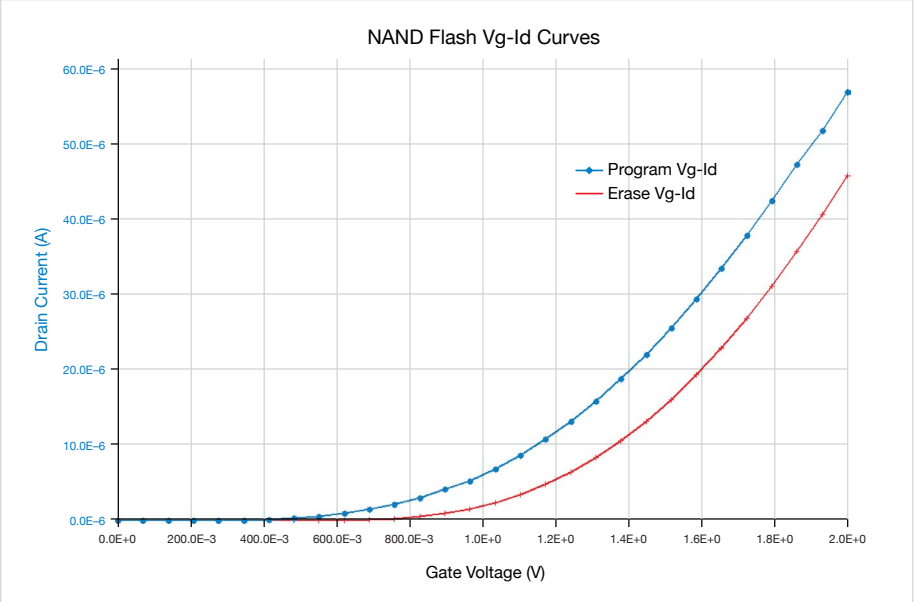

Figure 14. V_T sweeps for a programmed and erased cell taken with SMUs, from the ***vt-erased*** test (user module ***vt_ext***). In this graph, the difference in the V_T after program and after erase is about 180mV.

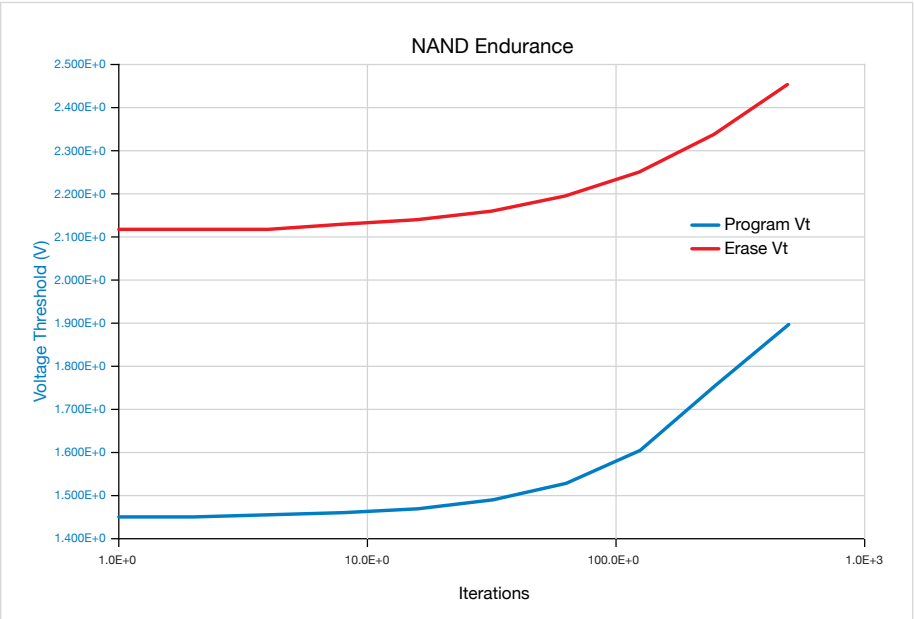

Figure 15. NAND flash endurance results from the ***Flash endurance*** test (user module ***flashEndurance***).

For initial characterization and determination of appropriate pulse parameters for program and erase, the ***flashProgramErase*** and ***vt_ext*** modules allow for adjustments of the pulse parameters, then the measurement of the voltage threshold using the SMU instruments. Note that the 4225-RPM switching capability is used to apply the pulses or the SMU instrument voltages alternately to the device, so no recabling is required.

The ***flashProgramErase*** module uses the 4225-PMU and the 4225-RPMs to output single-pulse or dual-pulse waveforms using the Segment ARB feature of the 4225-PMU. The module supports the two channels of the 4225-PMU, so unique pulse voltages can be output for the gate and drain. This module also measures the waveforms for diagnostic purposes, such as verifying pulse shape performance and proper voltage levels.

Setting Up the Parameters in the *flashProgramErase* Module

Table 3 lists the input parameters for the ***flashProgramErase*** module. This module has the settings for both the gate and drain program and erase pulses. It uses both channels of the 4225-PMU, each connected to a 4225-RPM (**Figure 12**). This module defines and outputs Program and Erase waveforms as shown in **Figure 16**. To measure the voltage threshold after sending the program and/or erase pulses, use the ***vt_ext*** module, described in the next section.

Table 3. Parameters in the ***flashProgramErase*** module.

Parameter	Range	Description
gateP	–40V to +40V	Gate Program Pulse Voltage
drainP	–40V to +40V	Drain Program Voltage
widthP	20ns to 1s	Program Pulse top width
gateE	–40V to +40V	Gate Erase Pulse Voltage
drainE	–40V to +40V	Drain Erase Pulse Voltage
widthE	20ns to 1s	Erase Pulse top width
riseT	20ns to 33ms	Pulse transition time, both rise and fall for Program, Erase
delayT	20ns to 1s	Pulse delay time, before Program pulse and between the Program and Erase pulses
loops	1 to 10^{12}	Number of times to output the ProgramErase waveform

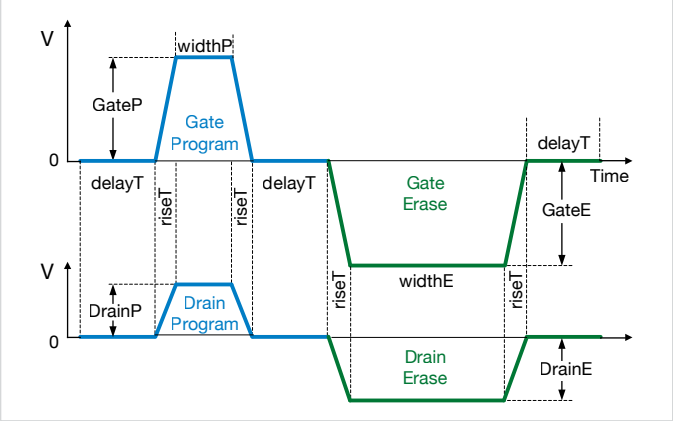

Figure 16. Waveform parameters for the flashProgramErase module.

If only one pulse is desired, set the other pulse levels to 0. For example, if the erase pulse is not desired, set drainE = gateE = 0. This will make the erase portion of the waveform stay at 0V.

For Fowler-Nordheim tunneling, usually the drain voltage is 0V, and just the gate pulse (gateP), is set to either pushing charge into the floating gate (gateP = +V) or clearing the charge from the floating gate (gateE = –V). For the hot carrier injection method, the drain voltage is positive, creating the field in the channel necessary to create the hot carriers.

Setting Up the Parameters in the *vt_ext* Module

Table 4 lists the input parameters for the ***vt_ext*** module. This module performs a V_{GS}-I_D sweep and returns transistor threshold voltage using the maximum gm method, where the threshold voltage is defined as:

$$V_T = V_{G\,MAX} - I_{D\,MAX} / g_{m\,MAX} - 1/2 * V_{DS}$$

$V_{G\,MAX}$ is the maximum gate voltage

$I_{D\,MAX}$ is the maximum drain current

$g_{m\,MAX}$ is the transconductance (g_m) at the maximum g_m.

Table 4. Parameters in the ***vt_ext*** module.

Parameter	Range	Description
DrainSMU	SMU1 to SMUn	SMU instrument for DUT Drain
GateSMU	SMU1 to SMUn	SMU instrument for DUT Gate
SourceSMU	SMU1 to SMUn	SMU instrument for DUT Source, if used
BulkSMU	SMU1 to SMUn	SMU instrument for DUT Bulk, if used
vlow	–40V to +40V	Starting sweep voltage for the Gate SMU instrument
vhigh	–40V to +40V	Final sweep voltage for the Gate SMU instrument
vds	–40V to +40V	Drain bias voltage for the Drain SMU instrument
vbs	–40V to +40V	Pulse delay time, before Program pulse and between the Program and Erase pulses
vgs_pts	10 to 100	Number of points in the Vgs-Id sweep
ids_pts	10 to 100	Number of points in the Vgs-Id sweep
gm_pts	10 to 100	Number of points in the Gm array
vt		Resulting voltage threshold from the max Gm calculation

The number of points in the V_T sweep is set by ***vgs_pts*** and ***ids_pts***, ***gm_pts***. Note that all three parameters must be set to the same value (v***gs_pts = ids_pts = gm_pts***). Typically, a 30-point sweep is sufficient to obtain a reliable V_T.

Note that this module assumes that ***DrainSMU*** is connected to RPM2 and ***GateSMU*** is connected to RPM1. As shown in ***Figure 12***, the test device Source and Bulk connections are to the RPM shield, so the appropriate setting in ***vt_ext*** are SourceSMU = BulkSMU = "".

Setting Up the Parameters in the *flashEndurance* Module

Table 5 lists the input parameters for the ***flashEndurance*** module. This module has the settings for both the gate and drain program and erase pulses and the maximum number of stress loops. It uses both channels of the 4225-PMU, each connected to a 4225-RPM (**Figure 12**). This module outputs a number (***max_loops***) of Program and Erase waveforms (**Figure 16**) to the test device. The module will use log10 stress counts from the ***max_loops*** and the desired number of iterations in ***iteration_size*** to determine how many program+erase pulse waveforms to apply for each stress interval. After each stress interval, the ***vt_ext*** is run, once after the program pulse is applied and once after erase. Note that ***iteration_size***, ***vtE_size***, and ***vtP_size*** must have the same value (***iteration_size*** = ***vtE_size*** = ***vtP_size***).

Table 5. Parameters in the ***flashEndurance*** module.

Parameter	Range	Description
gateP	–40V to +40V	Gate Program Pulse Voltage
drainP	–40V to +40V	Drain Program Voltage
widthP	20ns to 1s	Program Pulse top width
gateE	–40V to +40V	Gate Erase Pulse Voltage
drainE	–40V to +40V	Drain Erase Pulse Voltage
widthE	20ns to 1s	Erase Pulse top width
riseT	20ns to 33ms	Pulse transition time, both rise and fall for Program+Erase pulses
delayT	20ns to 1s	Pulse delay time, before Program pulse and between the Program and Erase pulses
max_loops	1 to 10^{12}	Number of times to output the Program+Erase waveform to stress the test device
vds	–40V to +40V	V_T sweep drain bias voltage for the Drain SMU
vgsstart	–40V to +40V	V_T sweep starting sweep voltage for the Gate SMU
vgsstop	–40V to +40V	V_T sweep final sweep voltage for the Gate SMU
vtP_size	2 to 100	Number of points in the V_{GS}-I_D sweep after the Program pulse
vtE_size	2 to 100	Number of points in the V_{GS}-I_D sweep after the Erase pulse
Iteration_size	2 to 100	Number of times to measure the V_T during the ***max_loops*** stress

PRAM Material Testing

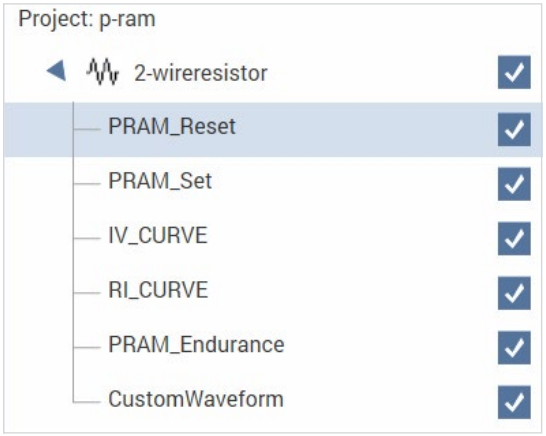

Figure 17. Tests for the PRAM two-terminal device in the ***Phase-Change NVM Project.***

Phase-change memory (PRAM, PCRAM, or PCM) cells are made of a chalcogenide alloy (i.e., with at least one element from the VI group of the periodic table of the elements, plus one element each from the V and IV groups). These same types of materials are also widely used in the active layers of rewritable optical media such as CDs and DVDs. PRAM is one type of resistive memory. Other types of resistive memory include OxRRAM and TMO-RRAM (both are types of Redox RAM) and cation-based, conductive-bridge memory (CBRAM). **Figure 17** shows the tests included for phase-change memory testing in the ***Phase-Change Nonvolatile Memory Characterization Project*** (PRAM).

Through the application of heat in the form of an electrical pulse (or a laser pulse in CDs/DVDs), PCM cells can be switched rapidly from an ordered crystalline phase (which has low resistance) to a disordered, amorphous phase (which has much higher resistance). The switch from the crystalline to the amorphous phase and back is triggered by melting and quick cooling (or a slightly slower process known as re-crystallization). GST [germanium (Ge), antimony (Sb), and tellurium (Te)], with a melting temperature from 500° to 600°C, has emerged as one of the most promising materials for PCM devices (**Figure 18**).

These devices can store binary data because of the differing levels of resistivity of the crystalline and amorphous phases of these alloys. The high resistance amorphous state represents a binary 0; the low resistance crystalline state represents a 1. Multiple resistive levels will permit multi-bit PCM, which has been demonstrated, allowing PCM to scale and provide lower cost-per-bit. [5, 6]. These states are stable over time, which is important for any commercial application [7].

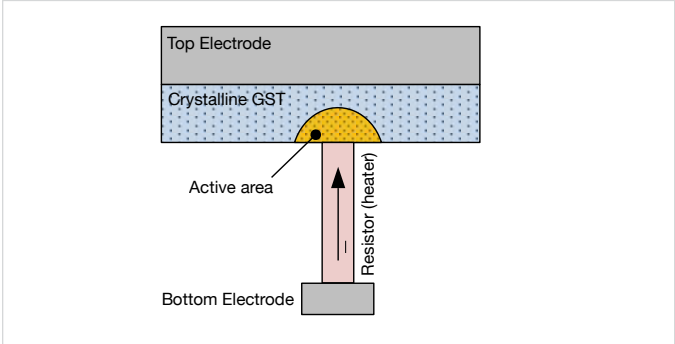

Figure 18. GST [Germanium (Ge), Antimony (Sb), and Tellurium (Te)] structure.

In the amorphous phase, the GST material has short-range atomic order and low free electron density, which means higher resistivity. This is sometimes referred to as the RESET phase because it is usually formed after a RESET operation, in which the temperature of the cell is raised slightly above the melting point, then the material is suddenly quenched to cool it. The cooling rate is critical to the formation of the amorphous state. If the rate is too slow, then the material will be less amorphous. For so-called “slow materials,” the cooling rate is about 30 nanoseconds; for ’”fast materials,” it is in the range of single nanoseconds or faster [8]. The fall time of the pulse can be slower than the required speed; what is important is the fall rate at the top of the pulse, when the cell cools from melting point to crystallization. After reaching crystallization temperature, the crystalline order is frozen. For example, the pulse fall time may be 20ns, but it might take 5ns to go from T_{MELT} to $T_{CRYSTALLIZE}$. In addition, some PRAM structures have a “Select Diode” or “Protection Diode” integrated in series with the PRAM cell. In addition to some drawbacks for the I-V curve, this diode will make the effective fall time shorter. The current flowing through a diode is exponentially dependent on the voltage, so a small decrease in the voltage results in a dramatic reduction in the current flowing through the diode, especially at small currents (~<50µA). Therefore, when testing devices with the series selection diode, the pulse fall time is not as critical for small current test devices and permits testing with standard pulse I-V instrumentation, such as the 4225-PMU and 4225-RPM.

Much like other types of NVM technologies, a PCRAM cell must be formed before it displays the consistent switching necessary to be a memory element. One way to explain the forming process is that it creates the active area of the PCRAM cell. The active area is the portion of the chalcogenide material that transitions between the amorphous and crystalline states. **Figure 18** shows a half-circle shape that represents the active area and is the result of the forming process. The goal of the forming process is reproducible cycling between the SET and RESET states. One challenge to testing a new or unknown cell is to determine the appropriate pulse parameters (amplitude, rise/fall, width) for the RESET and SET pulses. This is usually an iterative process, first starting with a reasonable RESET pulse, then optimizing the SET pulse. The ***pram-reset*** and ***pram-set*** tests are useful for this initial determination of the pulse parameters. Just as with flash memory, it is possible to over-stress the cell and permanently damage it. Because the RESET voltage is the largest, the search for the appropriate RESET voltage must be done with care.

There are tests for phase-change memory devices in the project (**Figure 17**). The ***pram-reset*** test applies a waveform with a RESET pulse and measure R pulse to the PRAM device (**Figure 20**). The ***pram-set*** test is similar to the first test but applies a waveform consisting of a SET pulse followed by a measure pulse. There is an I-V sweep test (iv-curve) that shows the switching effect (**Figure 22**). The ***ri-curve*** test shows the typical R-I curve, which is the resistance of the cell vs. the current (R-I) of the SET pulse (**Figure 24**). The ***pram-endurance*** test is an endurance test, showing the change in the SET resistance vs. the number of RESET-SET waveforms (**Figure 26**).

These tests require the following hardware:

- 4200A-SCS
- One 4225-PMU with two 4225-RPMs

The connection diagram is shown in **Figure 19**. To obtain the best possible measurements, the connection uses the source high, measure low method described in the “Optimizing Measurements” section. No SMUs are used in these tests, although adding SMU tests is possible.

The ***pram-reset*** test applies a two-pulse RESET and measure waveform to the test device and captures the voltage and current waveforms (**Figure 20**). This transient response data is useful to determine the resistance of the device and the degree of reset. This test and the ***pram-set*** test are used to determine the proper voltage and pulse width for reset and set pulses as well as a way to send a reset-only or set-only waveform to the test device. Use these tests to optimize the RESET and SET pulse parameters before performing an endurance test.

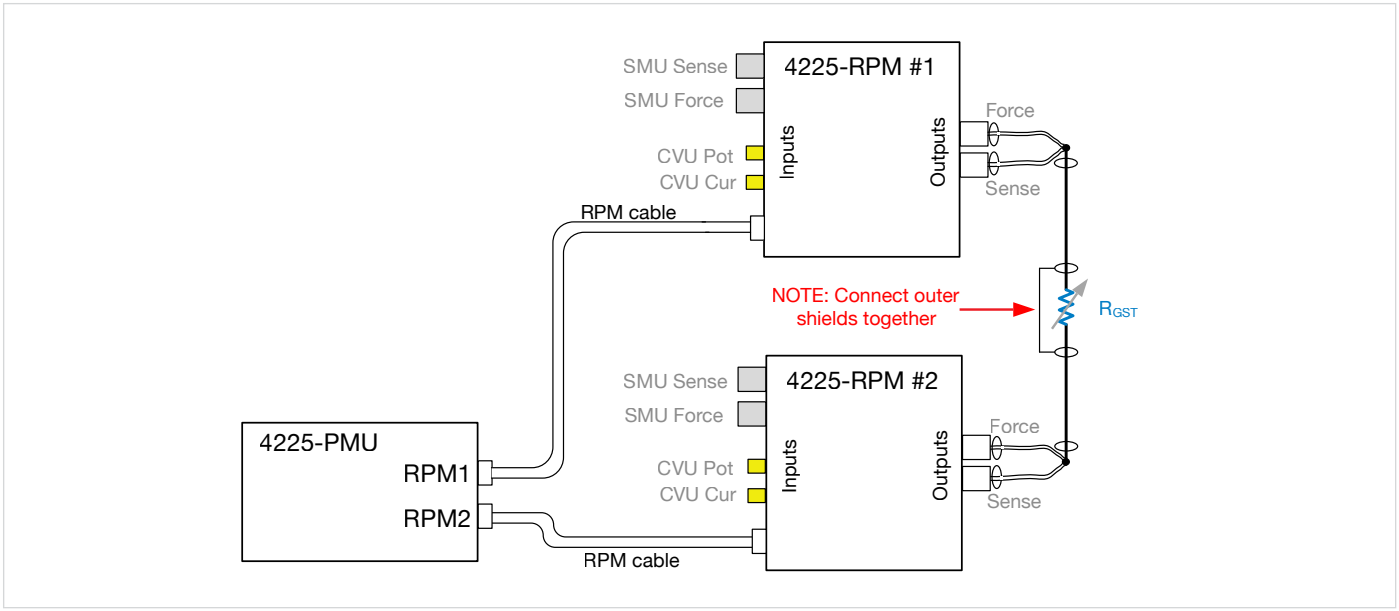

Figure 19. Connection diagram for PRAM tests. Note that the PRAM tests do not use the SMUs or CVU.

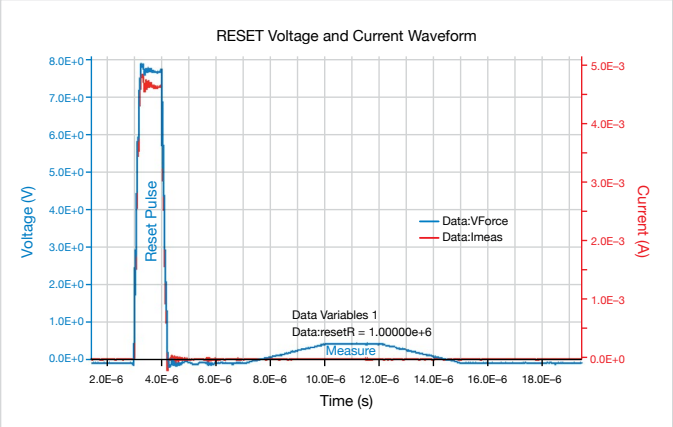

Figure 20. PRAM RESET waveform generated and measured by the 4225-PMU with 4225-RPMs (user module ***pramSweep***).

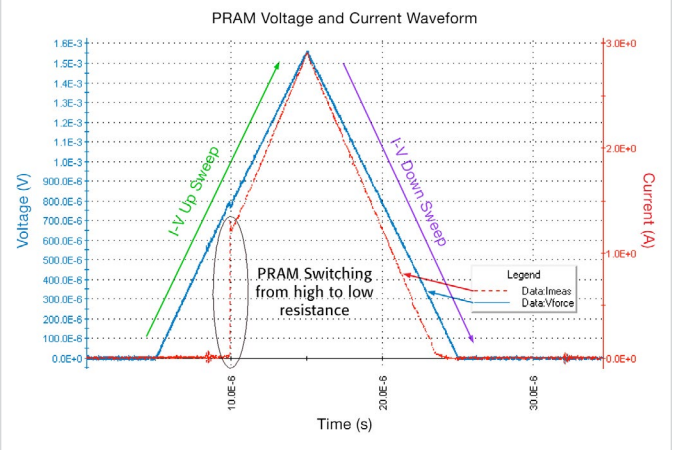

Figure 21. I-V waveform from the ***iv-curve*** test generated and measured by the 4225-PMU with 4225-RPMs (user module ***doubleSweepSeg***).

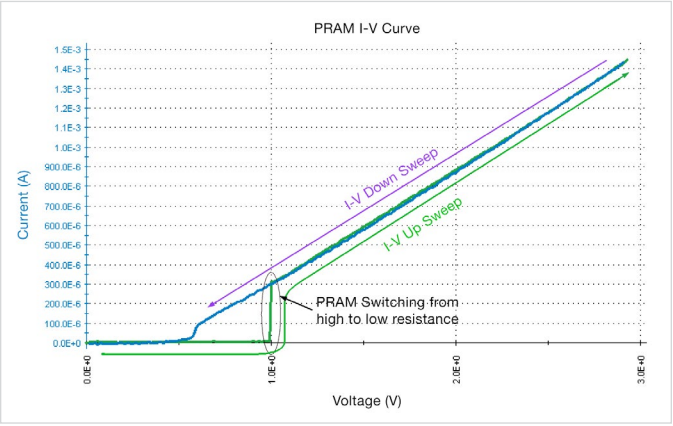

Figure 22. I-V curve from the ***iv-curve*** test generated and measured by the 4225-PMU with 4225-RPMs. This test uses the same data shown in Figure 21, but the curve plots I vs. V (user module ***doubleSweepSeg***).

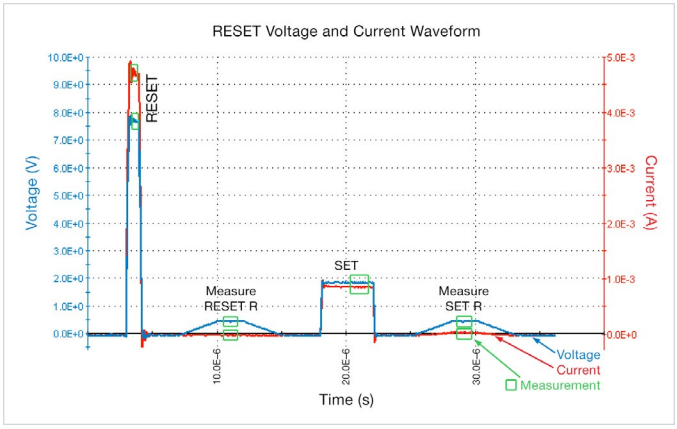

Figure 23. R-I RESET-Measure-SET-Measure waveform generated and measured by the 4225-PMU with 4225-RPMs (user module ***pramSweep***). This graph shows the voltage (blue, left y-axis) and current (red, right y-axis) waveforms. There are four pulses within this waveform. The first pulse is the RESET pulse, which resets the PRAM material, putting it into a high resistance, amorphous state. The second pulse measures the resistance of the RESET state. The third pulse is the SET pulse, which will put the material into a low resistance, crystalline state. The fourth and last pulse measures the resistance of the material in the SET state. Figure 24 is an R-I curve that results from sweeping the SET pulse height and plotting the results in the R-I curve.

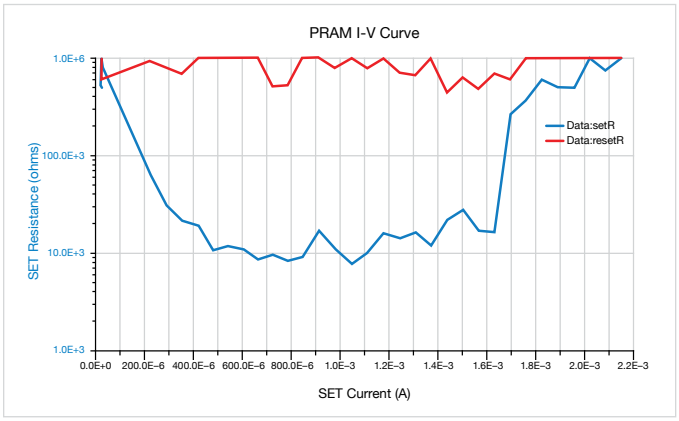

Figure 24. R-I curve shows the resistance variation of the SET state resistance generated and measured by the 4225-PMU with 4225-RPMs (user module ***pramSweep***). This test uses the data captured from the tops of the pulses shown in Figure 23.

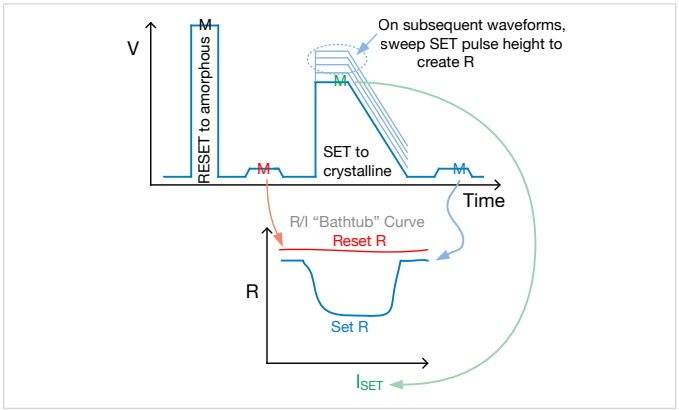

Figure 25. Diagram explains how the various measurements are used to define the R-I curve. The SET curve is swept while the RESET resistance (red M), SET current (green M), and SET resistance (blue M) are measured.

The I-V sweep test uses a single inverted-V-shaped pulse to capture the PRAM switching characteristics. Because this test uses a pulse with V and I sampling, there are two ways to view the data. **Figure 21** shows the waveform data, with I and V plotted vs. time. This is not the typical way to display the characteristics but shows how the test is performed. The second graph (**Figure 22**) shows the typical PRAM I-V curve (current vs. voltage).

The R-I curve is a typical phase-change measurement. The SET pulse voltage is increased while the RESET and SET resistance values are being measured. **Figure 23** shows the four-pulse waveform for one point in the R-I curve. For the curve, spot means are taken (green boxes) to capture the measurements for the R-I curve (**Figure 24**). Note that the RESET resistance is traditionally displayed with the SET resistance, even though the RESET pulse is not changing throughout the sweep, causing the RESET R to be a straight line. Plotting the RESET R does indicate if the RESET pulse is adequately resetting the material after each SET pulse. **Figure 25** shows how the waveform measurements map to the R-I results. Some test systems may use SMU instruments for the resistance measurements, but this requires additional switching and much longer test times. The PMU+RPM combination measures the voltage and current simultaneously at multiple points in the test, providing flexibility while ensuring that the proper measurements are made.

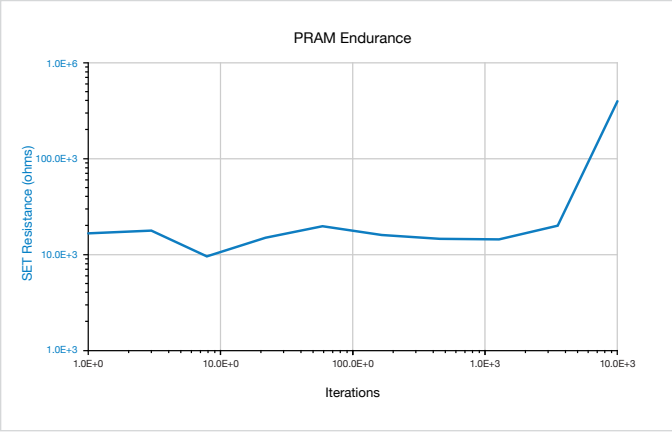

Figure 26. PRAM endurance curve generated and measured by the 4225-PMU with 4225-RPMs (user module ***pramEndurance***).

The PRAM endurance test applies the RESET+SET waveform (**Figure 23**) and measures the SET resistance every log n iterations. **Figure 26** shows an example of an endurance curve. The routine also measures the RESET resistance, so it can also be graphed if desired.

PRAM Test Modules

There are three modules for testing of phase-change materials or devices: ***doubleSweep***, ***pramSweep***, and ***pramEndurance***, using one 4225-PMU and two 4225-RPMs. The ***doubleSweep*** module applies a single V-shaped pulse while sampling the voltage and current.

Setting Up the Parameters in the *doubleSweep* and *doubleSweepSeg* Modules

Table 6 lists the input parameters for the ***doubleSweep*** module, which performs a transient I-V sweep by plotting the I-V samples from one or two V-shaped pulses (**Figure 27**) using one 4225-PMU and two 4225-RPMs. This module is useful for a variety of NVM technologies, whether unipolar (V1 and V2 +V) or bipolar (V1 = +V, V2 = –V). For PRAM, only the first pulse is used, so V2 = 0.

Table 6. Parameters in the ***doubleSweep*** and ***doubleSweepSeg*** modules.

Parameter	Range	Description
riseTime	20ns to 33ms	Transition time for the pulses
V1	–10V to +10V	Voltage amplitude for first pulse
V2	–10V to +10V	Voltage amplitude for second pulse
Irange1	100nA to 10mA	Current measure range for RPM1 (RPM1 forces voltage)
Irange2	100nA to 10mA	Current measure range for RPM2 (RPM2 measures current)

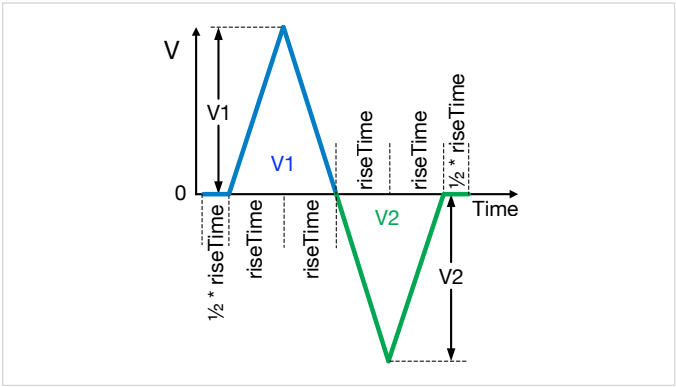

Figure 27. The multi-pulse waveform of ***doubleSweep***.

Two waveforms are returned from this test—the voltage waveform on RPM1 and the current waveform from RPM2. (See connection diagram, **Figure 19**.) Note that the V1 and V2 can be of either polarity. The base voltage for the pulses is

0V. The returned data is the voltage from RPM1 (V_{FORCE}) and the current from RPM2 (I_{MEAS}). The data can be plotted vs. time (**Figure 21**, showing V1 only) or as I-V (**Figure 22**). The difference between ***doubleSweep*** and ***doubleSweepSeg*** is that the ***doubleSweepSeg*** module returns each up and down segment as a separate array, which allows plotting each portion of the curve in a separate color to help distinguish the contributions of each to hysteresis or other relatively complicated I-V results. An example of this routine is shown in **Figure 22**, with the upsweep in green and the downsweep in blue.

For FeRAM, both pulses are used (**Figure 31**). This module is also useful for material characterization for ReRAM, CBRAM, and other conductive bridge or ion transport technologies, many based on transition metal oxide (TMO) materials. This test returns data that can be used to create "butterfly" curves, which is the standard technique for TMO ReRAM characterization.

Setting up the Parameters in the *pramSweep* Module

Table 7 lists the input parameters for the ***pramSweep*** module. This module performs a SET voltage amplitude sweep from ***setStartV*** to ***setStopV***, with the number of steps set by the parameter iteration. The waveform diagram is shown in **Figure 28**. At each step in the sweep, several measurements are extracted (green boxes in **Figure 28**) from the voltage waveform on RPM1 and the current waveform from RPM2: RESET resistance (measurement of cell resistance after the RESET pulse), SET resistance (measurement of cell resistance after the SET pulse), and Set V and Set I (current and voltage at the top of the SET pulse). Measurements are extracted from 30% to 90% of the pulse top (green boxes on **Figure 28**), which avoids the current settling issue and provides a relatively wide window to reduce the noise in the measurements. In addition to the scalar measurements for each sweep (Reset R, Set V, Set I, Set R), this routine also returns one current and voltage waveform from one step of the sweep. The choice of which waveform is captured and returned is set by the value in ***iteration***.

Table 7. Parameters in the ***pramSweep*** module.

Parameter	Range	Description
riseTime	20ns to 10ms	Rise and fall time for the RESET pulse
resetV	–10V to +10V	Voltage for the RESET pulse
resetWidth	20ns to 1s	Pulse top width of the RESET pulse
measV	–10V to +10V	Voltage for the measure V pulse
measWidth	20ns to 1s	Pulse top width for the measure V pulse
Delay	20ns to 1s	Delay time between the pulses and rise/fall time for measure pulses
setWidth	20ns to 1s	Pulse top width for the SET pulse
setFallTime	20ns to 10ms	Fall time for the SET pulse
setStartV	–10V to +10V	Start voltage for the SET pulse amplitude sweep
setStopV	–10V to +10V	Stop voltage for the SET pulse amplitude sweep
Irange1	100 nA to 10 mA	Current measure range for RPM1 (RPM1 forces voltage)
Irange2	100 nA to 10 mA	Current measure range for RPM2 (RPM2 measures current)
iteration	1 to 10,000	Which waveform to capture from the SET sweep
setR_size, resetR_ size, setV_size, setI_size	10 to 10,000	Number of steps in the SET sweep and the size of the measurement arrays. All sizes must be set to the same value.
pts	10 to 10,000	Number of waveform points returned

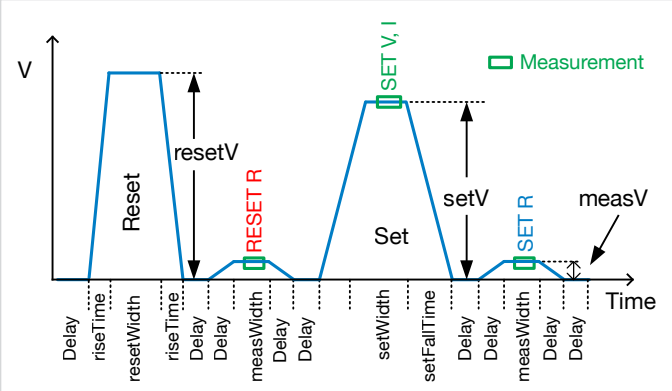

Figure 28. PRAM waveform definition.

To enhance the visibility of the changes in the resistances, values >1MΩ are set equal to 1MΩ. This prevents the occasional current measurements at the noise floor of the range from causing a very large R value (5MΩ to hundreds of mega-ohms). Note that the size parameters (***setR_size***, ***resetR_size***, ***setV_size***, ***setI_size***) for the pulse top measurements must all be the same value (***setR_size*** = ***resetR_size*** = ***setV_size*** = ***setI_size***). Similarly, for the sample waveform arrays, the sizes must be set to the same value (***VForce_size*** = ***IMeas_size*** = ***Time_size***).

Setting Up the Parameters in the *pramEndurance* Module

Table 8 lists the input parameters for the ***pramEndurance*** module. This module stresses the PRAM cell by applying the RESET+SET waveform (**Figure 28**) ***max_loops*** times and measuring the RESET and SET resistances. The number of stress/measure cycles is determined by the value of ***iteration_size***, which occurs in a log10 spacing within ***max_loops***.

Table 8. Parameters in the ***pramEndurance*** module.

Parameter	Range	Description
riseTime	20ns to 10ms	Rise and fall time for the RESET pulse
resetV	–10V to +10V	Voltage height of the RESET pulse
resetWidth	20ns to 1s	Pulse top width of the RESET pulse
measV	–10V to +10V	Voltage for the measure V pulse
measWidth	20ns to 1s	Pulse top width for the measure V pulse
delayT	20ns to 1s	Delay time between the pulses and rise/fall time for measure pulses
setWidth	20ns to 1s	Pulse top width for the SET pulse
setFallTime	20ns to 10ms	Fall time for the SET pulse
setV	–10V to +10V	Voltage height for the SET
Irange1	100nA to 10mA	Current measure range for RPM1 (RPM1 forces voltage)
Irange2	100nA to 10mA	Current measure range for RPM2 (RPM2 measures current)
max_loops	1 to 10^{12}	Maximum number of Reset+Set waveforms applied to the test device
setR_size, resetR_size, setI_size, iteration_size	2 to 10,000	Size of arrays for returned measurements. All sizes must be set to the same value.

FeRAM Material Testing

The ***Ferro-electric Nonvolatile Memory Characterization Project*** has tests for two-terminal ferro-electric materials used in FeRAM (or FRAM) and stand-alone (1C) devices, as shown in **Figure 29**. The connection diagram is shown in **Figure 30**. To obtain the best possible measurements, the connection uses the source high, measure low method described in the "Optimizing Measurements" section.

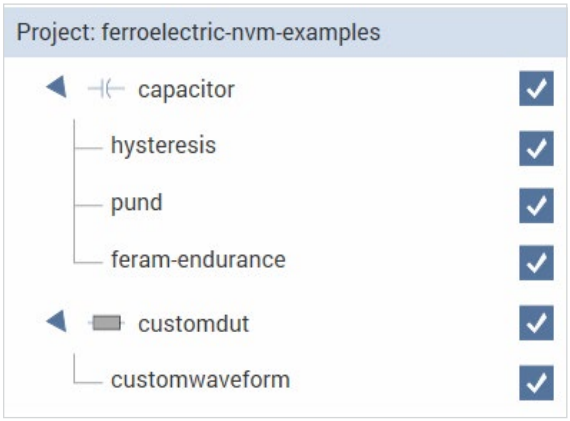

Figure 29. Tests for the FeRAM device

These tests require the following hardware:

- 4200A-SCS
- One 4225-PMU with two 4225-RPMs

FeRAM memory effect relies on charge storage in a capacitor but uses a ferro-electric layer instead of the dielectric layer of a typical capacitor. The memory mechanism for FeRAM is based on polarization shift in ferro-electric materials [9, 10, 11, 12]. Ferro-electric materials have strong non-linear dependency between applied electrical field (E) and polarization (P). When the electric field reaches a critical level, the ions inside the crystalline structure move from one stable location to another one. This shift is accompanied by a shift of the ferro-electric domain walls. Electrically, it is represented by the hysteresis chart (**Figure 32**), showing the dependency between electrical field and polarization. The switch between one state and another is characterized by the area of hysteresis, which represents the amount of charge moved during re-polarization.

The challenge of characterizing the ferro-electric capacitor is that the fundamental behavior is switching of the polarization state of the ferro-electric material, which requires measuring the polarization charge on the capacitor as it changes. Typically, a load capacitor, pulse generator, and oscilloscope are used, usually in a Sawyer-Tower circuit. In this approach, measuring the transient voltage, using an oscilloscope or sampler, across the load capacitor is a proxy for the charge flowing into the FE material. However, this method has several drawbacks.

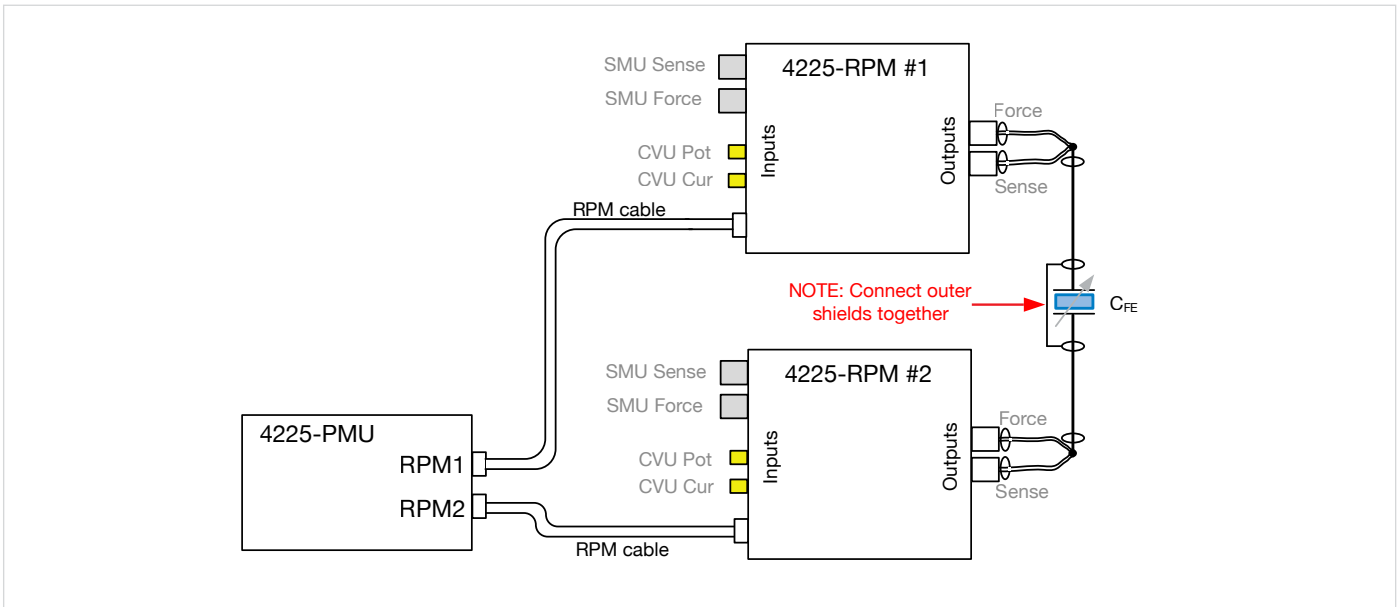

Figure 30. Connection for FeRAM tests. Note that the FeRAM tests do not use the SMUs or CVU.

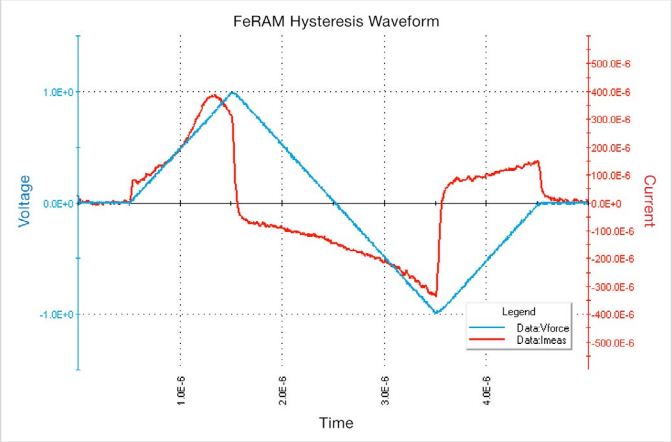

Figure 31. Hysteresis waveform generated and measured by the 4225-PMU with 4225-RPMs (user module ***doubleSweepSeg***). This graph shows the voltage waveform (blue) applied to the FE capacitor. The red curve shows the current flow. Figure 32 shows the typical hysteresis charge vs. voltage curve.

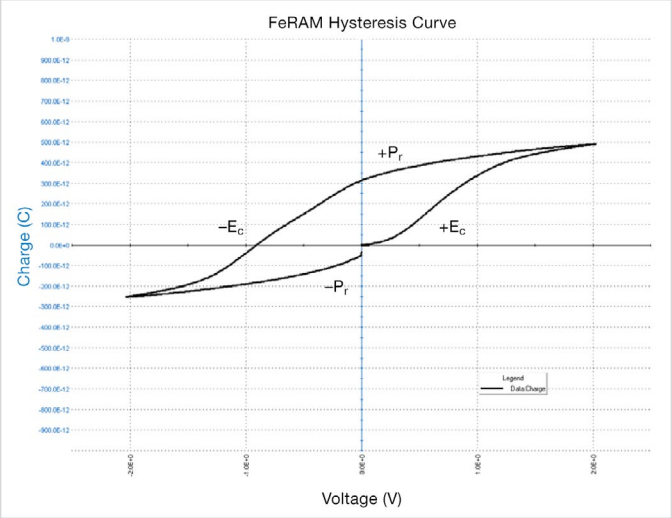

Figure 32. Hysteresis curve generated and measured by the 4225-PMU with 4225-RPMs (user module ***doubleSweepSeg***). This graph shows the variation in the polarity charge as the voltage across the material varies. E_c is the coercive field and Pr is the remnant polarization, which are key parameters for FeRAM performance. Proper test parameters on a good, non-leaky device should show a complete loop, with the beginning and end at 0V.

The load capacitance must be relatively large compared to the FE capacitance to ensure that the voltage drop across the load capacitor is not significant; otherwise, some somewhat-unsatisfactory assumptions have to be applied to obtain the voltage across the FE element. However, this large load capacitance means that the sense voltage is fairly small. This small voltage is difficult to measure accurately with an oscilloscope or digitizer. The PMU+RPM solution does not require the load capacitor method because it measures the current and voltage directly and simultaneously so that the total charge can be accurately determined. The charge is calculated from the high speed current measurements, which are sampled consistently over time, resulting in high speed charge measurements. Note that the value reported is charge, not charge per unit area. However, it's easy to calculate the charge per unit area from the provided charge values by using the Formulator.

Much like PCRAM and other NVM materials, FeRAM cells require a forming step or process before the cell exhibits reproducible switching behavior. The PUND or FERAM endurance tests can be used to apply the forming pulses. The PUND test is appropriate when a small number of pulses are required for forming, whereas the endurance test is better when a larger number of pulses are required. The hysteresis curve can indicate if the test device was sufficiently formed (see the gap at 0V in **Figure 32**).

The hysteresis test applies positive and negative V-shaped pulses to measure the current. Because the current is sampled continuously, calculating the total charge is straightforward. **Figure 31** shows the test signal applied to the FE capacitor, as measured by the PMU+RPM. **Figure 32** shows the hysteresis curve, which was extracted from the data in **Figure 31**. Proper test parameters on a good device should show a complete loop, with the beginning and end at 0V.

The characteristic shape of the hysteresis curve is not only a measure of the inherent ferro-electric material performance but may also show degradation due to the semiconductor processing that occurs after the FE capacitor fabrication.

The PUND test characterizes the polarity change in the ferro-electric material. It is called PUND because four pulses are applied sequentially: Positive, Up, Negative, Down (**Figure 33**). Note the change in the shape of the current between the two up pulses (red P and red U) and similarly for the two down pulses (red N and red D). The first pulse requires additional charge/current to change the polarization (red P or red N), compared to the second pulse, which has the capacitive charging only (red U or red D). The difference between them (P-U or N-D) represents the polarization charge or memory effect. P_{SW} is the polarization change

during the up pulses (P_{SW} = red P – red U). Q_{SW} is an average of the two charges from the two polarities (two up and two down pulses, Q_{SW} = ((red P – red U) + (red N – red D)) / 2). In addition to fundamental device and material characterization, the PUND test is used to determine the proper voltages and timing for the endurance test.

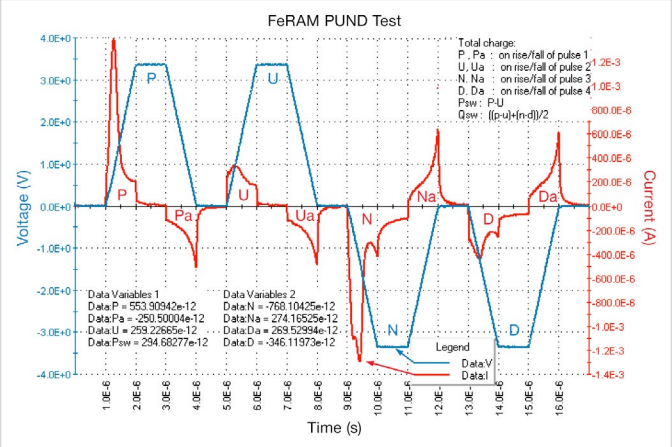

Figure 33. PUND waveforms generated and measured by the 4225-PMU with 4225-RPMs (user module ***pundTest***). This graph shows the applied voltage pulses and the current response. The values for P, U, N, and D are extracted from the current waveform.

The endurance test shows the reduction in the polarization charge as the number of pulses applied increases. For some devices, the polarization charge may increase slightly during the initial pulse stress, before declining with an even larger number of stresses [13]. **Figure 34** shows example endurance results for Q_{SW} and P_{SW}. The degradation in Q_{SW} begins at 11 million cycles. The onset of degradation is a strong function of the pulse amplitude, so different materials and PUND voltages can provide significantly different degradation curves. **Figure 35** shows the change in the charges for P, U, N, and D, which determines the data shown in **Figure 34**.

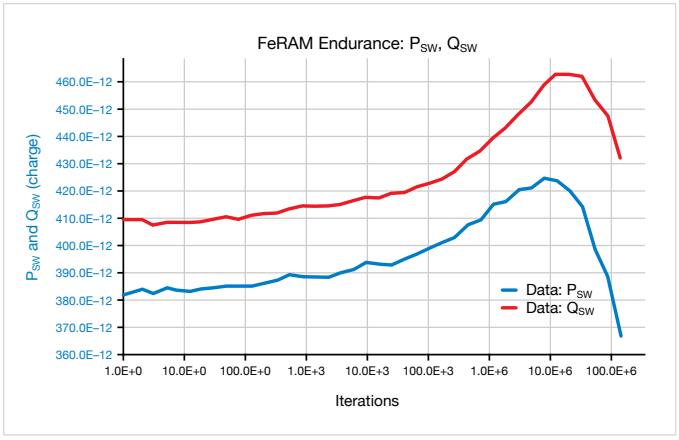

Figure 34. FeRAM endurance, showing the degradation in P_{SW} and Q_{SW} (user module ***pundEndurance***). Some FeRAM endurance curves only show Q_{SW}. This data was taken by the 4225-PMU with 4225-RPMs.

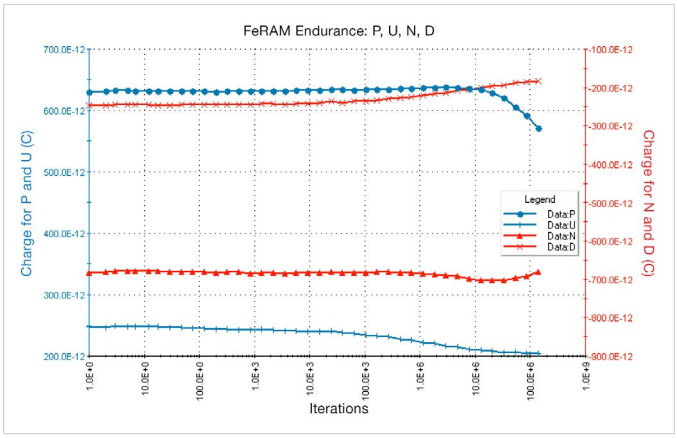

Figure 35. FeRAM endurance, showing the degradation in P, U, N, and D values (user module ***pundEndurance***). This data is used to create the data in Figure 34. This data was taken by the 4225-PMU with 4225-RPMs.

FeRAM Test Modules

There are three modules for testing ferro-electric materials or devices: ***doubleSweep***, ***pundTest***, and ***pundEndurance***.

Setting Up the Parameters in the *doubleSweep* Module

This module is the same module used in the PRAM test ***iv-curve***. However, the PRAM test used just one of the V-shaped pulses, while the FE capacitor hysteresis test uses two pulses (**Figure 27** shows the definition, **Figures 31 and 32** show test results on FeRAM).

Table 6 lists the input parameters for the ***doubleSweep*** module.

Setting Up the Parameters in the *pundTest* Module

This module applies the four pulses that make up the PUND test, with the parameters briefly explained in **Tables 9 and 10**. This test uses both 4225-RPMs connected to the first 4225-PMU in the 4200A-SCS chassis (**Figure 30**). RPM1 outputs the voltage pulses and measures the applied voltage. RPM2 measures the current flowing through the test device. The returned values include the voltage (from RPM1), current (from RPM2), and time arrays. In addition, the charge for each pulse transition is returned. **Figure 36** shows the pulse parameter definitions.

Table 9. Input parameters in the ***pundTest*** module.

Parameter	Range	Description
V_p	–10V to +10V	Voltage level for the four PUND pulses. The first and second pulses are $+V_p$ and the third and fourth pulses are at $–V_p$ (**Figure 36**)
t_p	20ns to 1s	Width of each pulse top
t_d	20ns to 1s	Delay time between each pulse
trf	20ns to 10ms	Pulse transition time for all pulses
Irange1	100nA to 10mA	Current measure range for RPM1 (RPM1 forces voltage)
Irange2	100nA to 10mA	Current measure range for RPM2 (RPM2 measures current)

Table 10. Output parameters in the ***pundTest*** module.

Parameter	Type	Description
V	Double Array	Array of voltage measurements for the PUND waveform
I	Double Array	Array of current measurements for the PUND waveform
t	Double Array	Array of timestamps for the PUND waveform
P	Double	Total charge on rise of pulse 1
P_a	Double	Total charge on fall of pulse 1
U	Double	Total charge on rise of pulse 2
U_a	Double	Total charge on fall of pulse 2
N	Double	Total charge on rise of pulse 3
N_a	Double	Total charge on fall of pulse 3
D	Double	Total charge on rise of pulse 4
D_a	Double	Total charge on fall of pulse 4
P_{sw}	Double	Polarization charge, defined as P – U
Q_{sw}	Double	Average polarization charge: ((p-u)+(n-d))/2
pts	Double	Total number of points recorded

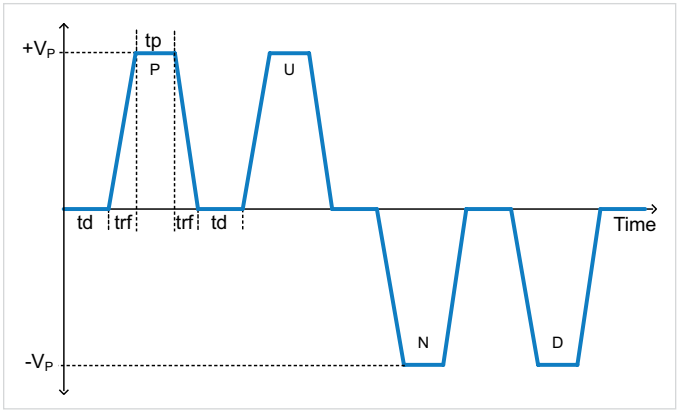

Figure 36. Pulse waveform parameters for pundTest.

Setting Up the Parameters in the *pundEndurance* Module

This module is a stress/measure test that applies the four pulses that make up the PUND test ***max_loops*** times to the test device, with the parameters briefly explained in **Tables 11 and 12**. While applying the stress PUND waveform ***max_loops*** times, the number of measurement intervals is set by ***fatigue_count***. The number of stress waveforms between each measurement is calculated on a log10 basis. The returned parameters are similar to ***pundTest*** and the pulse parameter definitions are shown in **Figure 36**.

Table 11. Input parameters in the ***pundEndurance*** module.

Parameter	Range	Description
V_p	–10V to +10V	Voltage level for the four PUND pulses. The first and second pulses are $+V_p$ and the third and fourth pulses are at $–V_p$
Vfat	–10V to +10V	Voltage pulse level for the two pulses of the fatigue waveform. First pulse is $+(V_p)$, last pulse is $–(V_p)$
T_p	20ns to 1s	Width of each pulse top
t_d	20ns to 1s	Delay time between each pulse.
trf	20ns to 10ms	Pulse transition time for all pulses
Irange1	100nA to 10mA	Current measure range for RPM1 (RPM1 forces voltage)
Irange2	100nA to 10mA	Current measure range for RPM2 (RPM2 measures current)
pts_ per_waveform	10 to 10,000	Number of measure points per PUND measure waveform
max_loops	1 to 10^{12}	Total number of stress waveforms applied to the test device
fatigue_count	2 to 100	Number of measurement intervals during ***max_loops***.

Table 12. Output parameters in the ***pundEndurance*** module.

Parameter	Type	Description
Iteration	Integer: 1 to 100	Number of measurement intervals, must be same or greater than ***fatigue_count***
P	Double	Total charge on rise of the P pulse
P_a	Double	Total charge on fall of the P pulse
U	Double	Total charge on rise of the U pulse
U_a	Double	Total charge on fall of the U pulse
N	Double	Total charge on rise of the N pulse
N_a	Double	Total charge on fall of the N pulse
D	Double	Total charge on rise of the D pulse
D_a	Double	Total charge on fall of the D pulse
P_{sw}	Double	Polarization charge, defined as P – U
Q_{sw}	Double	Average polarization charge: ((p-u)+(n-d))/2

ReRAM and CBRAM Testing

As mentioned previously, ReRAM and CBRAM are types of Redox memory [14]. Both ReRAM and CBRAM are typically tested in the DC realm using SMU instruments, but SMU instruments may not be the best instrument for testing some memory types.

In traditional ReRAM test setups, to create, or form, the low resistance state initially, SMU instrument current compliance is used to limit the maximum current flowing through the test device during the forming or reset operation. The desire is to limit the amount of current to reduce the stress on the cell and also improve the quality of the switching process. However, the compliance circuit in an SMU instrument is not instantaneous, and takes microseconds to milliseconds to engage fully. Before the circuit is active, the amount of current flowing is not fully known or controlled. The actual transient response of the current compliance and the detailed interplay between the changing test device impedance and the reaction of the SMU instrument is complicated and not well understood.

Pulse I-V characterization improves the situation by providing strict timing control of the voltage signal applied to the test device. Tests in the ***Resistive Nonvolatile Memory Characterization Project*** can be used for characterization of ReRAM and CBRAM.

In the project, ReRAM device results are shown. ReRAM memory devices are two terminal devices, with a “low” and “high” side. A voltage pulse is applied across the oxide, and according to the mainstream literature, this creates conductive filaments. The process for creation of filaments is called “forming” and is considered the most important aspect that determines the ReRAM switching behavior. Forming is usually performed with DC voltage sweep with current limit enabled.

The following process takes place, as generally accepted. As voltage ramps up, the electrical field grows. When it becomes sufficient, a conductive filament begins to grow through the material from one electrode to the opposite electrode. As soon as it happens, the current limit engages and arrests the further growth of the conductive filament section. Resistance of the device drops from high resistance to low, for example, from several mega-ohms to the kilo-ohm range. This plausible explanation can bring into question that the speed of current-limit engagement may be important for ReRAM forming and therefore worthy of additional characterization. In the industry it still not common knowledge that the speed of a DC (SMU instrument) current limit is relatively slow, in the ~100µs range.

An ideal solution to this problem is to design structures with current-limiting control transistors directly on-wafer. This will ensure minimum parasitic capacitance and minimum response time. If, however, a current limit is not available on the wafer, it is suggested to use both SMU instrument current limiting and 4225-RPM current limiting to better understand forming mechanisms.

After forming, the applied RESET pulse changes resistance of the structure from low resistance to high. It is thought to be caused by the destruction of the conductive filament in the vicinity of the one of the electrodes. ReRAM structures can be symmetrical or polar. Polar devices require certain polarity of the forming pulse, and have non-symmetric material layouts. For polar devices, the Forming (and Set Pulse) have an opposite polarity from the Reset pulse.

Figure 37 shows the tests used for ReRAM testing. The characterization test is a standard test, where a ReRAM device is tested and verified that it is valid and can be used.

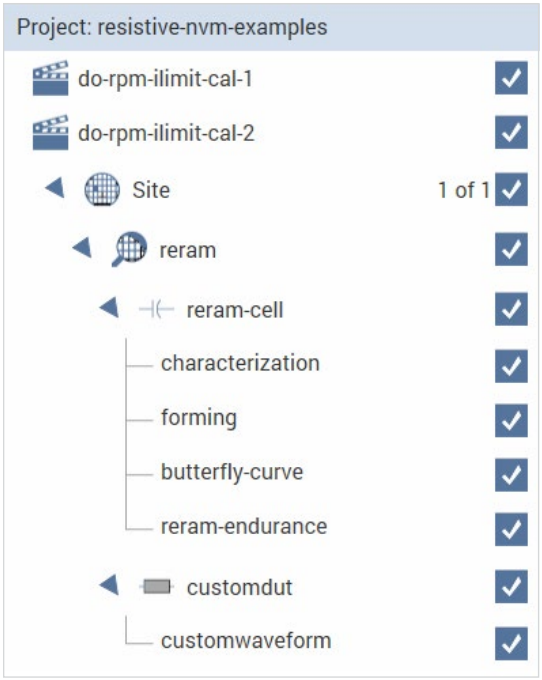

Figure 37: Screenshot of the tests for the ***ReRAM Project.***

The ***forming*** and ***butterfly-curve*** tests are a Set/Reset sequence. The ***reram-endurance*** test is an endurance test. **Figure 38** shows the connection diagram for a two terminal ReRAM device, showing both the pulse and SMU instrument connections. Note that if there is a chuck or backside connection, please connect RPM #1 to this terminal.

In **Figure 39**, the blue curve, using the left y-axis, shows transient voltage applied to the ReRAM device. The red curve, using the right y-axis, is the current response. Note that the x-axis is time, in hundreds of microseconds. The voltage amplitude is ±2.3V. The same data is also plotted as I vs V as shown on the right. Exponential dependency of the current on the bias demonstrates that the device is not yet formed and can be used for characterization.

This data was collected with a PMU and two RPMs, using test routine, reramSweep; it can also be configured to use SMU instruments to collect similar data. There are several main differences between tests with PMU with RPMs and SMU instruments. First, the SMU instrument sweep takes significant time, up to several seconds, while the PMU+RPM sweep can be as fast as hundreds of nanoseconds. Second, the current limit capability for an RPM is much faster than an SMU instrument. An SMU instrument current compliance "engage time" is approximately 100–500µs, depending on the particular configuration and SMU instrument model, while an RPM limit can be as fast as several hundred nanoseconds, effectively ~3 orders of magnitude faster. While a control transistor, located on-wafer, would be faster and better in terms of energy control, the RPM current limit does provide research benefits compared to the SMU instrument testing. Using the PMU+RPM provides information that may help during the complicated and potentially costly transition to

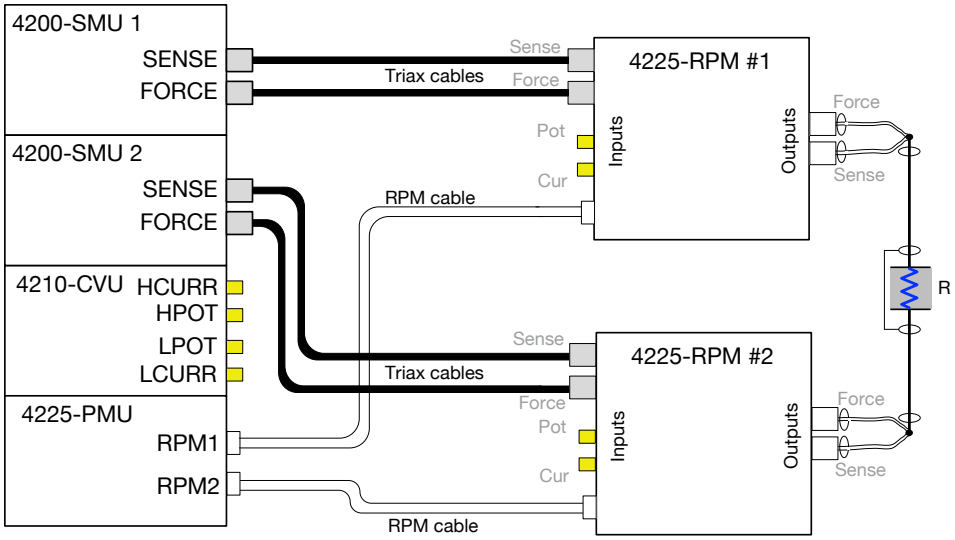

Figure 38. Connection to the 2-terminal ReRAM device.

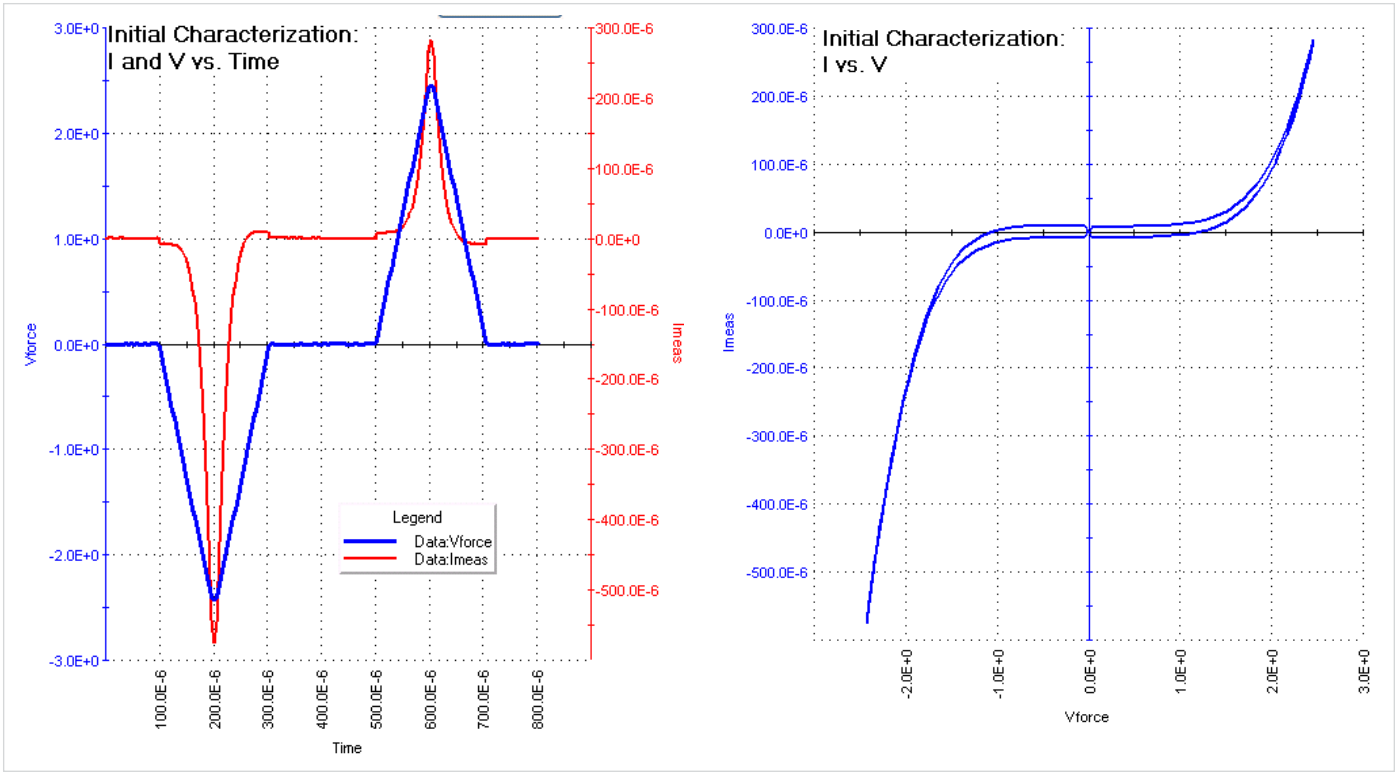

Figure 39. Characterization test of ReRAM structure.

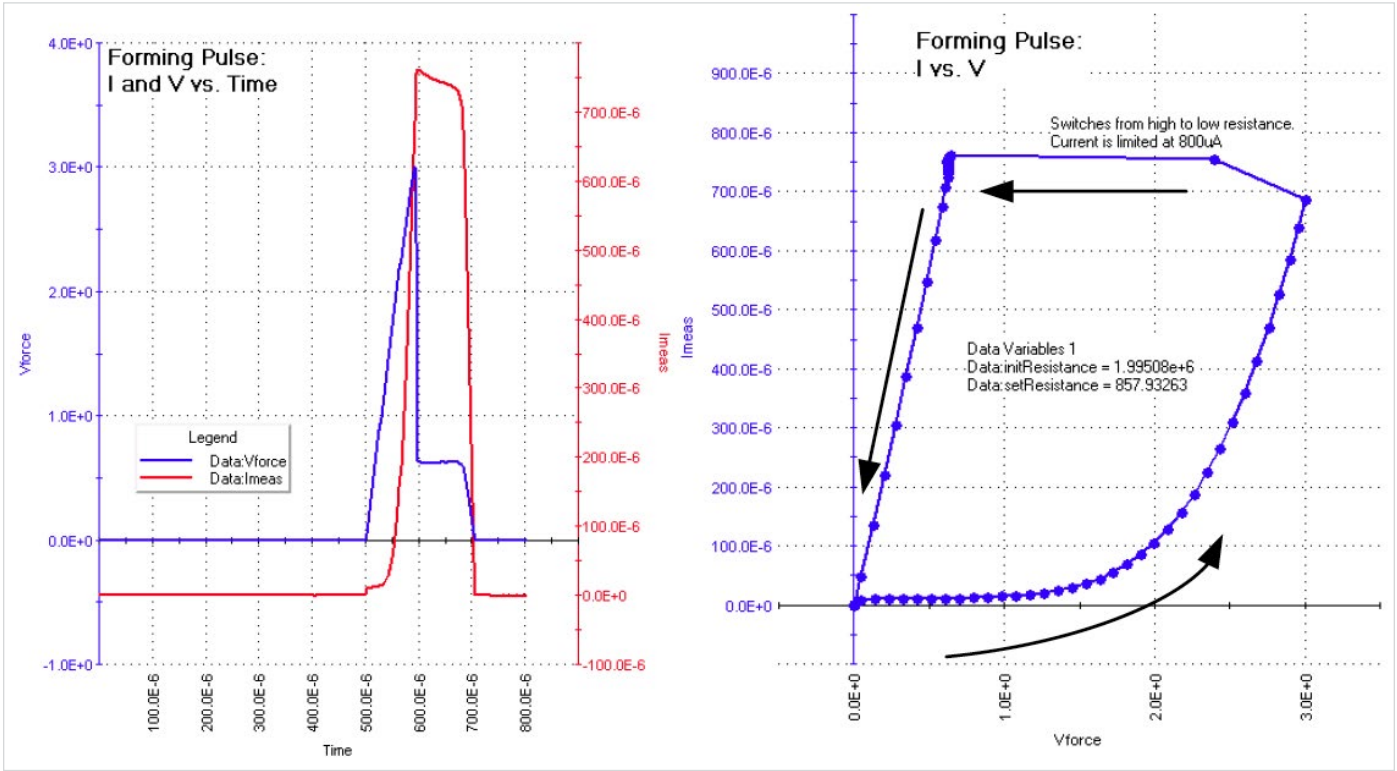

Figure 40. ReRAM forming.

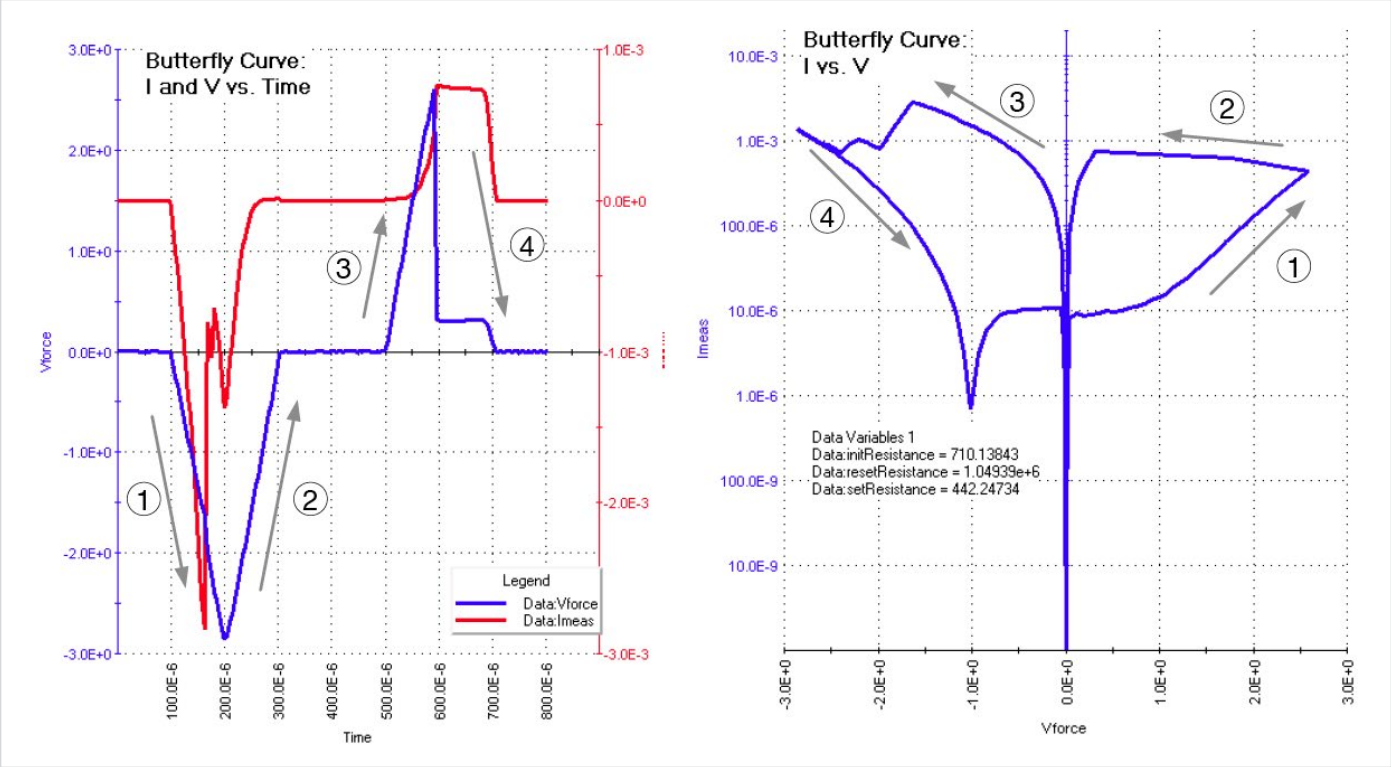

Figure 41. ReRAM "Butterfly" curve.

adding an on-wafer current limit capability. Another benefit to the pulse approach is using a second PMU+RPM channel to avoid capacitive charging effects by measuring the current through the test device on the low or side opposite the pulsing (**Figure 50**). The faster current limit is also useful during constant voltage stressing (CVS). Traditionally, CVS was performed using SMU instruments, but it can also be done using the PMU+RPM approach.

A detailed explanation of Capacitive Charging Effects during Pulse Transitions is given below.

ReRAM forming results are shown in the two graphs of **Figure 40**. The graph to the left is voltage and current transients (V and I vs. time), and the graph to the right is the same data plotted as current vs voltage. Current exponentially grows as voltage reaches a certain value. When the filament is established, the device switches into low resistance state and the current limit prevents further growth of the filament. Forming was performed using a PMU+RPM with current limit enabled. A standard test configuration, used by most of the researchers in ReRAM field is to use DC instruments, SMU instruments, with current compliance. Forming performed with a PMU+RPM, unlike the the SMU instrument approach, is able to measure current and power transients during forming, while forming done with an SMU instrument completely hides details of the process. According to the literature, the forming process is controlled mostly by the value of the current limit and the speed of its activation. The right graphs shows the same data, but with the current plotted vs the voltage. The added arrows show the time progression of the curve, to allow for comparison to the time-based graph on the left.

The same test routine that was used for characterization and forming was applied to an already formed device to collect the "Butterfly" curve, as shown in **Figure 41**. The chart to the left, as before, shows the current and voltage transient (I and V vs. time). The chart to the right is current vs. voltage in the shape of butterfly wings. The same routine, reramSweep [use fixed-width font], with different test conditions, can obtain both DC (SMU instrument) data and Pulse (PMU) data. This allows convenient switching between DC and PULSE modes of ReRAM characterization.

The left wing of the butterfly curve is a RESET transition, when resistance switches from low resistive state to high resistive state; note that the current limit is not enabled.

Voltage polarity is opposite to the polarity used for forming and SET. During RESET process, it is commonly assumed, that conductive filament loses continuity from one electrode to another one, but this affects a small section of the filament. The SET process is very similar to the Forming process, in that it uses pulses of the same polarity to re-establish continuity of the conductive filament from one electrode to another one. Since the SET bias does not have to grow the whole filament, just reestablish the connection; it requires less bias than the Forming process does. The SET procedure, similar to Forming, requires the use of the current limit capability but at a lower current level.

Selection of the test parameters for ReRAM testing, including Forming, SET, and RESET, follows a logical progression for initial forming and characterization.

1. First, prior to any forming, the test device is verified to be good and that it demonstrates a non-linear I-V dependency (**Figure 39**). During this initial pre-screening, care should be taken to use a voltage lower than the forming, SET, and RESET voltages.

2. Forming is a critical process (**Figure 40**). The value of the maximum bias should be selected to trigger filament growth. At the same time the current limit should be small enough, thereby preventing the filament from becoming too stable. If a conductive filament is too stable, than no amount of the Reset bias will disconnect the filament and no sufficient electrical field in the filament can be achieved. The value of the voltage bias for the RESET pulse should be just enough to break the filament.

3. Current limit for the SET bias, similar to Forming, should be just large enough to reconnect the filament, but not too large to prevent a “disconnect” in the next SET/RESET cycle. Selection of the Forming/SET and RESET parameters are somewhat tricky, require sufficient investigation, and in a critical way control the endurance of the ReRAM device. The endurance is defined as maximum number of SET/RESET cycles, where the LOW and HIGH resistance states are sufficiently different.

Figure 42 gives an example of the endurance test of a ReRAM structure. The endurance test is similar to endurance tests for PRAM, Flash, and FeRAM. The control parameter, which in case of resistive memory, is resistance, and has two states, low and high. Low resistance corresponds to the state when conductive filament is formed and connected opposite electrodes across the oxide. High resistance is the state where a small section of the filament is converted back to high resistive material. Selection of the Forming, SET, and RESET processes defines how many cycles it will take for the low resistance state to become indistinguishable from the higher resistance state, which is one way to determine the maximum number of cycles for device endurance.

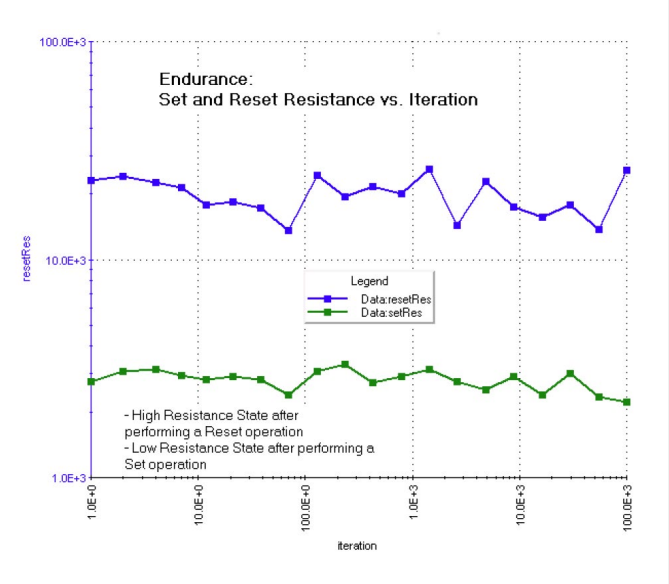

Figure 42: ReRAM endurance test.

Setting up the Parameters in the *reramSweep* Module

The ***reramSweep*** module is used to perform a double sweep with a flat section at the peak of each sweep. To test a ReRAM device, the user chooses appropriate values for the two peaks, either positive or negative, and then sets the timing (**Figure 43, Table 13**). Either SMU instruments or a PMU with 2 RPMs can be used, depending on the setting of useSmu parameter. The Low side (**Figure 38**) of the device needs to be connected to PMU channel 1 using a RPM. “Low” side is defined as the side connected to the bulk, substrate, or chuck if there is connection between DUT and the substrate. SMU1 is also connected to channel 1, RPM1. SMU2 is connected to the channel 2 RPM. The voltage bias is applied to channel 1, channel 2 is kept at virtual ground potential and current is measured on channel 2.

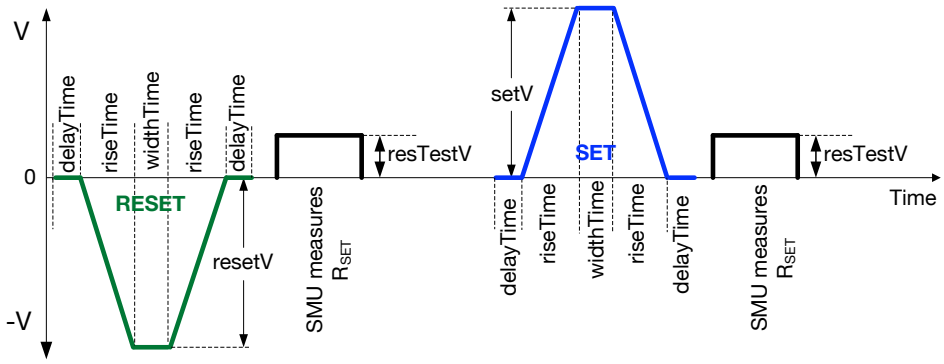

Figure 43. Pulse waveform with measure for ***reramSweep*** and ***reramEndurance***.

Table 13. List of Input Parameters in the reramSweep module (see **Figure 43**)

Parameter	Range	Description
riseTime	2e-8s to 33 ms	The time it takes for voltage to ramp to the SET or RESET voltage. This value is slew rate-limited. To reach the slowest rise time, a higher voltage must be used.
widthTime	2e-8s to 1s	The time to wait at the top of the pulse at full voltage
delayTime	20 ns to 1 s	The time between the SET and RESET pulses
compliance	1 or 2	On which SMU instrument channel to enforce current compliance
resetV	–20V to 20V	The peak voltage of the reset pulse. For ReRAM devices, this value should be negative.
setV	–20V to 20V	The peak voltage of the set pulse. For ReRAM devices, this value should be positive.
Irange	100nA to 10mA for RPM 10 pA to 1A for SMU	The range at which to measure current. The SMU instrument has more ranges and also accept 0 for autorange.
resetIcomp	–100mA to +100mA	Please note that this variable is used both for PMU and SMU instrument control during RESET. If it is set to 0, then no current limit is applied. If useSmu = 1, and sweep is performed with the SMU instrument, and current limit is 0, autorange is used. With current limit not zero and useSmu = 1, the SMU instrument is set in the fixed current range.
setIcomp	–100mA to +100mA	Please note that this variable is used both for PMU and SMU instrument control during SET. If it is set to 0, then no current limit is applied. If useSmu = 1, and sweep is performed with the SMU instrument, and current limit is 0, autorange is used. With current limit not zero and useSmu = 1, the SMU instrument is set in the fixed current range.
resTestV	–10V to +10V	SMU instrument voltage used to measure device resistance.
takeRmeas	0 or 1	Whether or not to take resistance measurements. 1 means yes, take resistance measurements, while 0 means no, do not take resistance measurements.
useSmu	0 or 1	Whether or not to use an SMU instrument to take DC measurements instead of using the PMU+RPM for pulsing measurements. A 1 means yes, use the SMU instrument and a 0 means no, don't use the SMU instrument, use the PMU.
numIter	1 to 100	This parameter should be set to 1.
Vforce_size Imeas_size Time_size	10 to 10000	These three values should be the same and represent the number of items in the output arrays.

Table 14. List of Output Parameters in the reramSweep module.

Parameter	Description
Vforce	Array of forced voltages
Imeas	Array of measured currents
Time	Array of measured times
resetResistance	Resistance of DUT after the reset pulse
setResistance	Resistance of DUT after the set pulse
initResistance	Resistance of DUT before any pulse

Setting up the Parameters in the *reramEndurance* Module

The reramEndurance routine is used to perform a series of double sweeps (SET+RESET) using the same parameters used for the single sweeps as described in the reramSweep routine. To test a ReRAM device, choose appropriate values for the two peaks, either positive or negative, and then set the timing you would like to implement. Choose the number of times you would like to run the double sweep (***max_loops***) and how often you want to take measurements (***fatigue_count***). The routine will use a log10 approach to spacing the total number of measurements (***fatigue_count***) across the total pulses (***max_loops***). For example, if ***max_loops*** = 10000 and ***fatigue_count*** = 4, then there will be R_{SET} and R_{RESET} measurements after 10, 1000, 1000, and 10000 SET+RESET pulses applied to the test device.

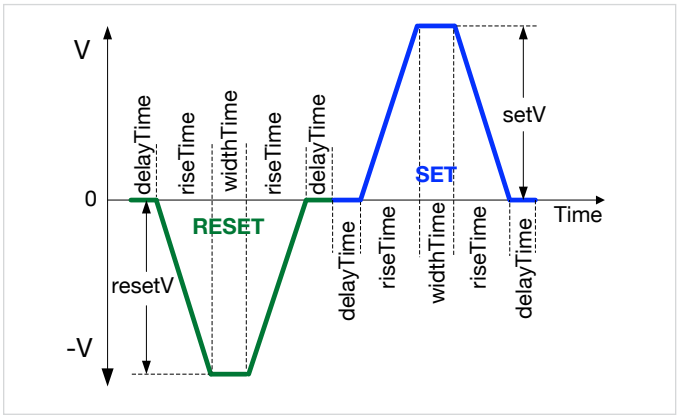

Figure 44. Pulse waveform parameters for the stress reramEndurance.

RPM current limit calibration

The pulse current limiting capability is provided by the 4225-RPM. The short distance of the RPM to the DUT minimizes parasitic capacitance and time it takes for the current limit to activate and become effective. As mentioned above, this time is ~3 orders of magnitude smaller than the current compliance activation time for a typical DC SMU instrument. The RPM current limit capability requires initial and periodic calibration. Before using the current limit feature of the 4225-RPM, calibration has to be performed manually by calling routine ***Do_RPM_Ilimit_Cal*** (from user library ***RMP_ILimit_Control***). This test is included in the ReRAM and PRAM projects at the top of the project tree.

Note that the 4225-RPM-LR does not have the current limit feature. Attempting to perform a current limit calibration on or set the current limit of a 4225-RPM-LR module will cause an error.

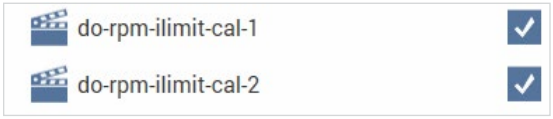

Figure 45. RPM Current limit tests in the ReRAM project tree.

Here, two calls are shown to calibrate both RPMs (**Figure 45**). To execute a calibratation procedure for channel 1 of PMU1, set up input conditions to the routine as in **Figure 46**, and connect SMU2 to the force output connector of the RPM1. To calibrate the channel 2 RPM, use the ***do-rpm-ilimit-cal-2*** test (**Figure 45**) and connect SMU1 to the force output connector RPM2 and use SMU1 for parameter ***smuname***. The quality of the calibration is determined by correlation factors called PosRsq and NegRsq. Calibration is considered successful if both these numbers are close to 1.000, with at least the first 4 or 5 digits = 9 (**Figure 47**, showing 999.995E-3 or 999.999E-3). The calibration will drift due to temperature, so for better performance, daily calibration is recommended. The current limit range is from ~10µA to 10mA.

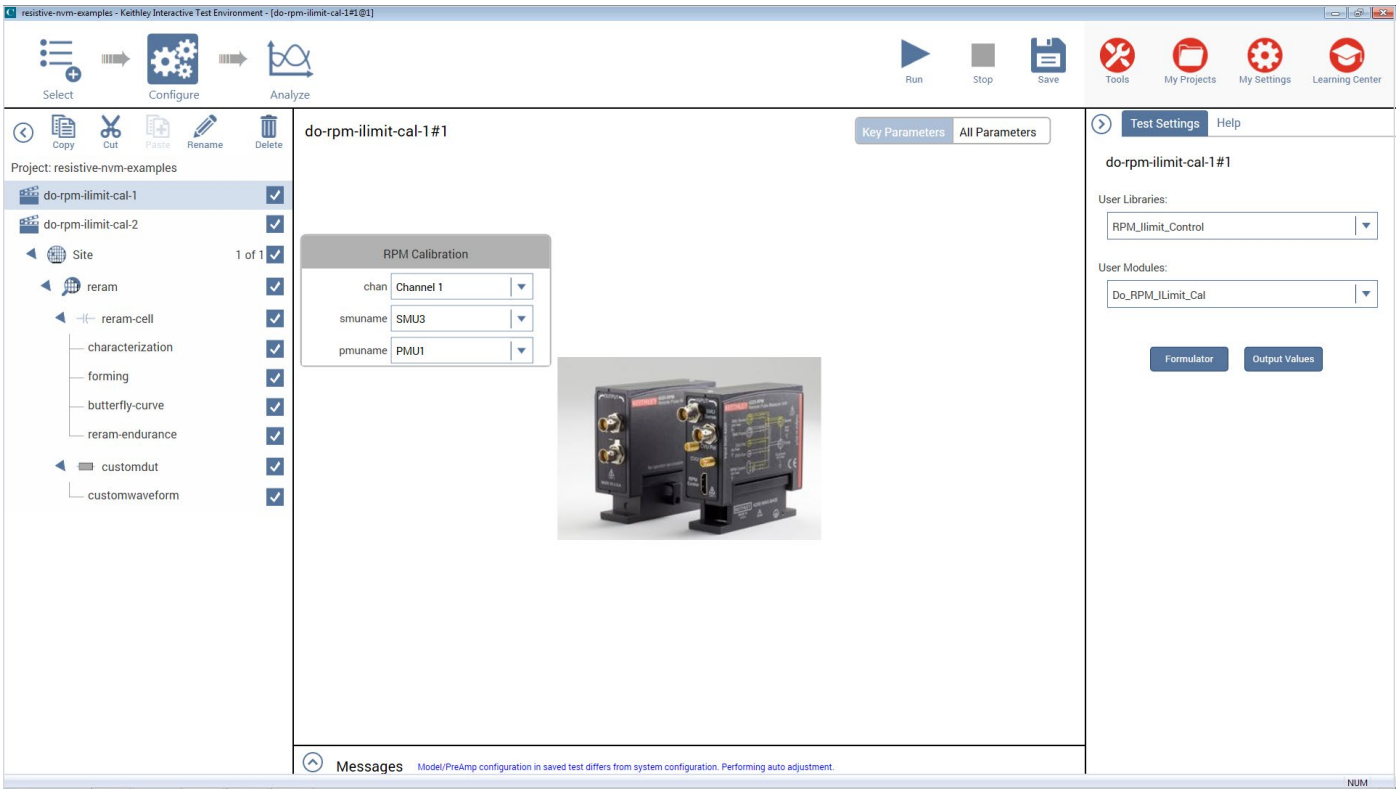

Figure 46. Settings for current limit calibration of the PMU channel 1 RPM.

Do_RPM_ILimit	PosRsq	NegRsq
0	999.9990E-3	999.9950E-3

Figure 47. Example good results for RPM Current limit calibration, as shown in the Sheet.

Status and Error Codes for the nvm User Library

When debugging an error, start with the error code below (**Table 17**) and also look at the debug log file (C:\nvmlog.*txt*).

Optimizing Measurements

Because the 4225-PMU and 4225-RPM provide waveforms for each of the pulse waveform tests, determining the pulse fidelity is greatly simplified compared to source-only pulse systems. During initial setup, use the pulse waveforms to confirm proper voltage levels and timing response in addition to the extracted values (V_T, SET R, Hysteresis, PUND).

When measuring, there is always a tradeoff between the size of the measure window vs. the noise floor. A longer measure time will provide a less noisy result. The 4225-PMU and 4225-RPM also follow this fundamental fact of measurement. However, because timing is a primary parameter, the tradeoff is more visible and therefore more controllable.

In addition to noise, note that lower current measure ranges have slower response than higher ranges. This is true for SMU current ranges, as well as 4225-PMU and 4225-RPM ranges. For example, the 4225-RPM current measurement settles much faster on the 10mA range (100ns best case) than the 100µA range (750ns best case). This means that sometimes using a higher current measure range will permit shorter pulse timing parameters because of the faster settling time but at the expense of a bit more noise.

Table 15. List of In put Parameters in the ***reramEndurance*** module (see Figure 43 and Figure 44).

Parameter	Range	Description
riseTime	4e-8 to 1e-2s	The time it takes for voltage to ramp to the final value
widthTime	4e-8 to 1e-2s	The time to wait at the top of the pulse at full voltage
delayTime	4e-8 to 1e-2s	The time between the two pulses and between the sweeps
useSmu	0 or 1	Should stay zero. Used for debugging purposes
compliance	CH 1 or 2	On which SMU instrument channel to enforce current compliance
resetV	–20 to 20V	The peak voltage of the reset pulse. For ReRAM devices, this value should be negative
setV	–20 to 20V	The peak voltage of the set pulse. For ReRAM devices, this value should be positive
Irange	0 to 0.2	The range at which to measure current
resetIcomp	–100mA to +100mA	Please note that this variable is used both for PMU and SMU instrument control during RESET. If it is set to 0, then no current limit is applied. If useSmu = 1, and sweep is performed with the SMU instrument, and current limit is 0, autorange is used. With current limit not zero and useSmu = 1, the SMU instrument is set in the fixed current range.
setIcomp	–100mA to +100mA	Please note that this variable is used both for PMU and SMU instrument control during SET. If it is set to 0, then no current limit is applied. If useSmu = 1, and sweep is performed with the SMU instrument, and current limit is 0, autorange is used. With current limit not zero and useSmu = 1, the SMU instrument is set in the fixed current range.
resTestV	0.1 to 2V	The voltage at which to measure the resistance of the DUT. This should be much less than the set and reset voltages as to not set or reset the DUT
max_loops	1 to 10^{12}	Number of pulses to output and stress the test device. Set the fatigue_count to determine the number of measure intervals within the max_loops number of pulse waveforms.
fatigue_count	2 to 100	Number of times to measure during the max_loops tests, using a log interval. For example, if max_loops = 1000 and fatigue_count = 4, there will be measurements of the SET and RESET resistance after 1, 10, 100, 1000 SET+RESET pulse waveforms are applied to the test device.

Table 16. List of Output Parameters in the ***reramSweep*** module.

Parameter	Range	Description
reset	Resistance	Resistance of DUT after the reset pulse
set	Resistance	Resistance of DUT after the set pulse
init	Resistance	Resistance of DUT before any pulse

Table 17. Error codes and descriptions for the ***nvm*** user library.

Code	Description
1	Test ran successfully
–10	Could not initialize NVM structure
–20	Return arrays are not the same size, or ***iter_size*** is smaller than ***fatigue_count***
–40	Current range on one of the channels is too large, should be 10mA (10e-2) or less
–50	Error in ***pg2_init***
–60	Error in ***pulse_load***
–70	Error in ***pulse_ranges***
–80	Error in ***pulse_burst_count***
–90	Error in ***pulse_output***
–100	Error in ***pulse_standby***
–110	Error in ***pulse_sample_rate***
–120	Error in ***Set_RPM_ICompliance***
–130	Error in ***seq_arb_sequence***
–140	Error in ***pulse_exec***
–150	Error in ***pulse_fetch***
–160	No points returned
–170	Error in ***seg_arb_waveform***
–210	Error completing the test
–220	Error during measurement

Capacitive Charging Effects During Pulse Transitions

Figure 48 shows a simplified block diagram of a configuration used to create the waveforms shown in **Figure 49**. During pulse transitions, current flows to charge and discharge capacitance in the test system. This current is not flowing through the DUT but does flow out from the instrument and into the cabling, as shown in **Figure 48**. This charging current is measured by the PMU+RPM. **Figure 49** shows the capacitive charging effect using the pulse waveforms. The equation for this effect is:

$$I = C\ dV / dt$$

where:

I is the capacitive charging current.

C is the capacitance of the system (that is, the capacitance "seen" by the measurement circuit).

dV is the change in voltage.

dt is the change in time, in this case, the pulse transition or pulse rise and fall time.

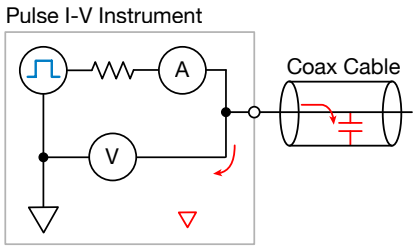

Figure 48. Block diagram of pulse I-V instrument showing the capacitive charging current during pulse transitions.

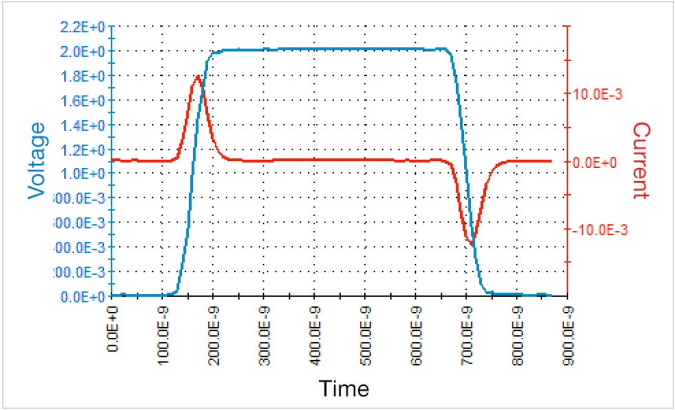

Figure 49. Capacitive charging effect. The blue curve is the voltage pulse applied to a short length of coax cable. The red curve is the resulting current flow, measured from the same side as the applied voltage pulse (***Figure 48***, or Channel 1 in ***Figure 50***). The charging effects are the humps in the red curve during the voltge pulse transition.

This effect is fundamental and not implementation-specific, meaning that all instruments that measure high speed current will measure this effect. Note that measurements during the pulse top are not affected, which means that pulse I-V results are not affected by capacitive charging/discharging. This capacitive charging effect has not been previously seen because nearly all waveform measurements were voltage only.

Based on the equation, the effect is caused by the dV/dt and the C. Generally, the capacitance of the cable is larger than the DUT or instrument capacitance. The capacitance can be minimized by using shorter cable, but there will always be some capacitance in the instrument and in the interconnect. The dV/dt can be reduced by either reducing the voltage or increasing the rise and fall times. Reducing the voltage is usually not an option, as it is the desired signal level for characterization. Reducing the time may be possible in certain situations, but the time is a key test parameter for transient characterization.

The dV/dt provides the hint to a solution to the capacitive charging effect. Measuring the current on the other side of the DUT, away from the applied pulse, is the key to avoiding the effect. **Figure 50** shows the connection setup. Note that the side of the device connected to Channel 2 has a dV/dt that is essentially 0 for most cases. The results of the two-channel setup are shown in **Figure 51**. Note that there is no charging or discharging effect seen during the pulse transitions. This approach is sometimes called pulsing on the high side (red curve in **Figure 51**) and measuring the current on the low side. Note that high and low are referring to the relative voltages across the device.

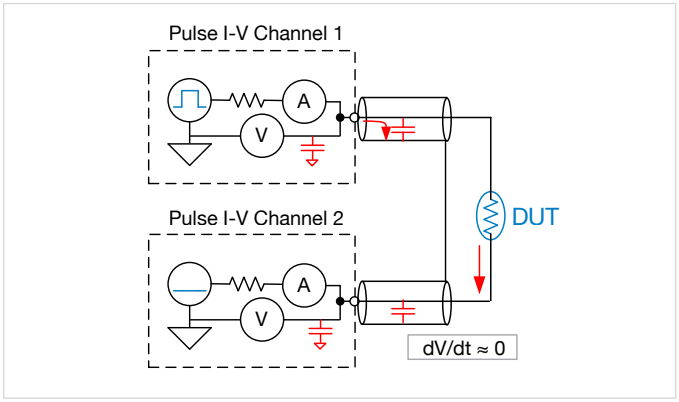

Figure 50. Block diagram of two pulse I-V channels connected to a two-terminal device.

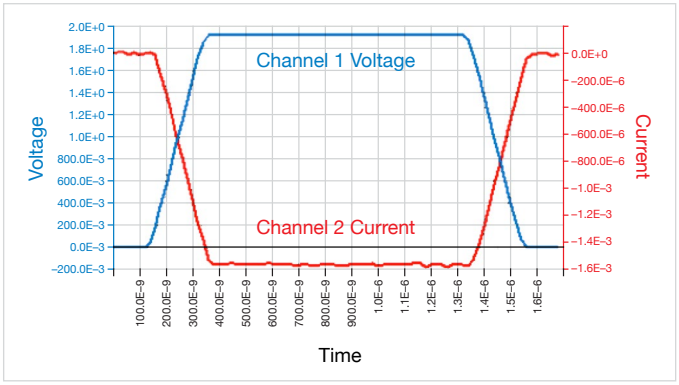

Figure 51. Pulse I-V waveforms for the configuration shown in Figure 50. No capacitive charging current is seen during the pulse transitions, only the current flowing through the resistor DUT.

Test Equipment

Minimum configuration:

- 4200A-SCS
- Two SMU instruments, either medium-power (4200-SMU) or high-power (4210-SMU). Note that the SMU instruments are used in the Flash and ReRAM tests only.
- One 4225-PMU with two 4225-RPMs
- Optional: Compiler to modify the nvm user modules (Order Number: 4200-Compiler)

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