Tektronix

泰克云上大讲堂

光通信眼图精讲

[讲师介绍]

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泰克科技资深项目拓展经理

直播时间

7月23日（周五）14:30-16:00

	日程
14：30 - 15：30	**光通信眼图精讲**
15：30 - 15：45	互动与答疑
15：45 - 16：00	抢答有奖

抢答有奖思考题（需填写小问卷后答题才生效喔~）：

1. 为什么要使用hit ratio来进行眼图模板测试?

2. 为什么眼图模板测试最终被取代?

3. PAM4 TDECQ测试较之NRZ时代的类似测试有何不同?

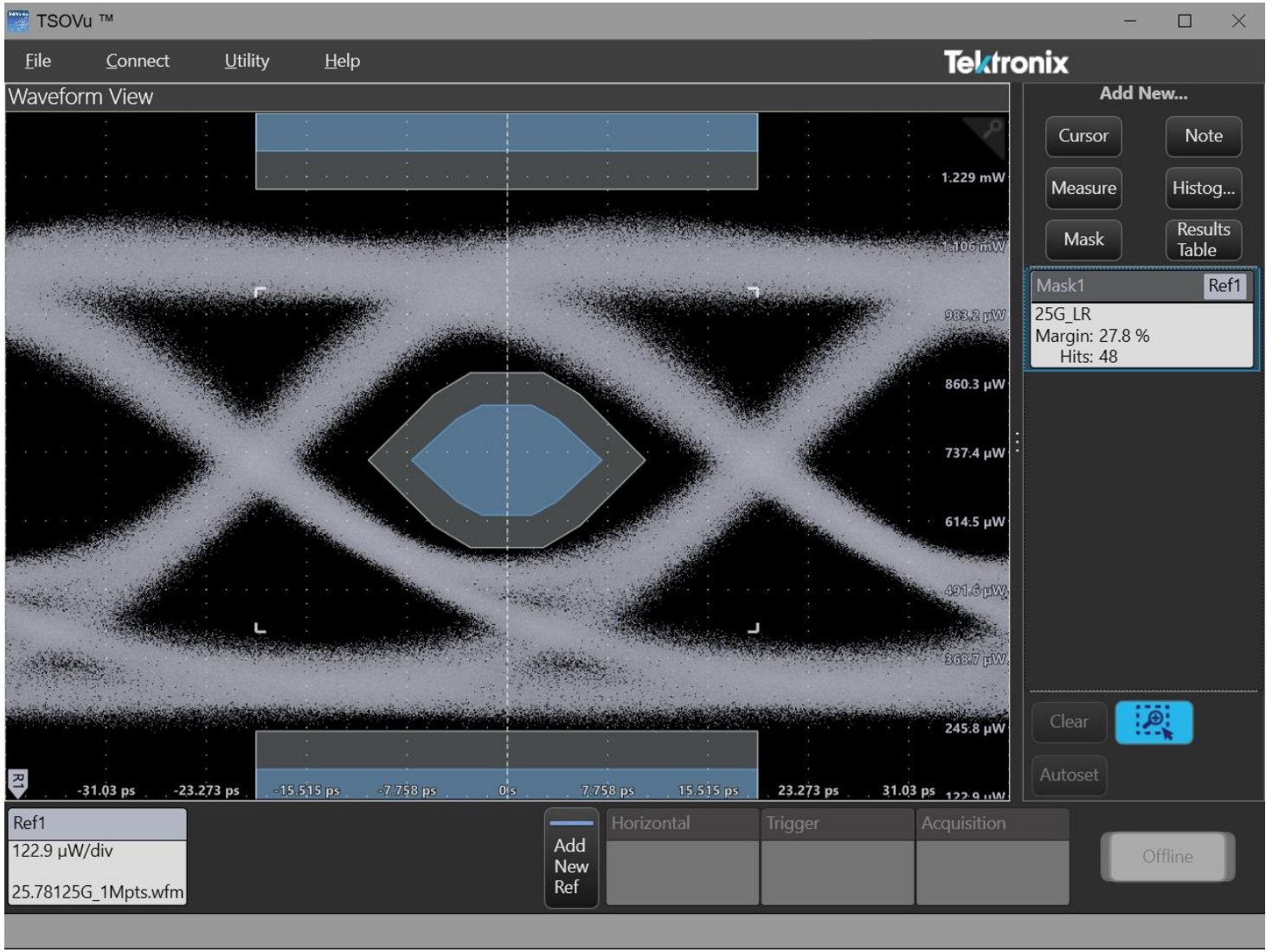
Tektronix

Looking for the BEST eye

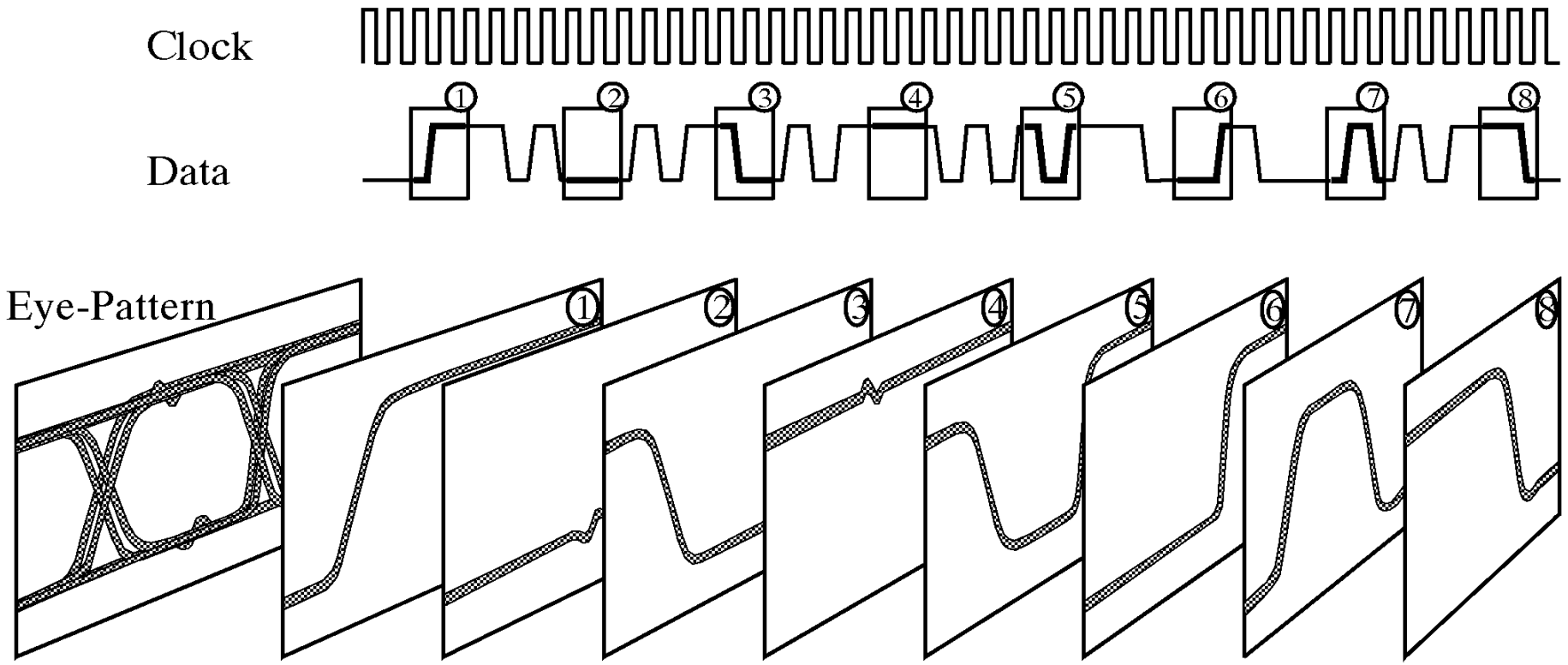
TEKTRONIX CHINA AE TEAM

Eye diagram, a traditional method for signal test

- Vertical
  - SNR
- Horizontal
  - Tr/Tf
  - Jitter

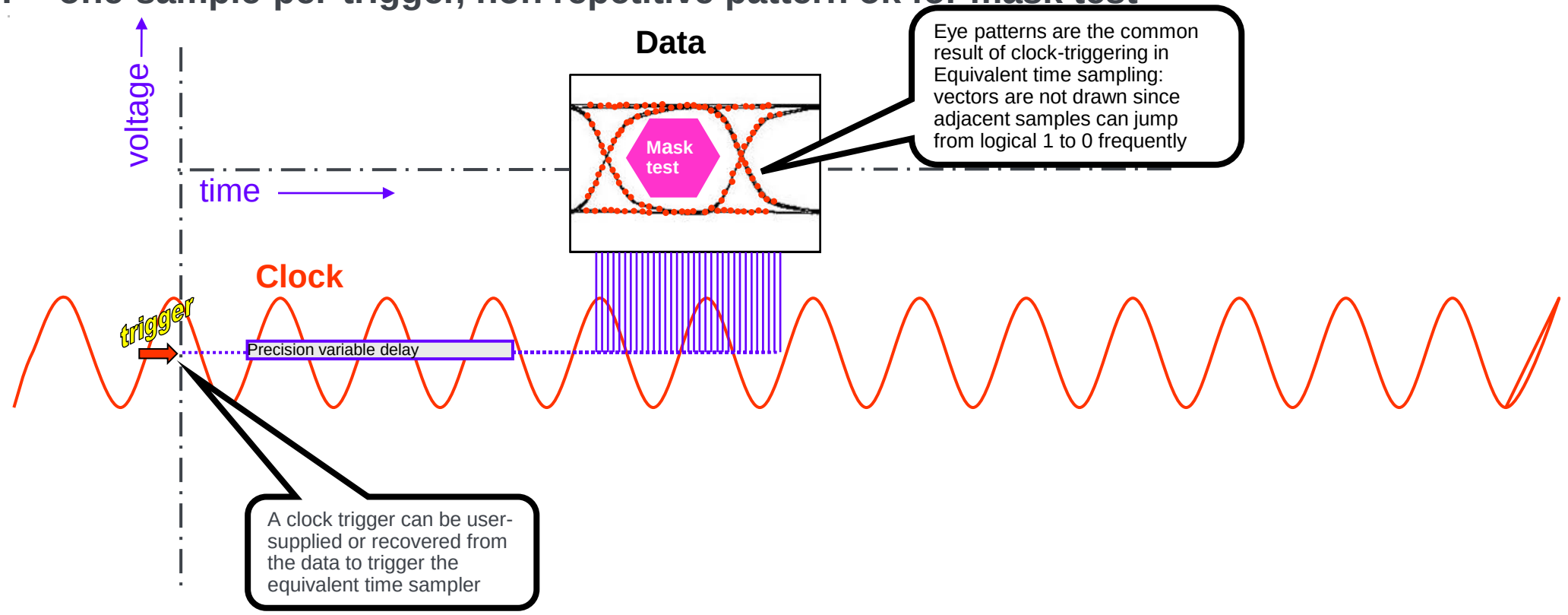


The eye diagram on the scope



ET-RT Basics:

ET – one-sample-per-trigger, non repetitive pattern ok for mask test



- *When a clock signal is used to trigger the equivalent-time sampling scope the sampled DATA signals generally create EYE PATTERNS (between clock triggers the sampled DATA could be either a logical 1 or 0)*

We never stop looking for the best DUT

WHAT IS “BEST”

- What we are looking for?
  - A “PASS” device
  - If we could mark the devices as “PASS” , “Good” , “Fantastic” we might sell with different prices to reach the highest profit
  - Customers might choose the “Better” device between me and competitors.

- What is a “good test” ?
  - Good test puts bad devices into PASS, and Bad devices into FAIL
  - Good test measures the parameters that matter to end user and to production
  - Good test finds margin accurately and repeatably

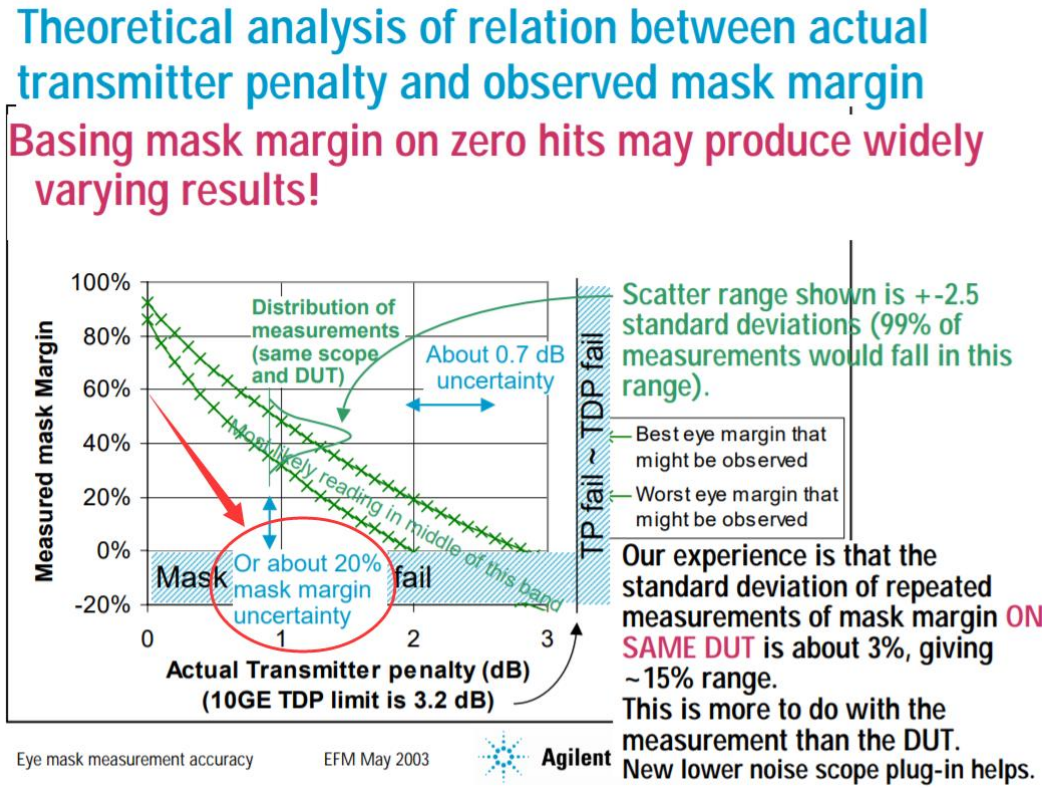
Why are we testing devices…

- Why are we testing?
  - To separate bad devices from good devices
  - To track production and control the result
  - To find the margin of devices

- What is a “good test” ?
  - Good test puts good devices into PASS, and Bad devices into FAIL
  - Good test measures the parameters that matter to end user and to production
  - Good test finds margin accurately and repeatably

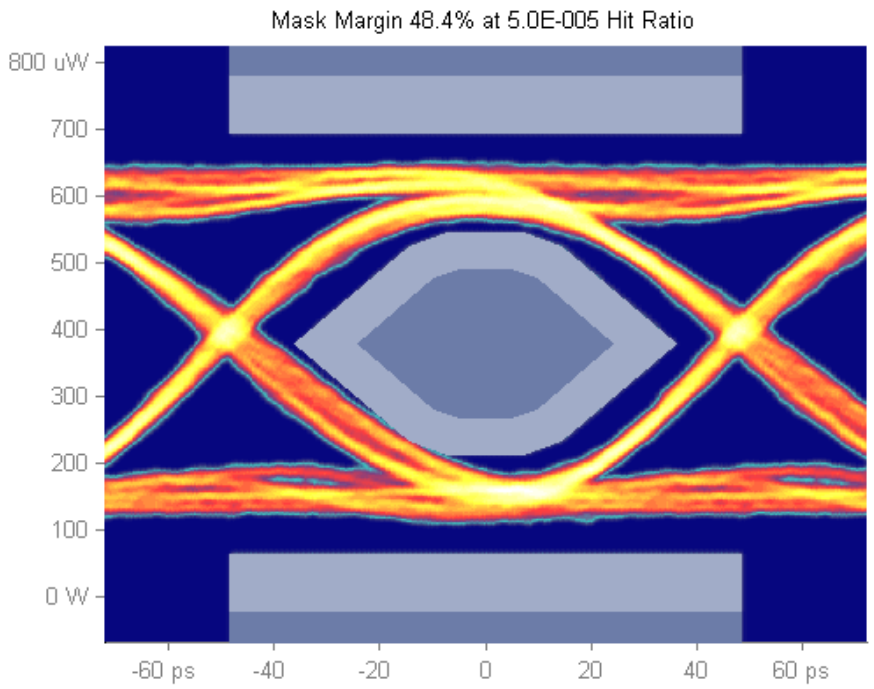
“Zero hit” is a BAD method

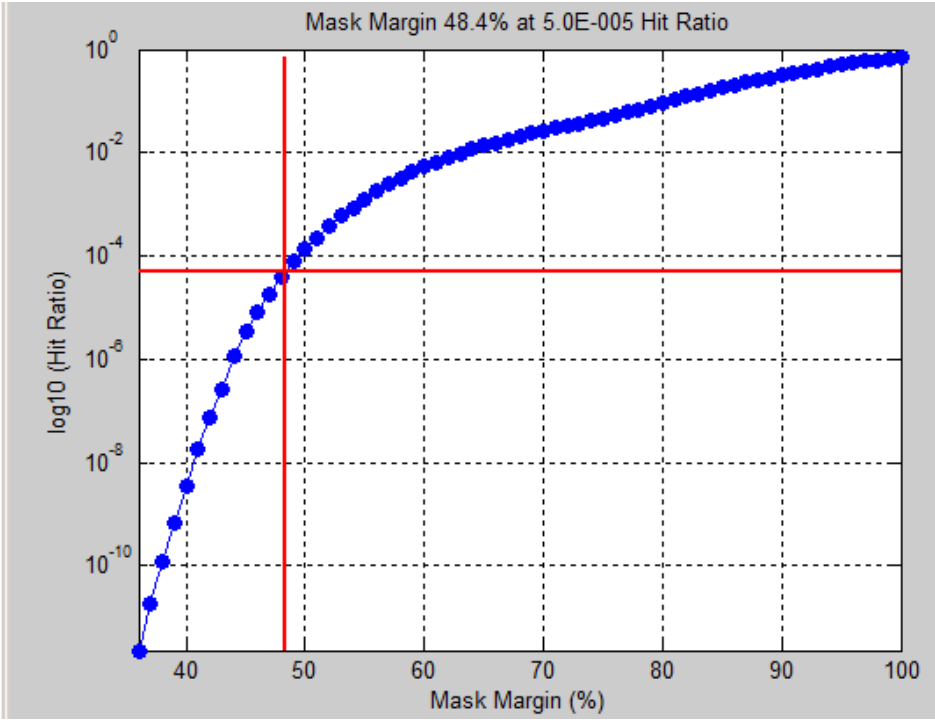
- Industry standard use to be “200 waveforms no hit”
  - The mask margin results are varying
    - About 20% mask margin uncertainty (Agilent’s paper)
  - The more waveforms or samples captured issue the worse result
- Hit Ratio, 802.3aq @2006 defined the hit ratio 5E-5 as mask margin test
  - Mentioned the “hit ratio” method @ 2003 EFM
  - 10GBase-LRM defined 5E-5



More mask test: *what* is **the trade-off between the mask margin and hit ratio?**

- For a particular case (eye diagram on the left, 48 % margin at 5E-5 10GBASE-LR hit ratio masi) what is the mask margin vs. hit ratio? – plot on the left
- Lower hit ratio takes much longer time. 5E-6 10x time to 5E-5





Mask test conclusion

- Should use “hit ratio” instead of “0 hit”

- Mask test has finally achieved maturity…
- … and thus it figures that it would be replaced *!*
  - 100GBASE-SR4 defines TDEC
  - PAM4 standards (“400G”) define TDECQ

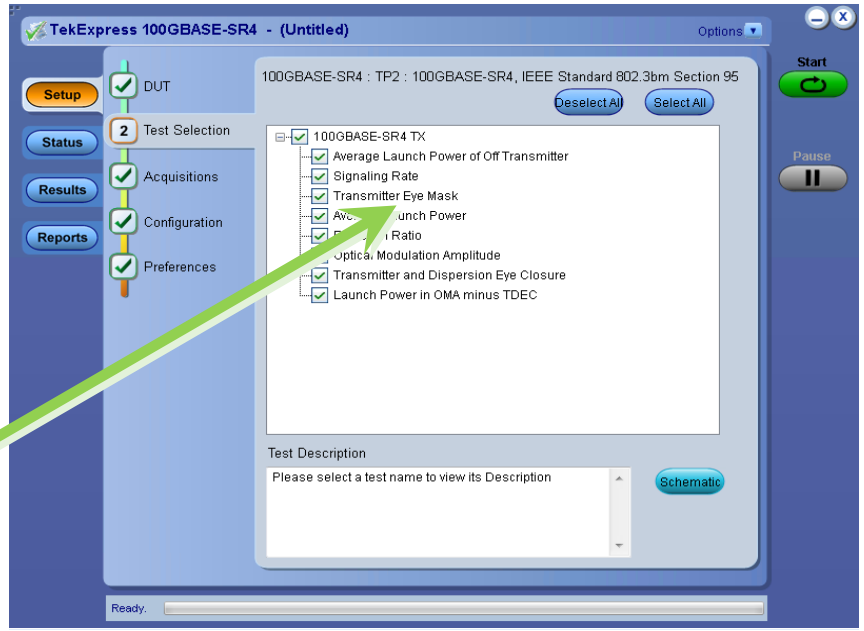
- Reason to replace mask test:
  - Its correlation to BER (bit error rate) (or for PAM4 to SER, symbol error rate) is not direct enough
  - Margin is not in terms usable to the link designer

TDEC test for multi-mode standards

- 100GBASE-SR4 testing; concept ok for PAM4 as well

Table 95–6—100GBASE-SR4 transmit characteristics

Description	Value	Unit
Signaling rate, each lane (range)	25.78125 ± 100 ppm	GBd
Center wavelength (range)	840 to 860	nm
RMS spectral width[a] (max)	0.6	nm
Average launch power, each lane (max)	2.4	dBm
Average launch power, each lane (min)	–8.4	dBm
Optical Modulation Amplitude (OMA), each lane (max)	3	dBm
Optical Modulation Amplitude (OMA), each lane (min)[b]	–6.4	dBm
Launch power in OMA minus TDEC (min)	–7.3	dBm
Transmitter and dispersion eye closure (TDEC), each lane (max)	4.3	dB
Average launch power of OFF transmitter, each lane (max)	–30	dBm
Extinction ratio (min)	2	dB
Optical return loss tolerance (max)	12	dB
Encircled flux[c]	≥ 86% at 19 μm ≤ 30% at 4.5 μm	
Transmitter eye mask definition {X1, X2, X3, Y1, Y2, Y3} Hit ratio 1.5×10^{-3} hits per sample	{0.3, 0.38, 0.45, 0.35, 0.41, 0.5}	



Tektronix TekExpress 100GBASE-SR4 / TDEC solution.

So – what is TDEC, and where did the mask test go?

100 GBASE-SR4 and TDEC

- TDEC replacing both mask test and TDP, Transmitter and Dispersion Penalty (TDEC: Transmitter and Dispersion Eye Closure penalty)
- To characterize the transmitter's waveform shape, observe its ISI as vertical eye closure
- To include modal dispersion, emulate m. d. with a low pass filter… also leads to vertical eye closure

95.8.5.1 TDEC conformance test set-up

A block diagram for the TDEC conformance test is shown in Figure 95–3. Other measurement implementations may be used with suitable calibration.

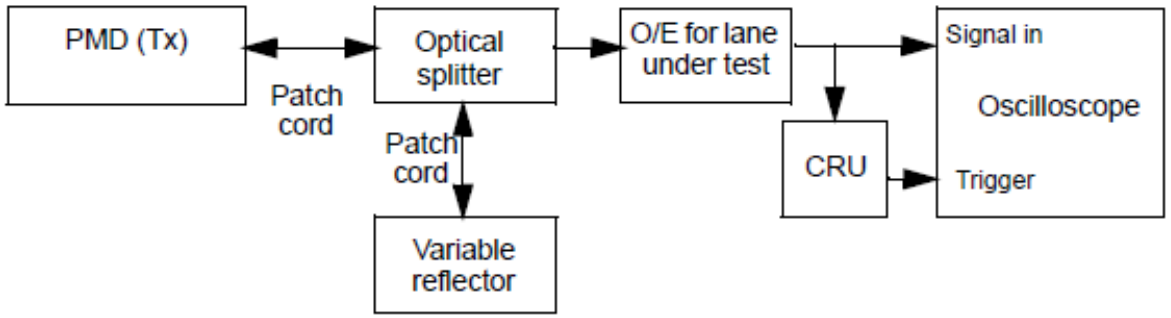


Figure 95–3—TDEC conformance test block diagram

TDEC measurement process

- All about the vertical eye closure
- Relatively complicated processing of four histograms to find the eye closure to BER of interest

This accumulates the histograms (PDFs, probability density functions) into a CDF, cumulative density function)… equivalent to a BER contour, not to a waveform density

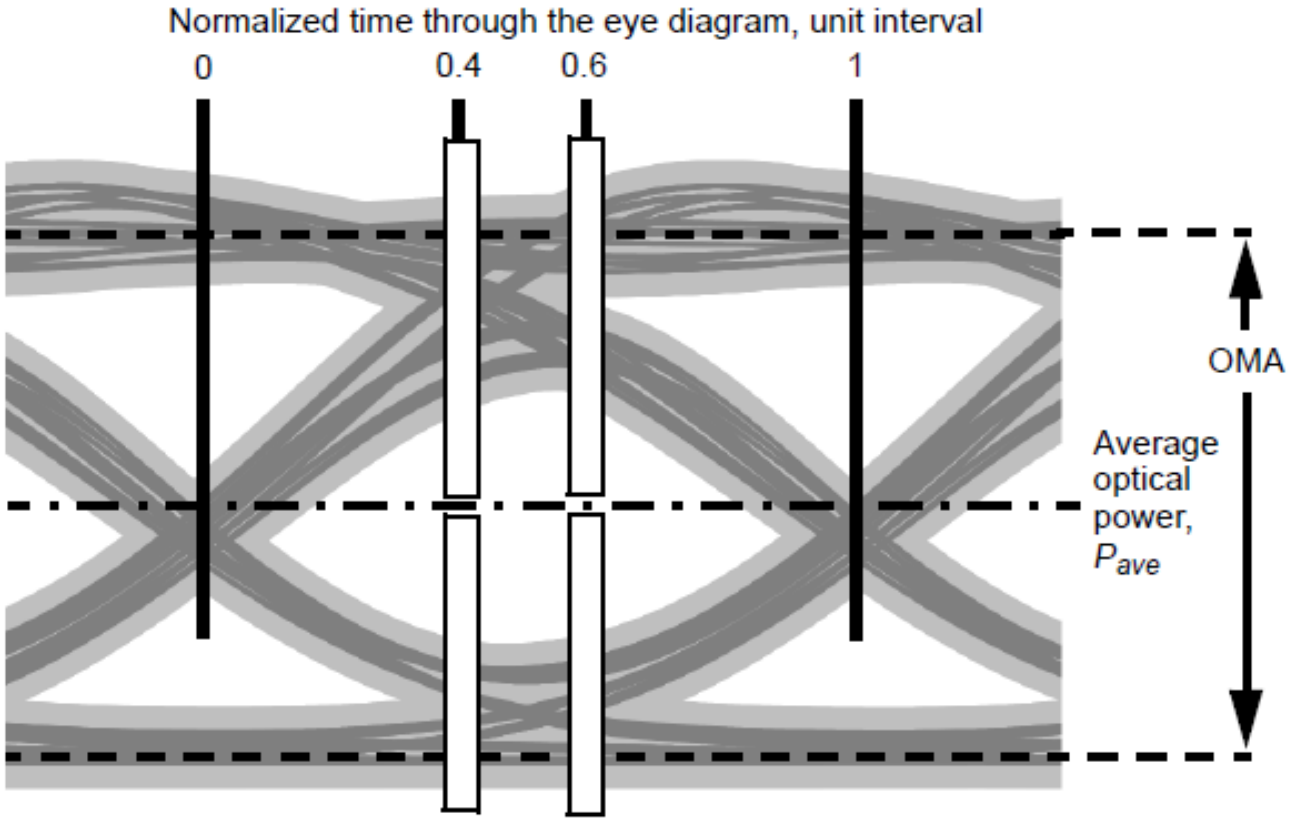
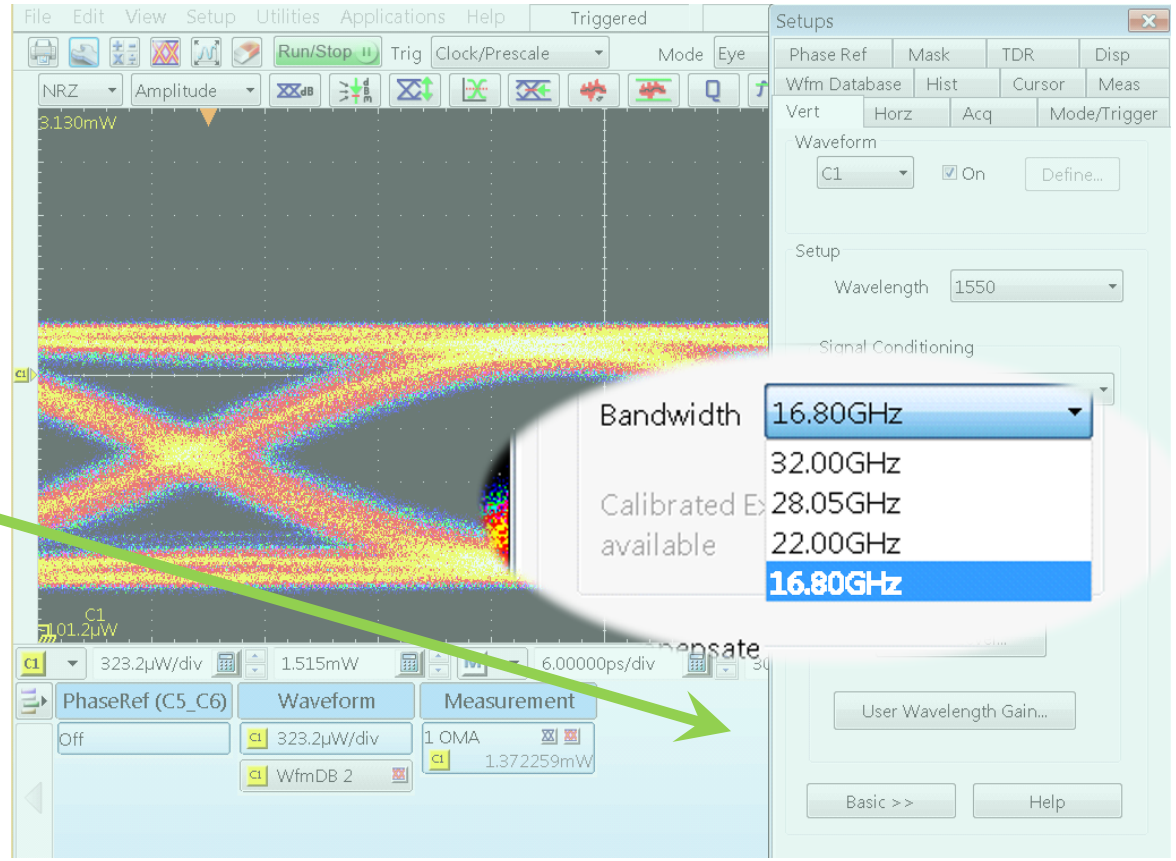


Figure 95–4—Illustration of the TDEC measurement

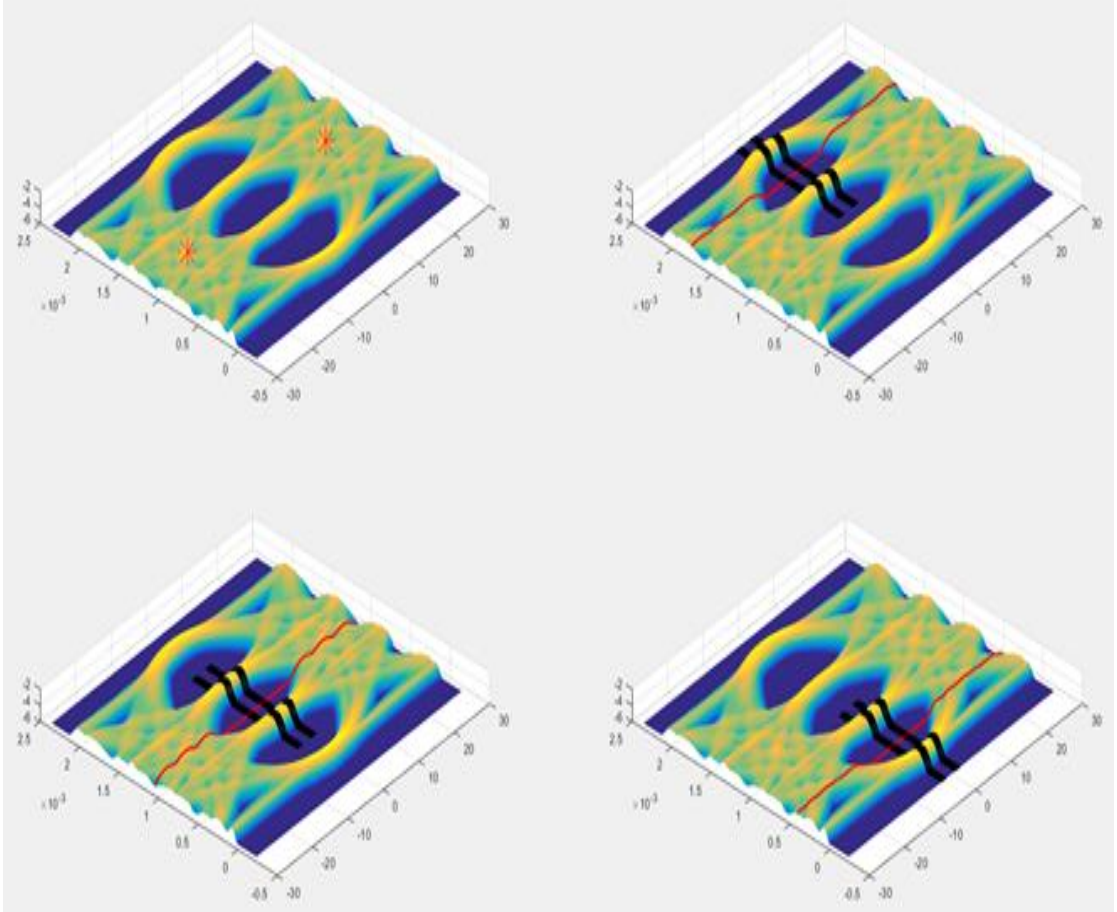
TDEC: special filter emulates modal dispersion

- TDEC is at best 0 dB (i.e. no penalty – the TX is IDEAL)
- Standards set the highest TDEC (highest penalty) allowable
- TDEC for Multi Mode fiber uses special BW limiting in the module:
  (BWoptical shown; BWelectrical 12+ GHz)
- Discussion on SR4
  and TDEC
- Is this so different than a mask test?
  →includes channel
  →'mask' really now a rectangle
  →test the CDF (not probability of waveform)



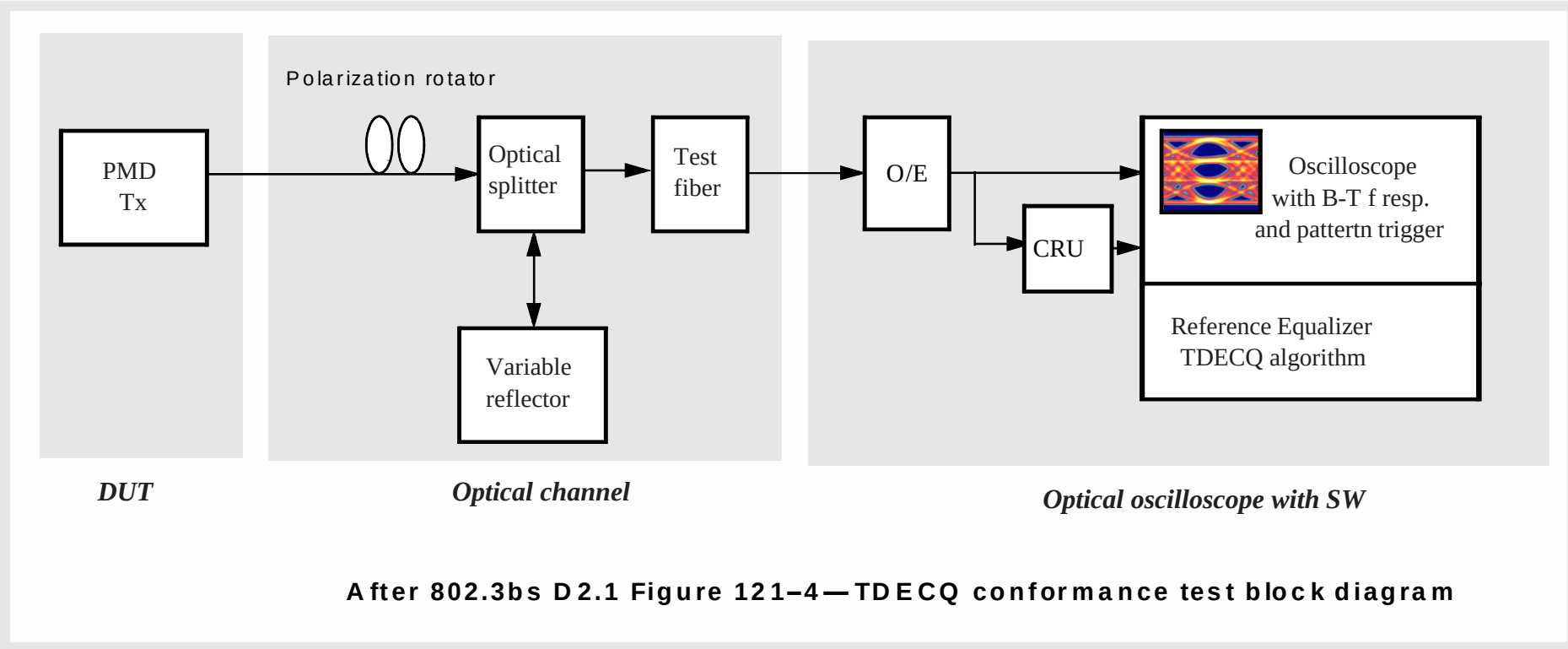
PAM4 test: no eye mask test anymore
Mask → TDECQ (quaternary)

- Optical measurement on *equalized* optical links with PAM4
- Transmitter waveform-shape penalty
- Dispersion penalty: insert fiber (see next page) with max and with min dispersion



TDECQ measurement setup

- (TDEC: Transmitter and Dispersion Eye Closure penalty Quaternary)

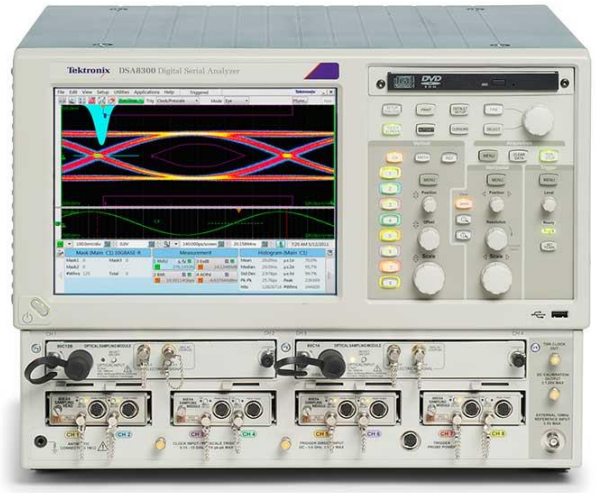


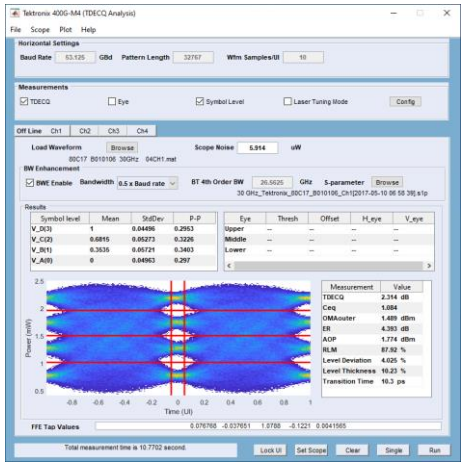
After 802.3bs D2.1 Figure 121–4—TDECQ conformance test block diagram

- Difficult part of TDECQ: Equalization!

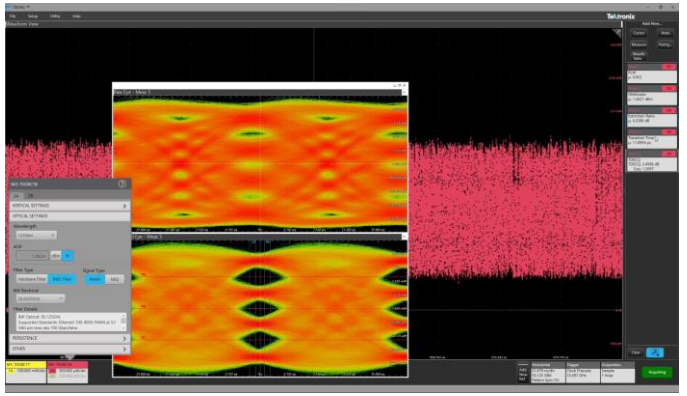
Performance Sampling products

DSA8300





8 Series

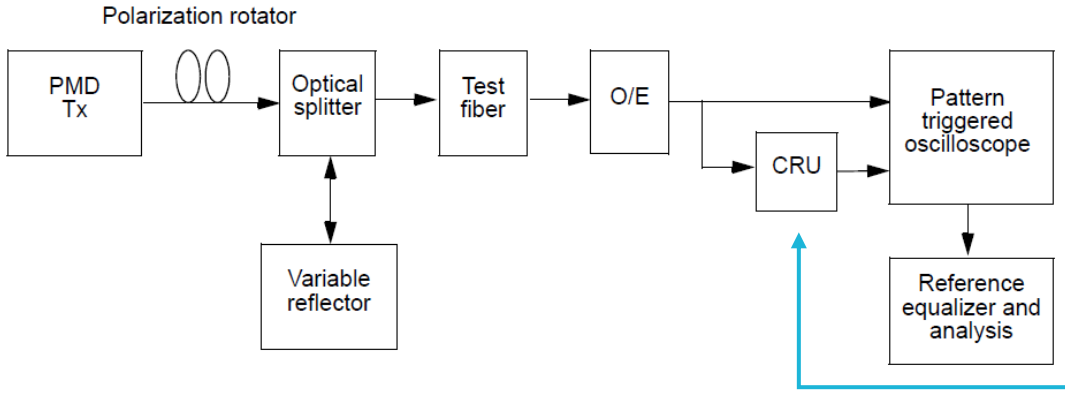


TCR801

TCR801 Clock Recovery

WHAT CHANGED ON THE TRANSCEIVER MARKET?

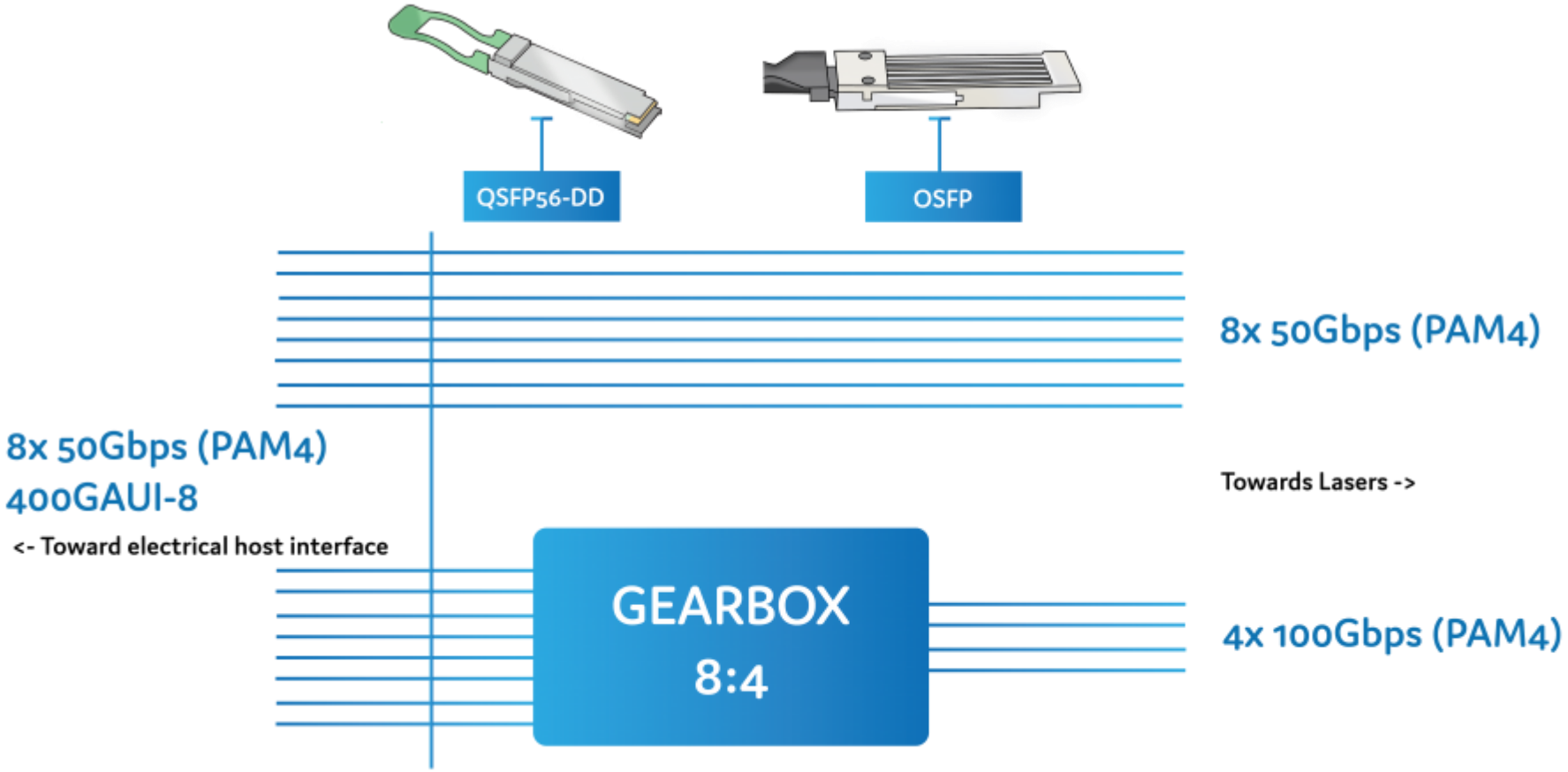
- Technical Challenges:
  - No access to a stable clock to trigger the scope
    - Resulting in false passes or higher yield loss
  - IEEE 802.3bs/cd **mandates** to use an optical clock recovery in order to guarantee accurate results unless you prove alternate solution with same results.
- Clock Recovery Units in the standards:



400GBASE-DR4: The clock recovery unit (CRU) has a corner frequency of 4 MHz and a slope of 20 dB/decade. The CRU can be implemented in hardware or software depending on oscilloscope technology.

Optical clock recovery will guarantee no field failures!
Optical clock recovery will guarantee highest yield.

If gearbox inside, then needs CDR



Optical Clock Recovery: TCR801

TECHNICAL SPECIFICATION

Product	Options	Nomenclature	Description
TCR801		TCR801	26 and 53GBd Optical Clock Recovery – 50/50% splitter included
Optical splitter	SPLT20	TCR801 SPLT20	20% 1310nm Optical Splitter
Optical splitter	SPLT10	TCR801 SPLT10	10% 1310nm Optical Splitter

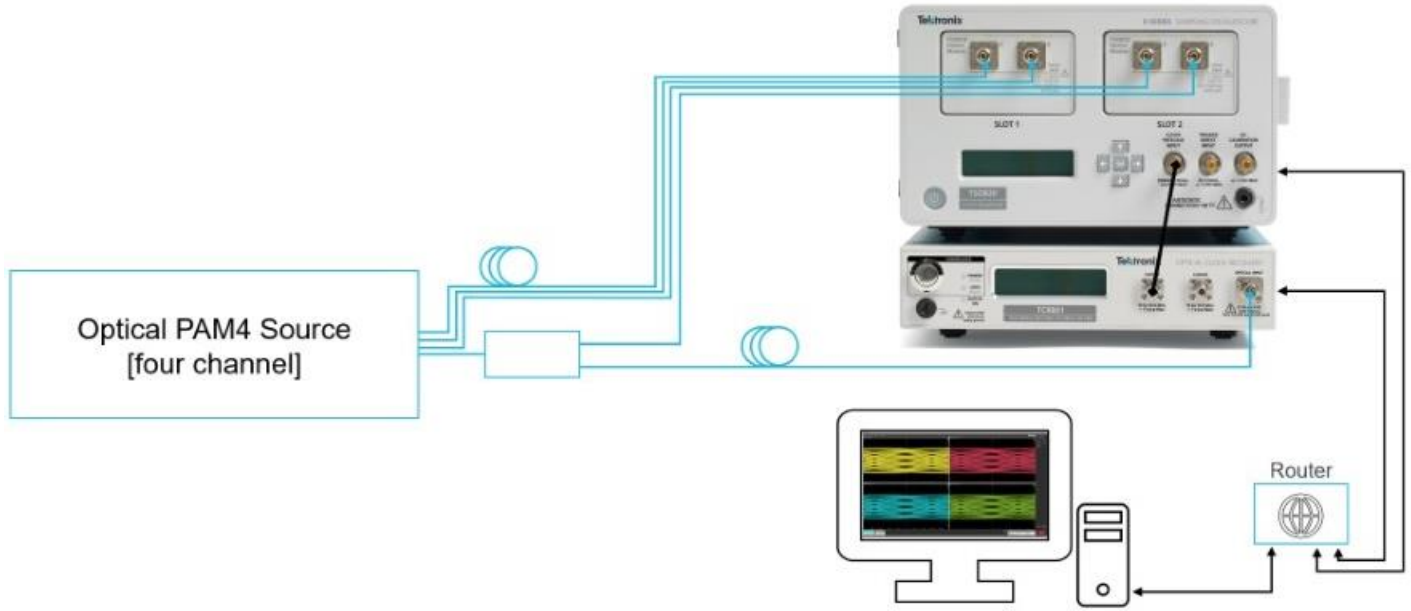
- ✓ Covers narrow band ranges around both 26 and 53 GBd
- ✓ SMF, PAM4 and NRZ, external optical splitter (50/50, 80/20 or 90/10)
- ✓ Works with the Tektronix TSO820 Sampling Oscilloscope, DSA8300, and others
- ✓ Required when external trigger for sampling oscilloscopes is not available
- ✓ Interface with the equipment over Ethernet
- ✓ User selectable external optical splitter; 50/50 optical splitter **included**

Key features

- Designed to lock in two ranges
  - 25.6 to 28.5 GBd PAM2/NRZ or PAM4
  - 51.2 to 58 GBd PAM2/NRZ or PAM4
- 1250 nm to 1650 nm wavelength

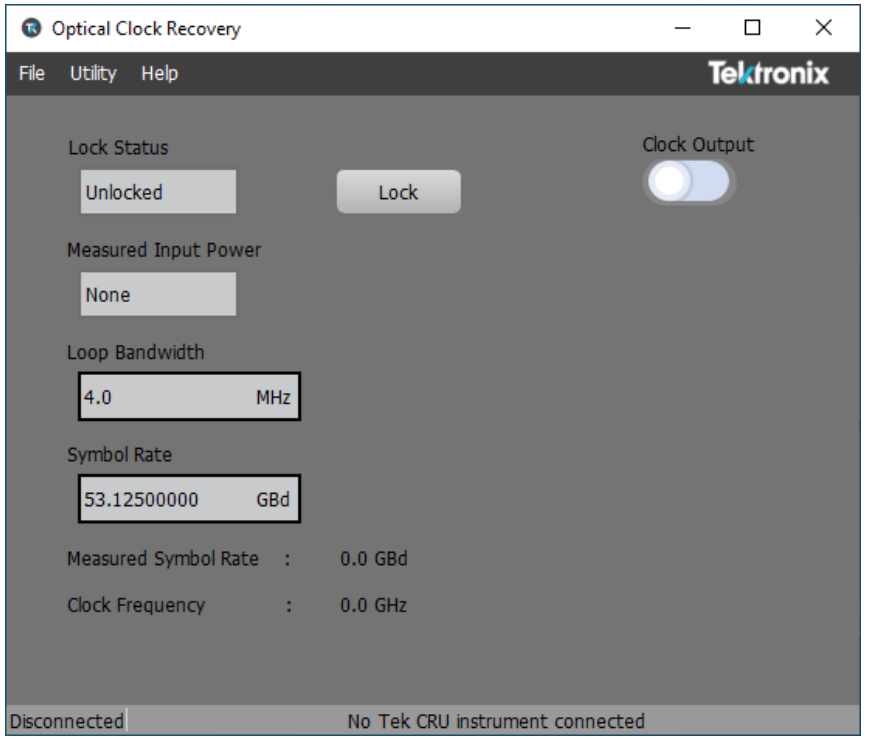
Topology

- Example
  - In fact TCR801 could work with any other instruments needing CDR such as scopes or ED of a BERT



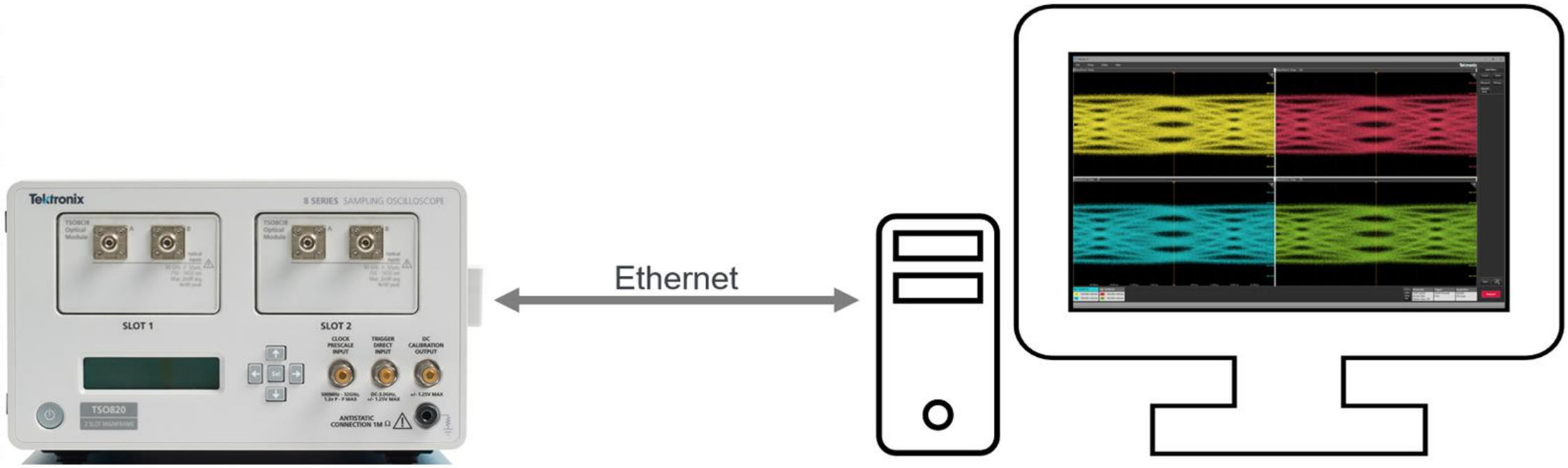
TCR801 is awesome for R&D and MFG

- Performance of CR
  - Corelating with N1078A with no problem. Sometimes TCR801 better sometimes N1078A better, all slightly.
- Lock Speed
  - As fast as 5 seconds, average 6 seconds
  - Relock as fast as 1 second
- Easy to use
  - PC Client: ready
  - PI : ready
  - Button on front panel: ready
  - Parameters setting : only two numbers need to input!



TSO820

- example


Tektronix
8 SERIES SAMPLING OSCILLOSCOPE
SLOT 1
SLOT 2
CLOCK PRESCALE INPUT
TRIGGER DIRECT INPUT
DC CALIBRATION OUTPUT
TSO820
ANTISTATIC CONNECTION 1M Ω
Ethernet


LIFT TO REMOVE


Tektronix
SLOT 1
SLOT 2

Configuration Comparison

DSA8300	8 Series	PRODUCT FEATURES
DSA8300	TSO820	Mainframe
ADVTRG	✓	Pattern Sync
80C17/18	TSO8C17/18	1/2 channel sampling module for 26/53GBd Optical Test
Opt. IMP	✓	Impulse response for bandwidth enhancement
Opt. CRTP	Not available	Clock recovery trigger pick-off option for MM application
82A04B	Not available	Phase Reference Module
DSA8300 TekScope	TSOVu	Base oscilloscope software
80SJNB	Not yet available	R&D capabilities for optical test
400G-M4	Opt. PAM4-O	Option PAM4-O – manufacturing test

✓ Included in base unit