



直播大讲堂—MIPI/LVDS物理层测试解决方案

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泰克直播大讲堂系列?

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精彩直播, 等您解锁!

主题	时间
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Agenda

1) MIPI D-PHY

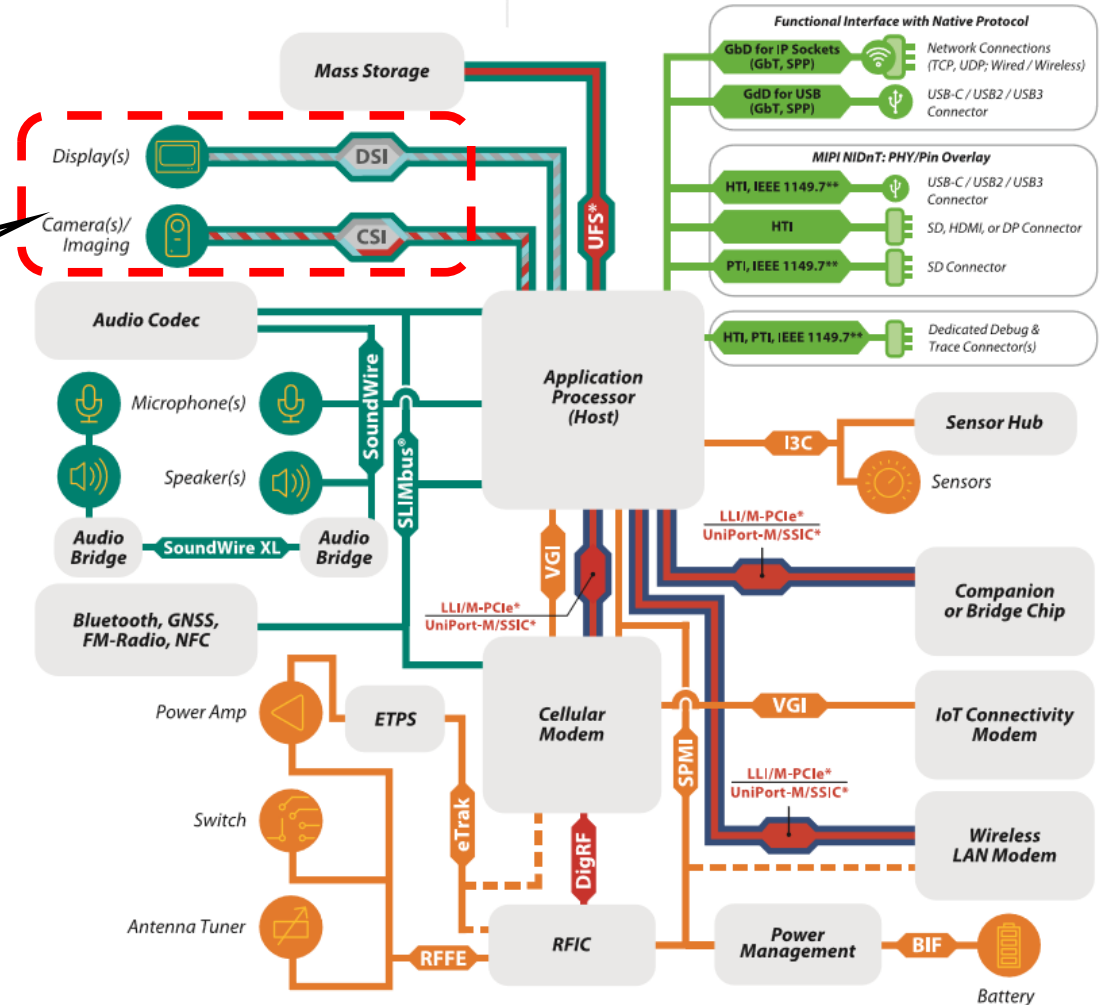
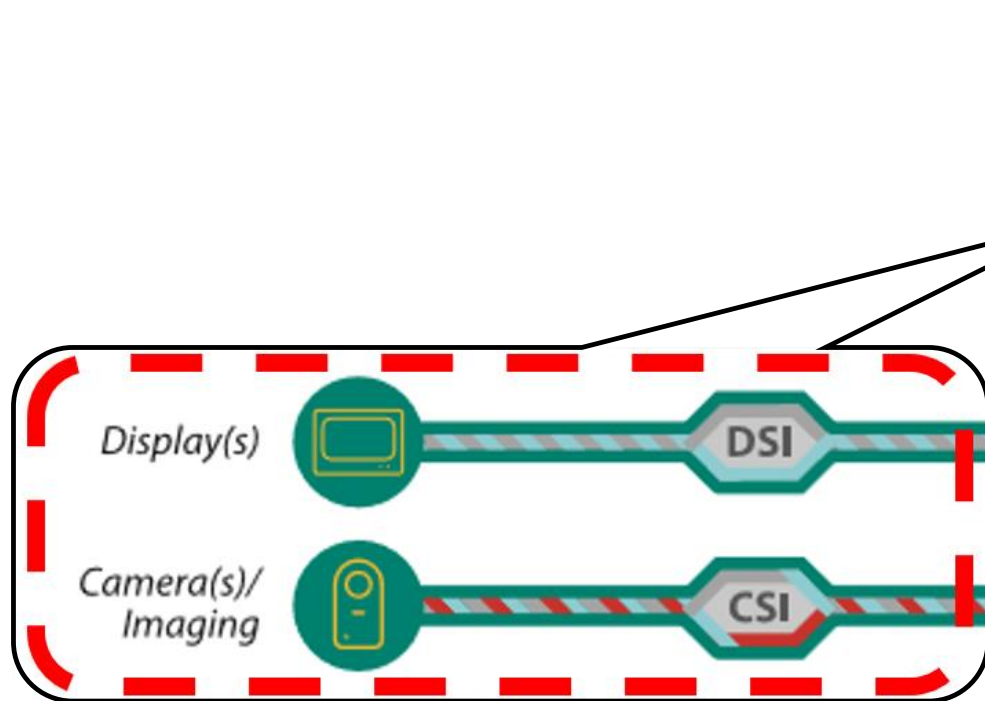
- MIPI D-PHY 基础
- D-PHY信号探测
- 自动化解决方案

2) LVDS

- LVDS 基础
- 测试挑战
- 定制化测试方案

MIPI D-PHY

mipi alliance Mobile System Diagram



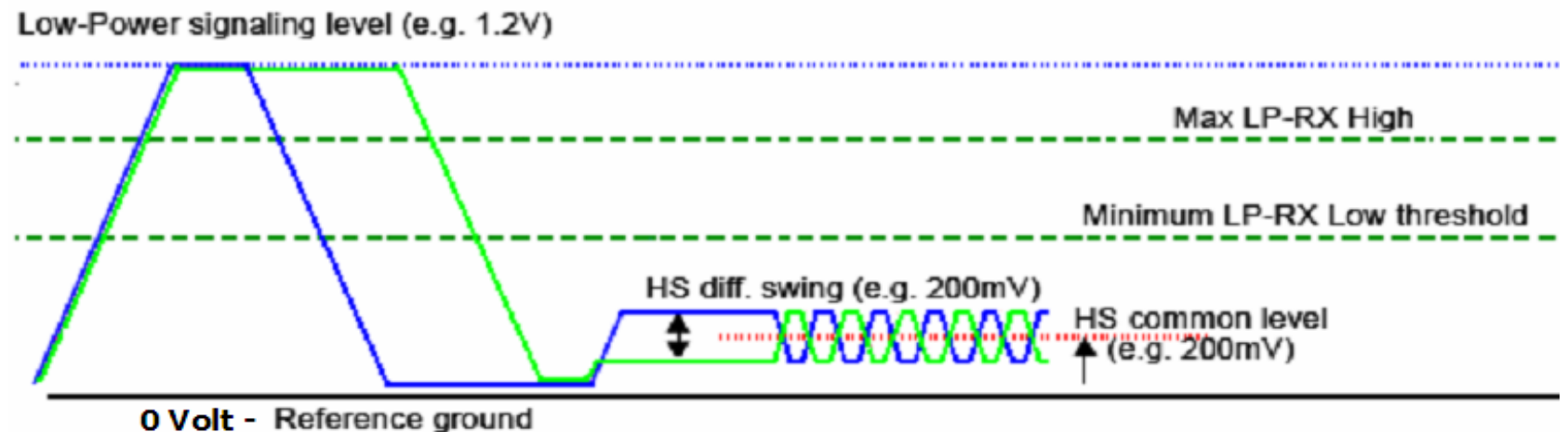
Source: MIPI Alliance

MIPI D-PHY 介绍

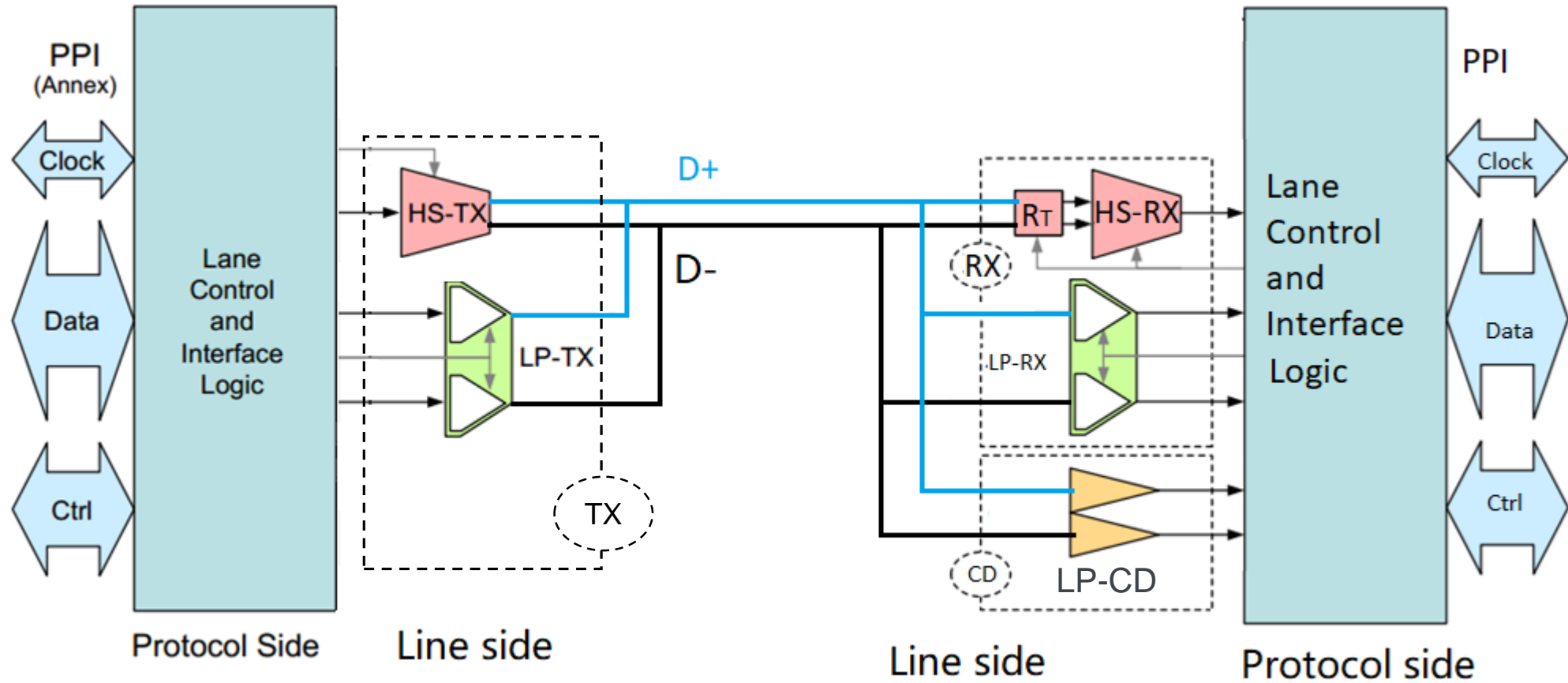
Characteristic	D-PHY
HS clocking method	DDR Source-Sync Clock
Data rate per lane (HS)	80Mbps to 4.5Gbps V1.1: 1.5 Gbps V1.2: 2.5 Gbps V2.0: 4.5 Gbps V2.5: 4.5 Gbps(STD. channel) 6.0 Gbps(Short channel)
Data rate per lane (LS)	< 10 Mbps
Minimum configuration pins	1 Clock Lane + 1 Data Lane 4 pins
Conventional pins per Port (3 or 4 lanes)	10 pins (1 clock Lane + 4 Data lanes)

What is D-PHY ?

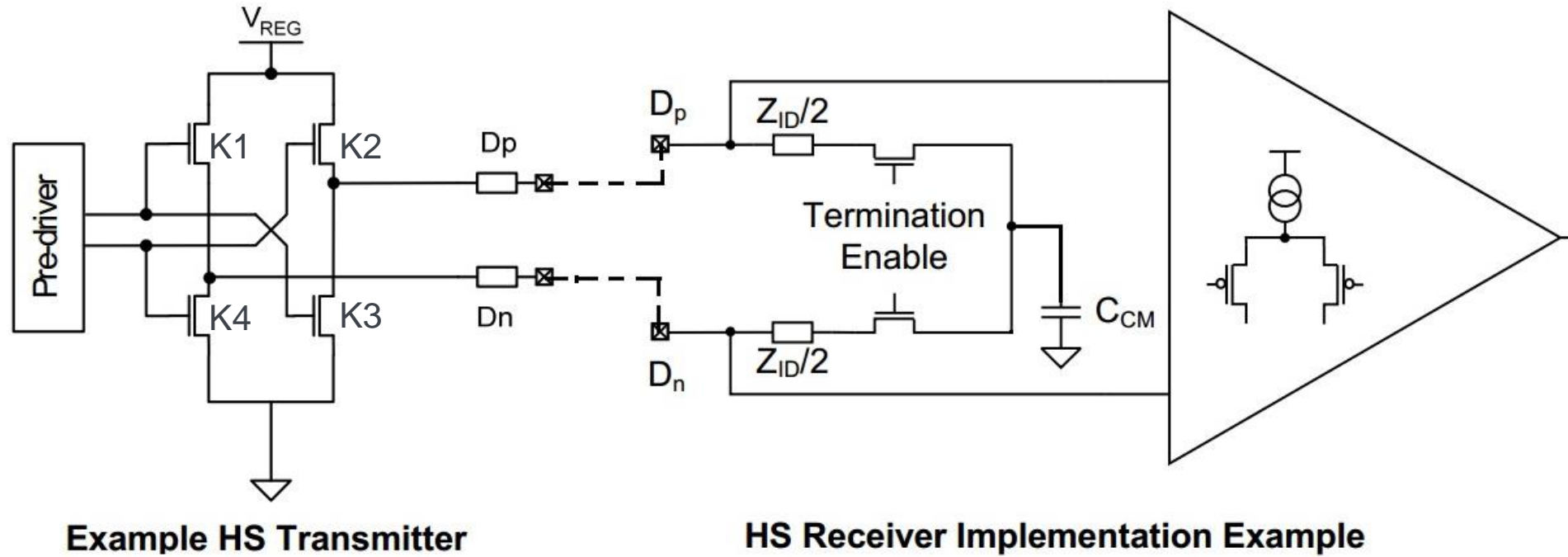
- It's a PHY standard for interfacing Camera (CSI) & Display (DSI)
- Two modes of transmission
 - High Speed (HS) and Low Power (LP)
- Modes are mixed during the operation
 - Transitions from LP to HS and back to LP on the fly
- Maximum Data Rate
 - High Speed mode: 80 Mbps – 4.5 Gbps
 - Low Power mode: Up to 10 Mbps
- Bus termination
 - 50 ohms in HS single end
 - Hi-Z in LP



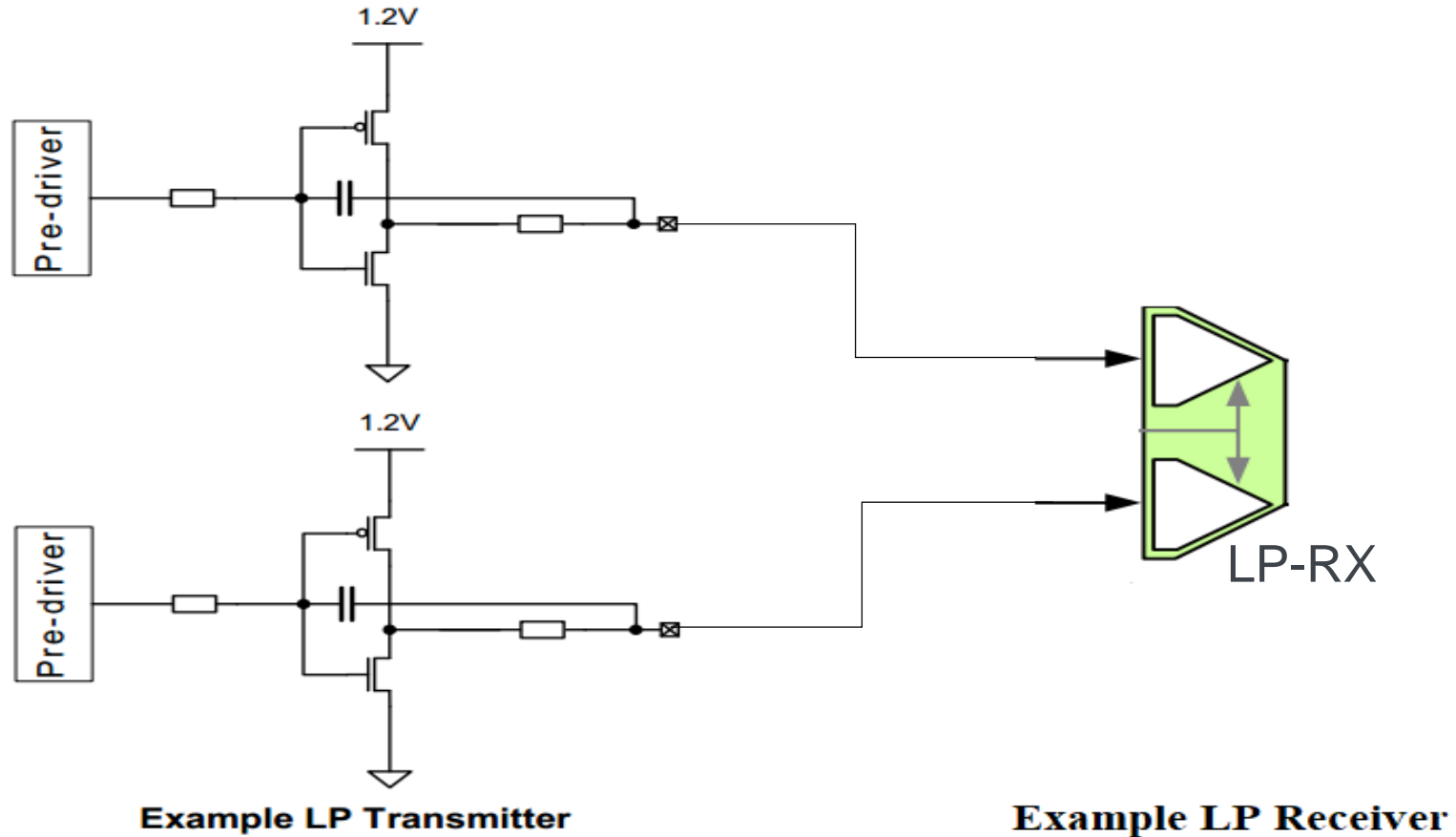
D-PHY Lane Module Functions



D-PHY HS TX/RX Implementation

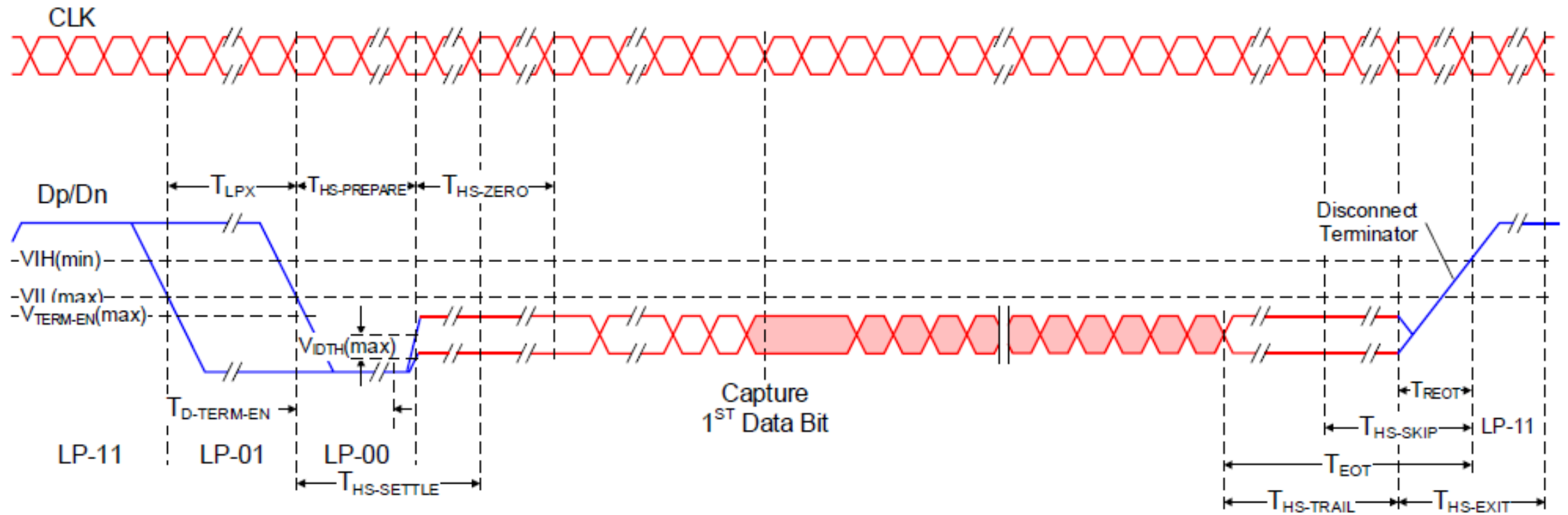


D-PHY LP TX/RX Implementation



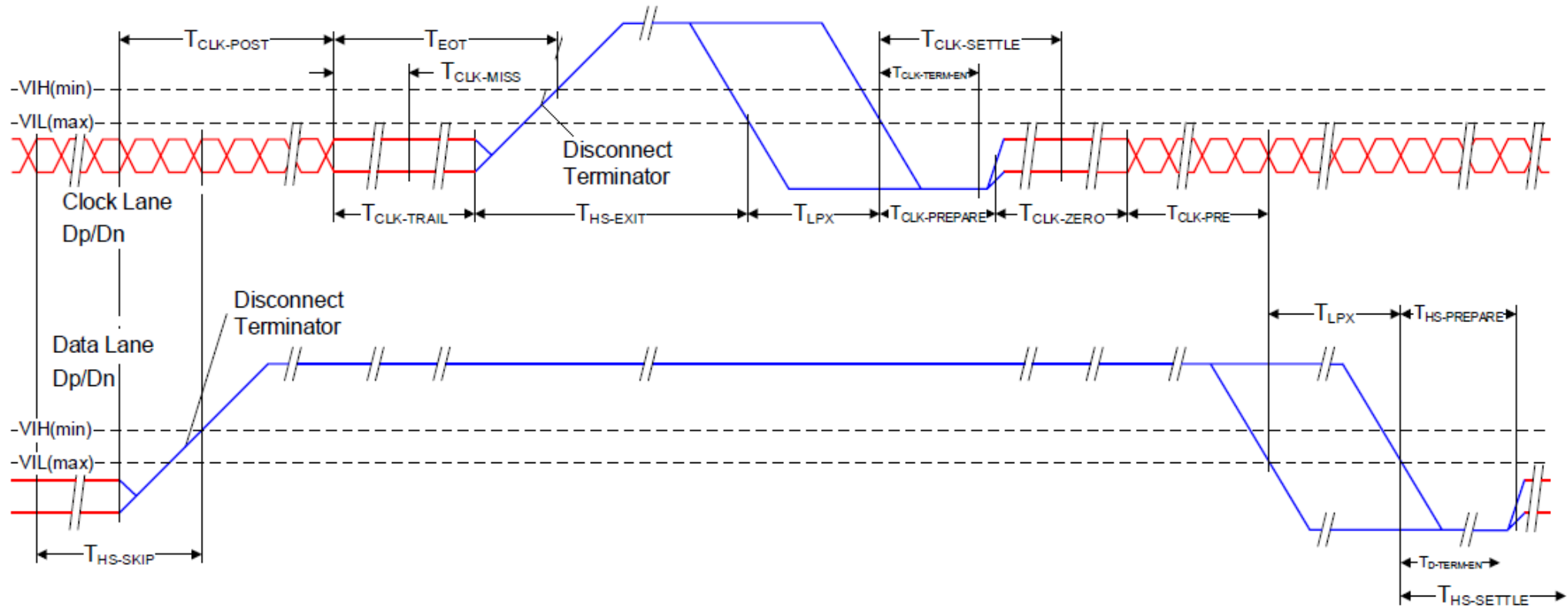
D-PHY HS Data transmission

Clock Continue Mode

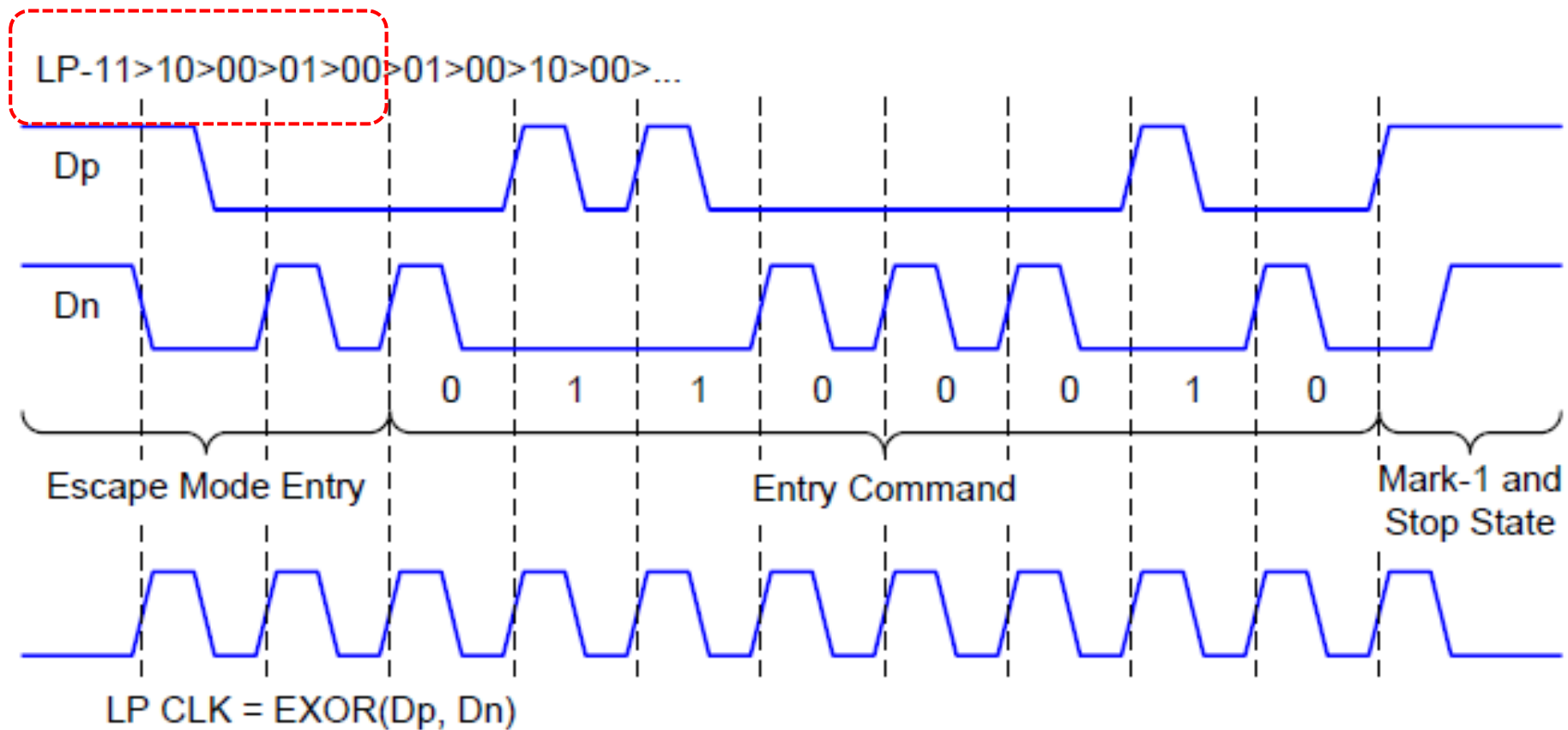


D-PHY HS Data transmission

Clock Normal Mode



Escape mode

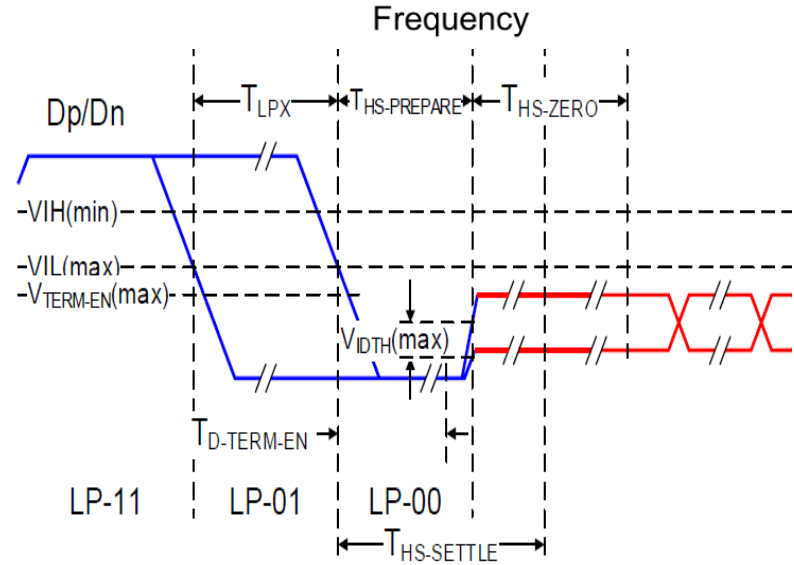
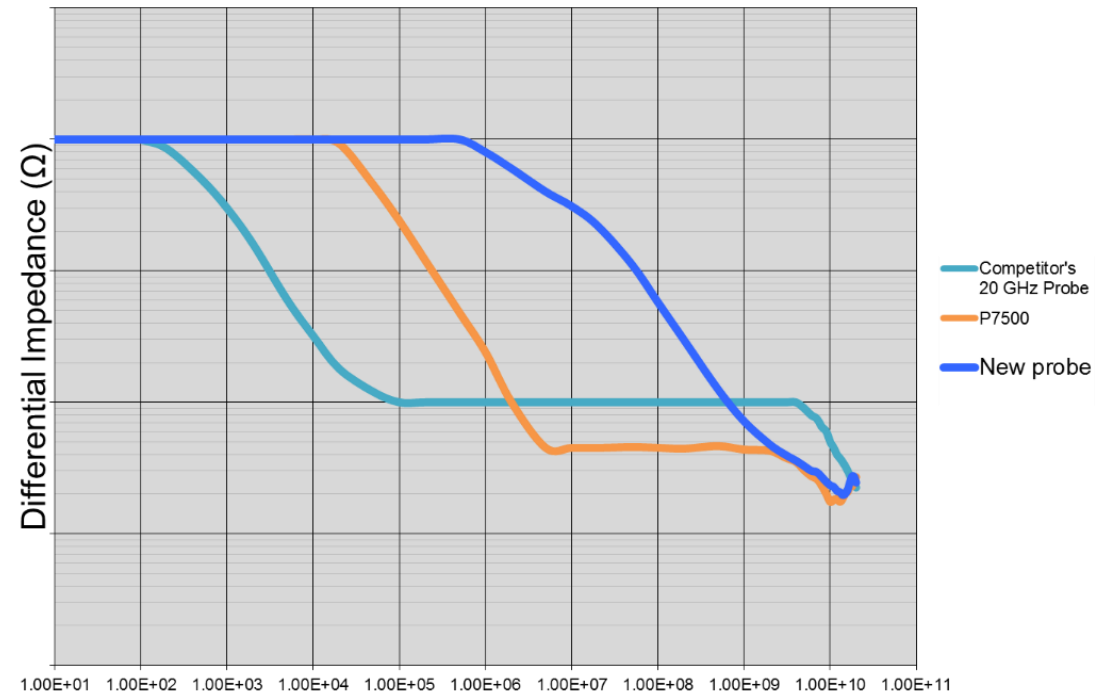
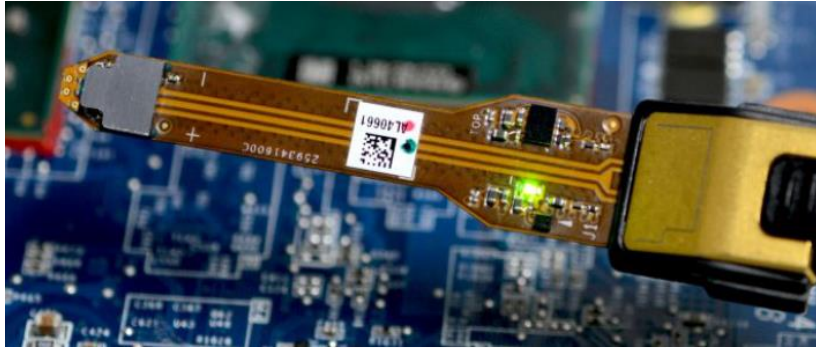


Escape mode Entry procedure (LP-11, LP-10, LP-00, LP-01, LP-00)

测试挑战

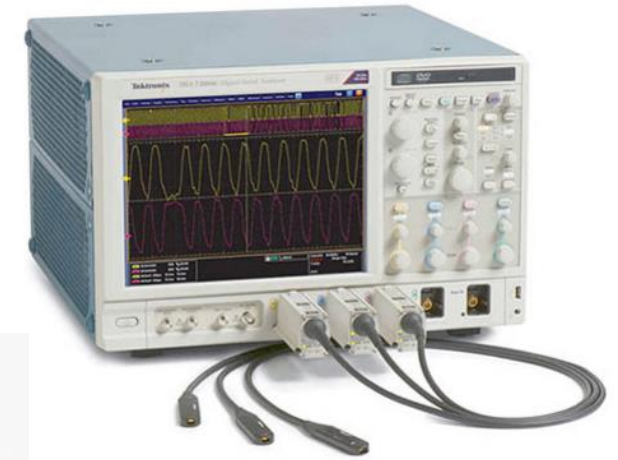
- 58+测试项目
- 自动检测跳变沿, 测量项目依据跳变沿进行
- 最小化探头的负载效应, HS 端接, LP模式高阻
- 板子密度越来越高, 测试点难以直接接触及
- 自动测试设置, 适应HS/LP

Better Probing

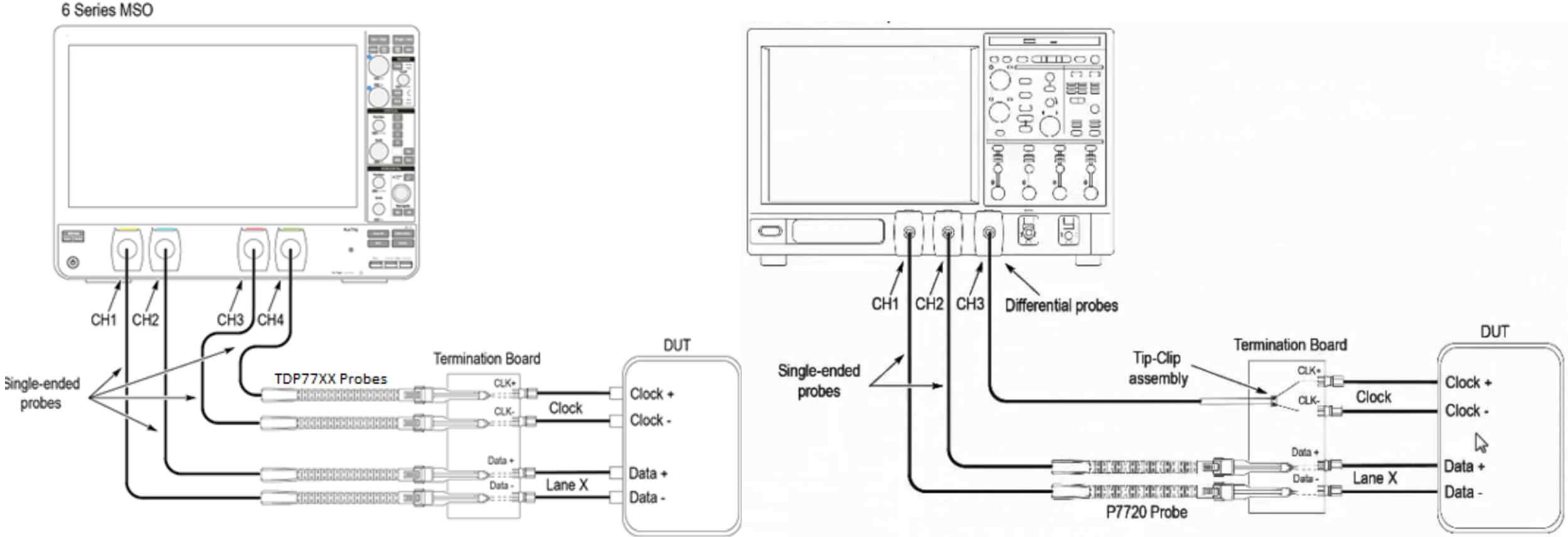


D-PHY Tx Test Solution

- Oscilloscope & Probes
 - 6 Series MSO-4GHz and above /DPO70000C/DX/SX series
 - TDP7708Probe /P77XX
- Conformance software
 - D-PHY Tx: CTS1.2*
- Debug
 - Pre-Recorded waveform analysis
- MIPI D-PHY Termination Board
 - Dynamic termination based on mode

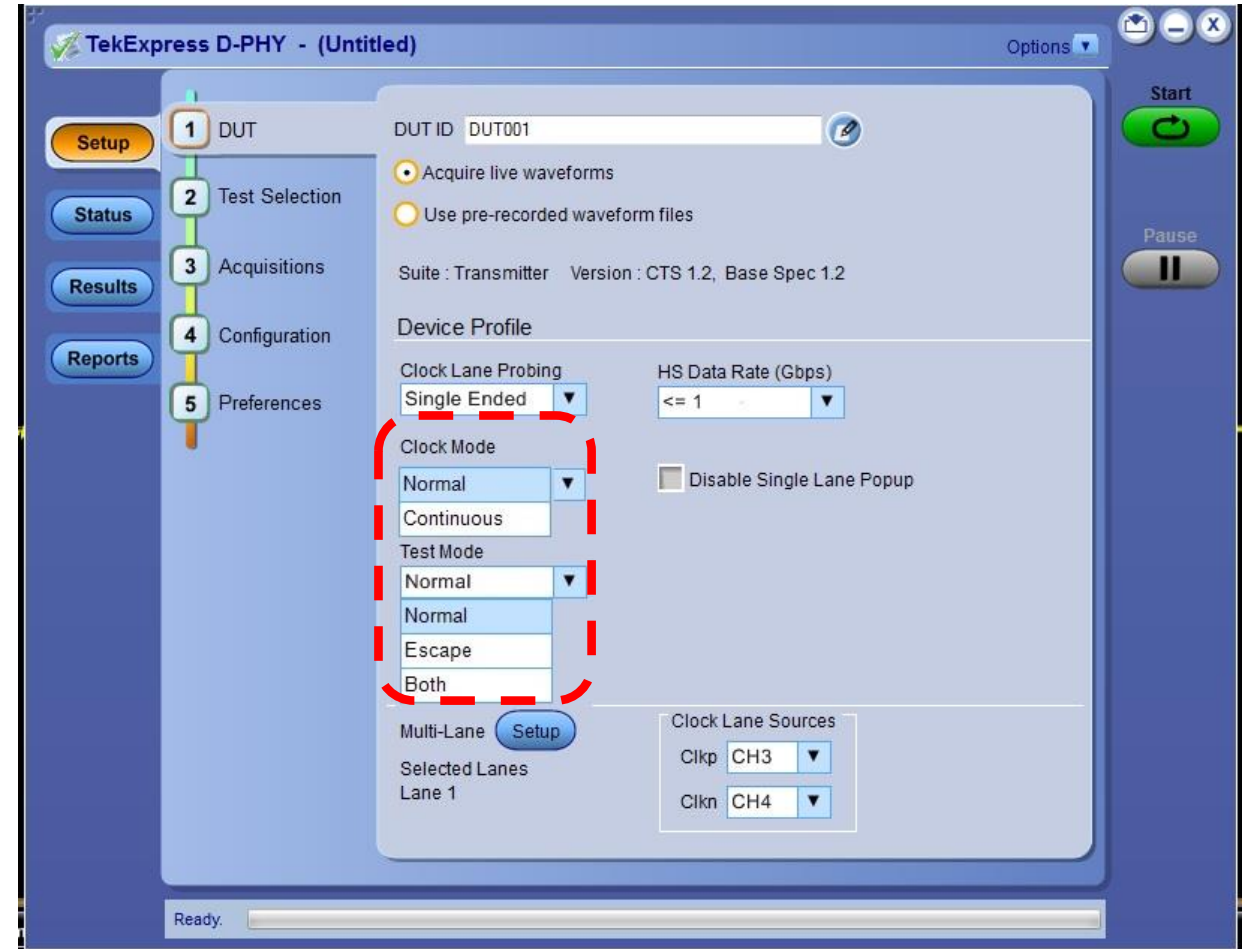


Probe Connection



Tx Testing: Solutions

- 100% Support for all the tests as per CTS 1.2
- Probes and probe tips to accurately make measurements.
- Automated test solutions with scripting capability and reduced test execution times ~20* mins
- Ability to terminate signals appropriately and measure the dynamic Switching between LP & HS
- No two MIPI devices are the same
 - Variable Data Rates
 - Up to 4 lanes of Data traffic



Test Group and Configuration

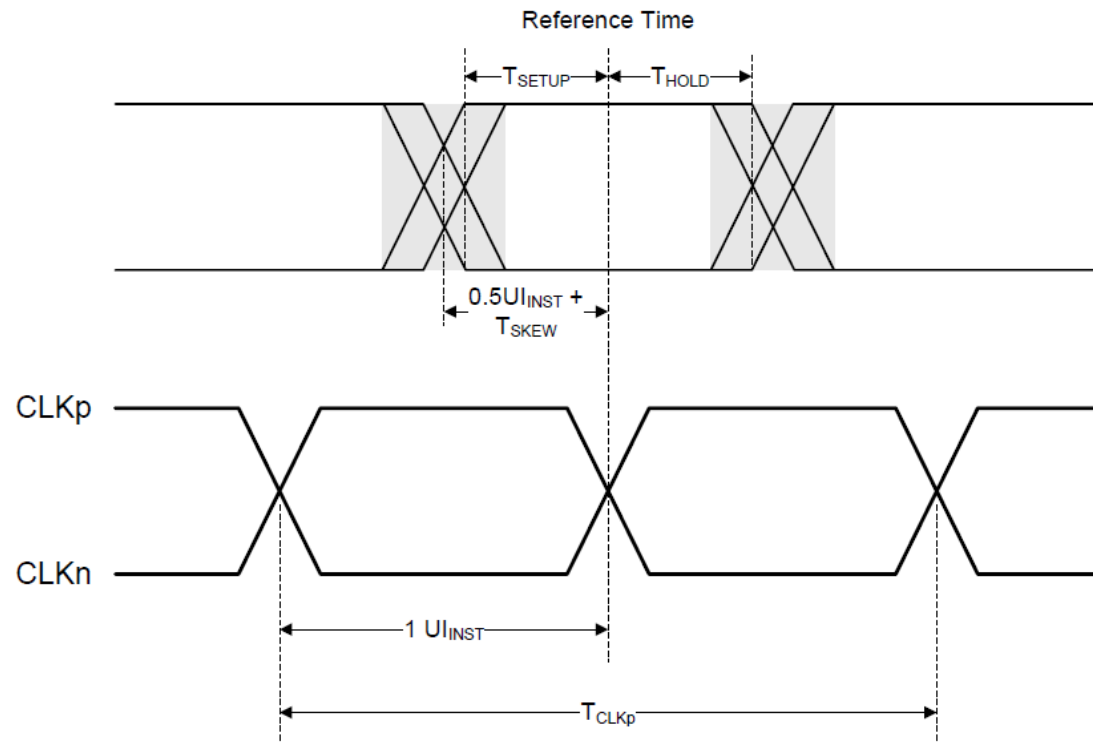
Escape mode LP signal: Group 1/2/6; HS signal: Group 3/4/5

The screenshot shows the TekExpress D-PHY software interface. The left sidebar has a vertical navigation menu with steps 1-5: 1. DUT, 2. Test Selection, 3. Acquisitions, 4. Configuration, 5. Preferences. Step 2 is highlighted. The main window displays 'D-PHY : Transmitter : CTS 1.2 Base Spec 1.2'. Below this, there are 'Deselect All' and 'Select All' buttons. A tree view shows 'Group 1' selected, containing seven test items: 1.1.1 Data Lane LP-TX Thevenin Output High Level Voltage (VOH), 1.1.2 Data Lane LP-TX Thevenin Output Low Level Voltage (VOL), 1.1.3 Data Lane LP-TX 15%-85% Rise Time (TRLP), 1.1.4 Data Lane LP-TX 15%-85% Fall Time (TFPL), 1.1.5 Data Lane LP-TX Slew Rate vs. CLOAD, 1.1.6 Data Lane LP-TX Pulse Width of Exclusive-OR Clock (TLP-PU), and 1.1.7 Data Lane LP-TX Period of Exclusive-OR Clock (TLP-PER-TX). Below the tree is a 'Test Description' box with text: 'This group of tests (Escape Mode) verifies various requirements specific to Data Lane LP signaling. The intent of the structure of this Group is to facilitate performing a set of related LP-TX measurements on a single Data Lane'. A 'Schematic' button is also present. The status bar at the bottom says 'Ready.'.

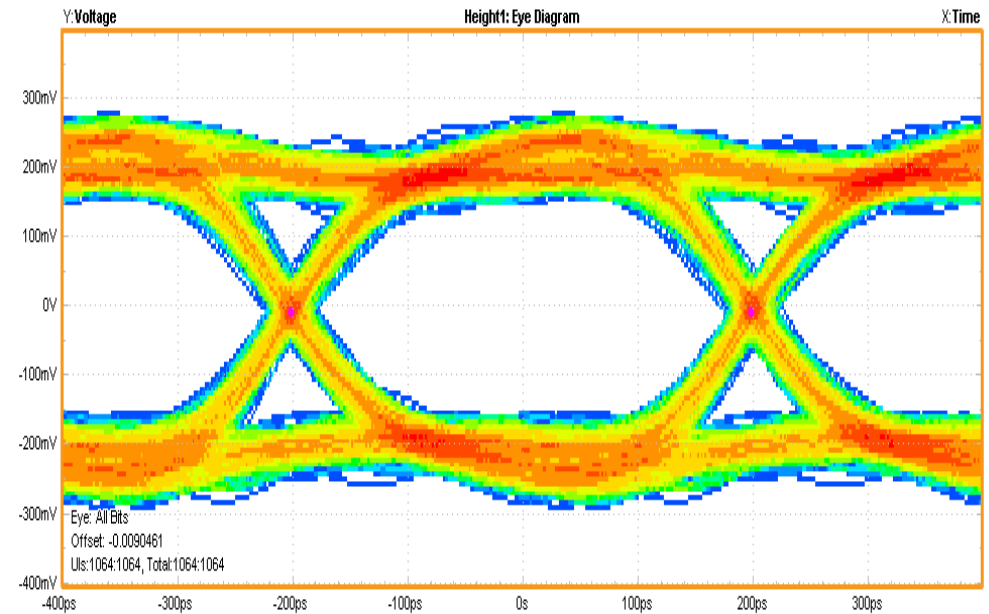
The screenshot shows the TekExpress D-PHY software interface with the 'Measurements' tab selected. The left sidebar is the same as in the first screenshot. The main window shows 'Compliance Mode' selected. Below this, there are 'Global Settings' and 'Measurements' tabs. The 'Measurements' tab contains a list of acquisition settings: Data Lanes Acquisition In Escape Mode with Data As Trigger, Clock Lanes Acquisition In Escape Mode with Clock As Trigger, Data and Clock Lanes Acquisition with Data As Trigger, Clock Lanes Acquisition with Clock As Trigger, Data and Clock Lanes Acquisition In Escape Mode with Data As Trigger6_1, Clock Lanes Acquisition In Escape Mode with Clock As Trigger, Data and Clock Lanes Acquisition in Escape Mode with Data As Trigger6_3, and Data and Clock Lanes Acquisition in Escape Mode with Data As Trigger6_4to6. Below this list is a 'Trigger Settings' section with a 'Trigger Type' dropdown set to 'Transition'. The 'Trigger Settings' section includes: Source (Dp), Slope (Positive), Transition (Greater Than), Delta Time (ps) (500), and Qualify (Occurs). On the right side of the 'Trigger Settings' section, there are input fields for 'Lower Level (V)' (0.05) and 'Upper Level (V)' (1). The status bar at the bottom says 'Ready.'.

Test ID 1.5.4 Data to clock Skew – Eye Diagram

6-DJA mandatory for Eye Diagram plot



Test ID 1.5.4 $T_{SKEW(TX)}$



Eye Diagram of Test ID 1.5.4 $T_{SKEW(TX)}$

Agenda

1) MIPI D-PHY

- MIPI D-PHY 基础
- 更好的探测方案
- 自动化测试方案

2) LVDS

- LVDS 基础
- 测试挑战
- 定制化测试方案

What's LVDS

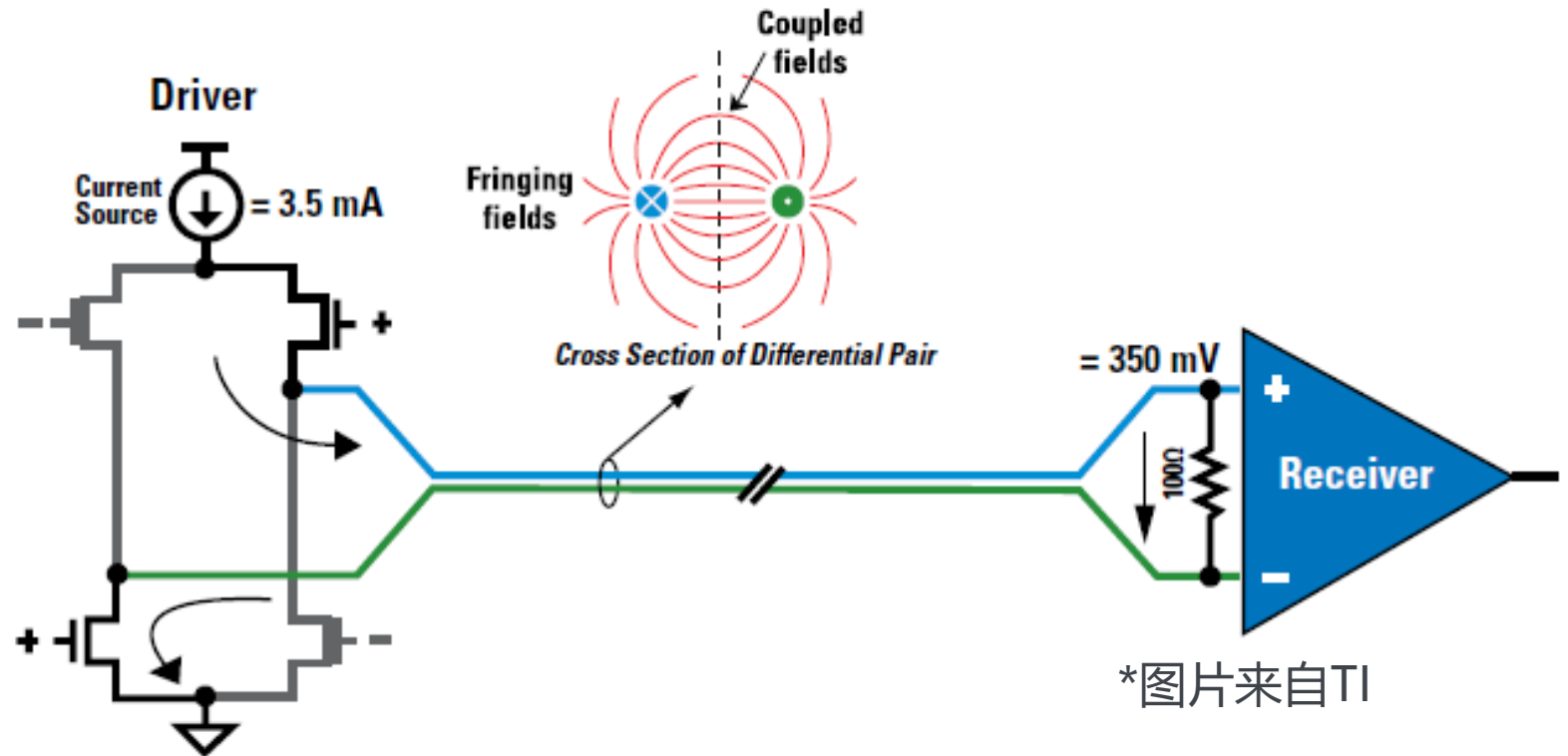
LVDS: Low-Voltage Differential Signaling

Standards :

ANSI/TIA/EIA-644 (LVDS)

IEEE 1596.3 SCI-LVDS

- 低功耗
- 低噪声
- 抗干扰能力强
- 可扩展
- 应用广泛

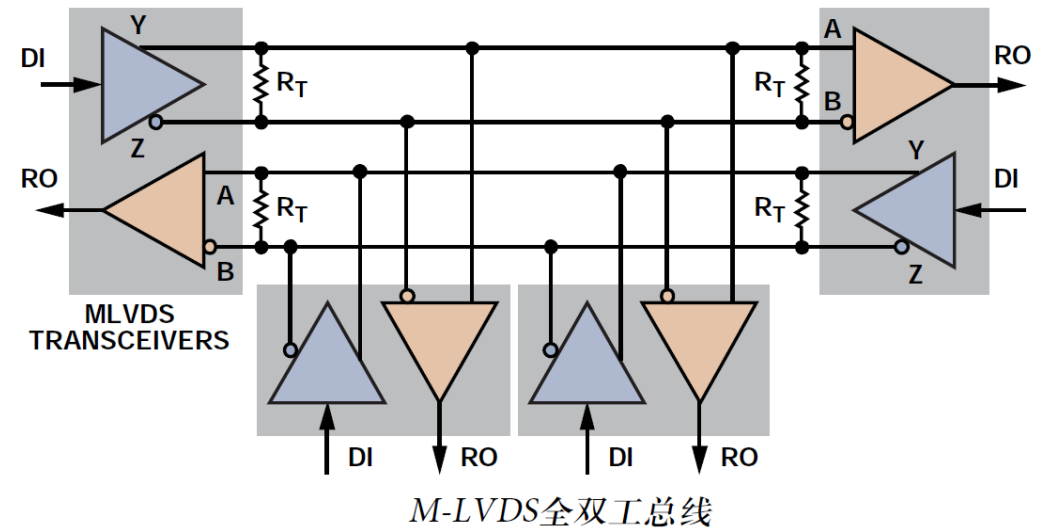
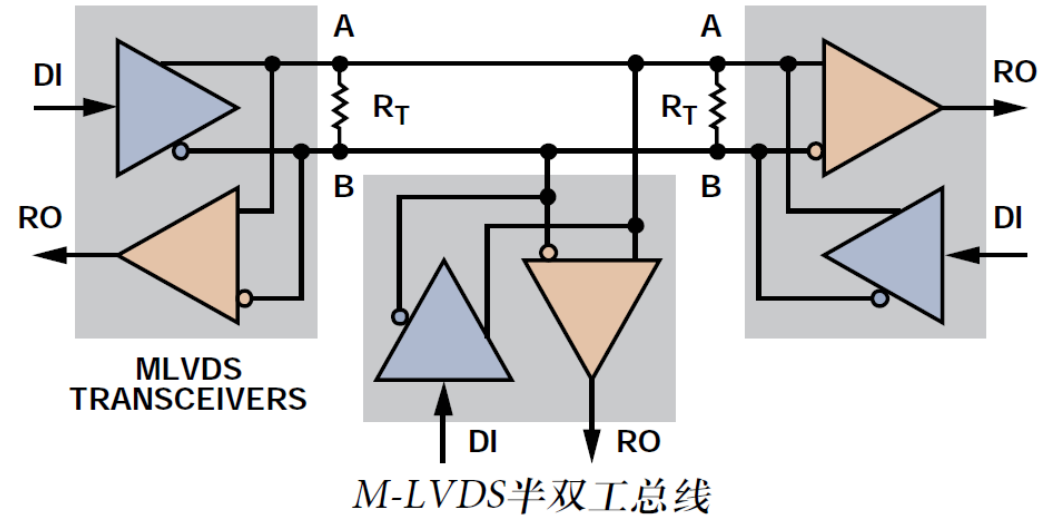
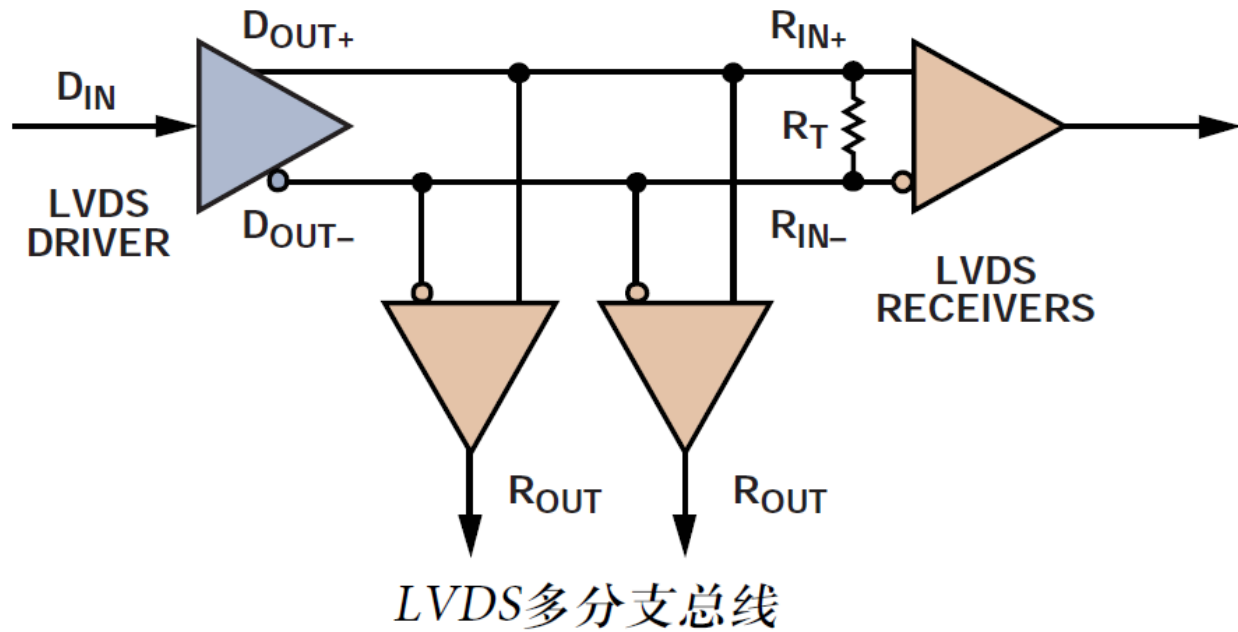


LVDS Types

Bus Config	LVDS	Bus-LVDS	M-LVDS	Mini LVDS
Point to Point	Yes	Yes	--	Yes
Multi drop	Yes	Yes	Yes	
Multi point		Yes	Yes	
Application	≤ 2Gbps 5m-10m	≤ 500 Mbps 20m-40m	≤ 500 Mbps	

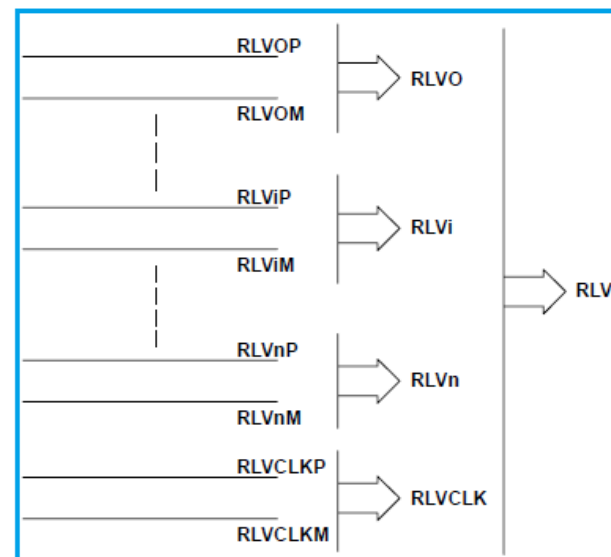
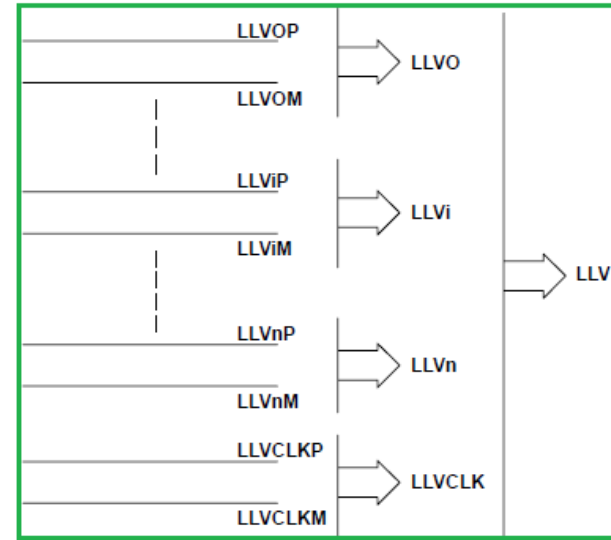
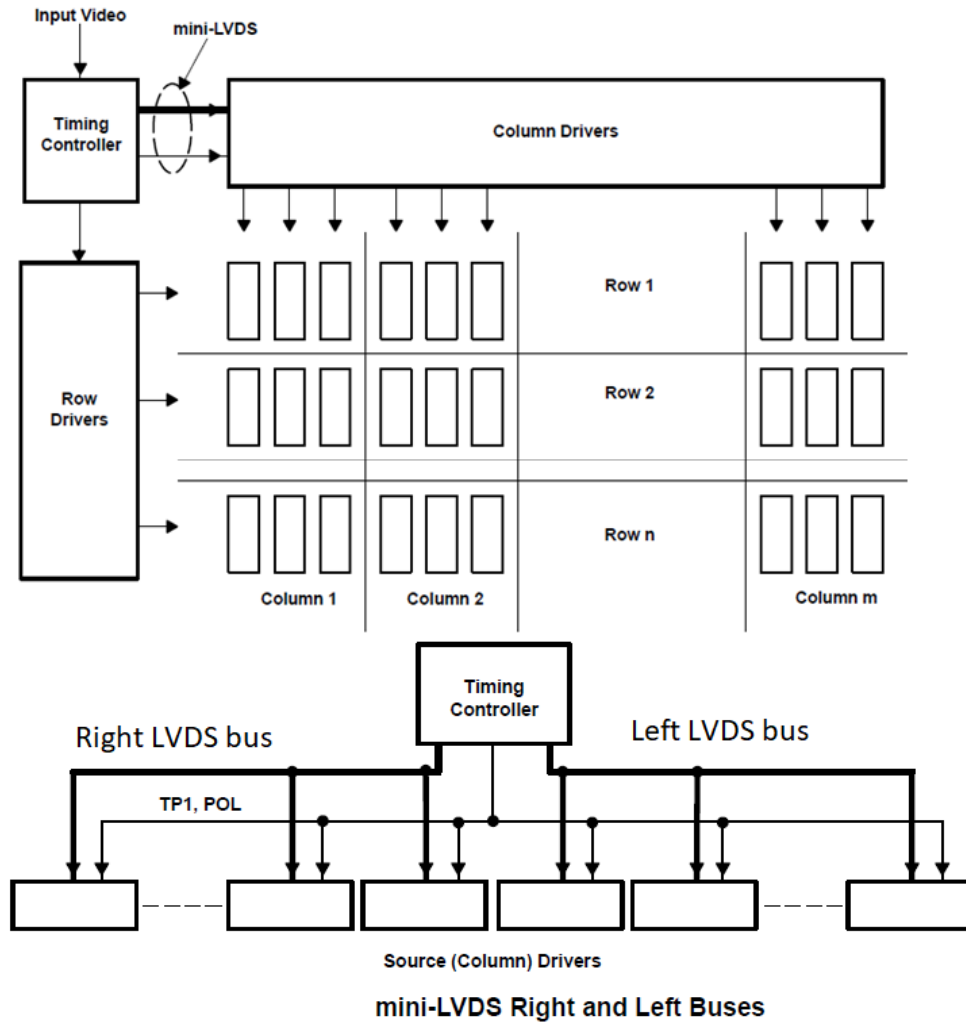
- ANSI/TIA/EIA-899 M-LVDS Standard
- IEEE 1596.3-1995 LVDS for SCI Standard
- JEDEC GLVDS Specification, Rev 1.0
- JEDEC SLVS (JESD8-13) October 2001

M-LVDS



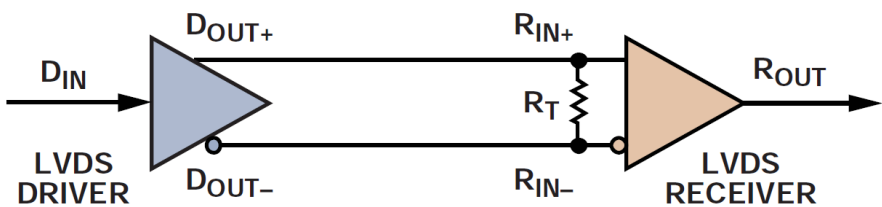
*图片来自ADI

Mini-LVDS



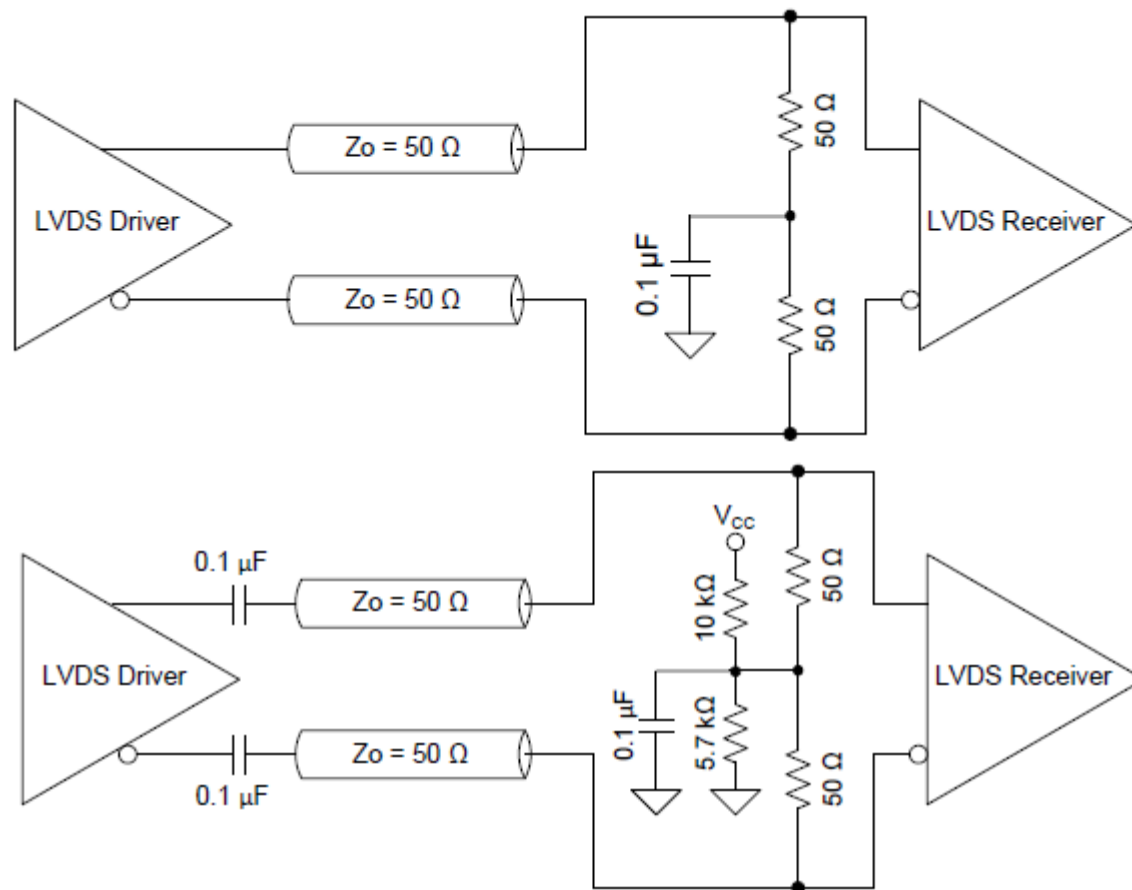
1 CLK Lane
3/4/5/6 data lane

耦合和端接方式



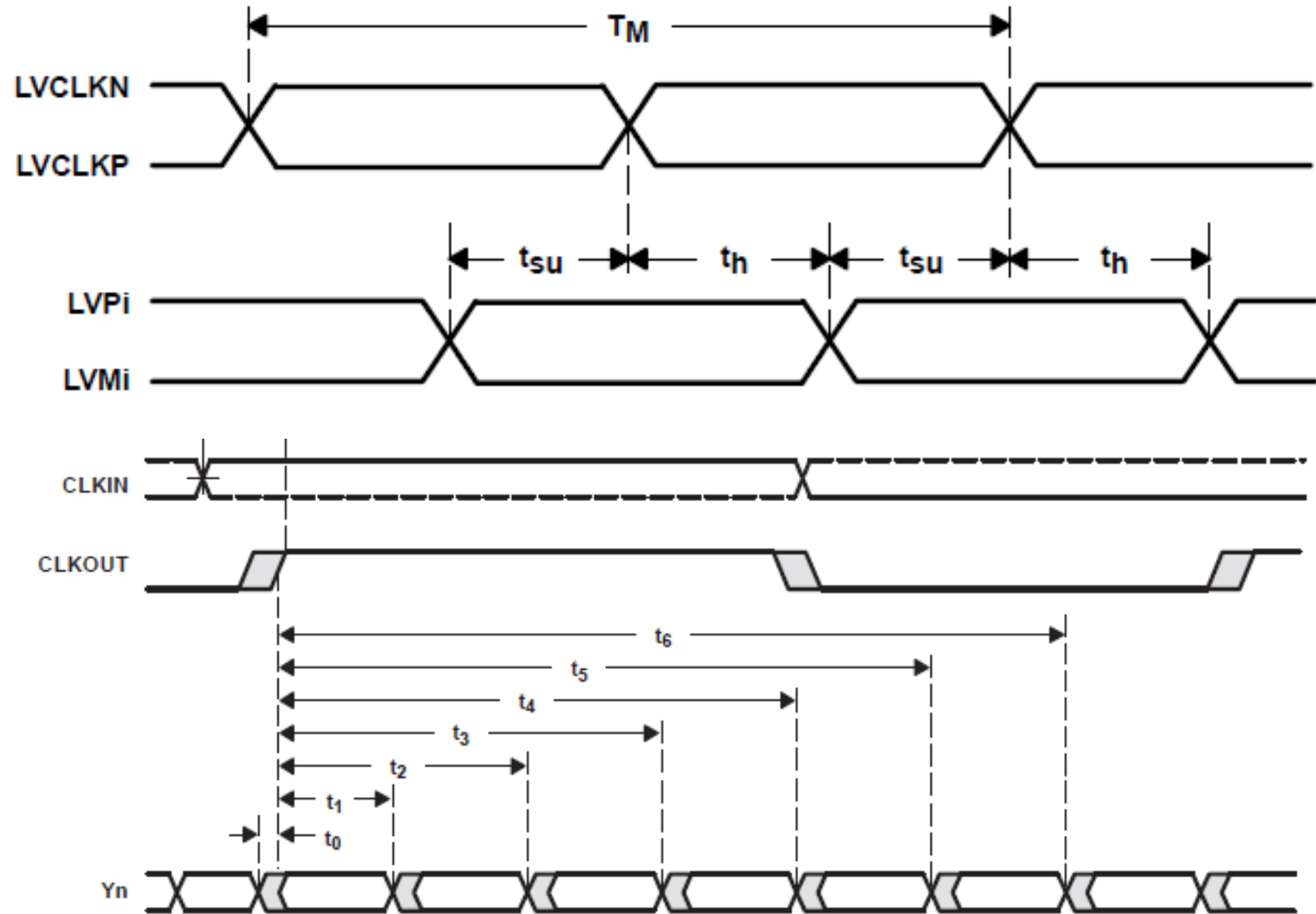
LVDS点到点链路

- Filter common-mode noise
- Transmission line skew
- Change DC bias voltage
- Protect Driver from getting shorted
- Prevent DC currents flowing
- DC balanced signal



Clock VS Data

Clock : Data = 1:2



• Clock : Data = 1:7

Test Challenge

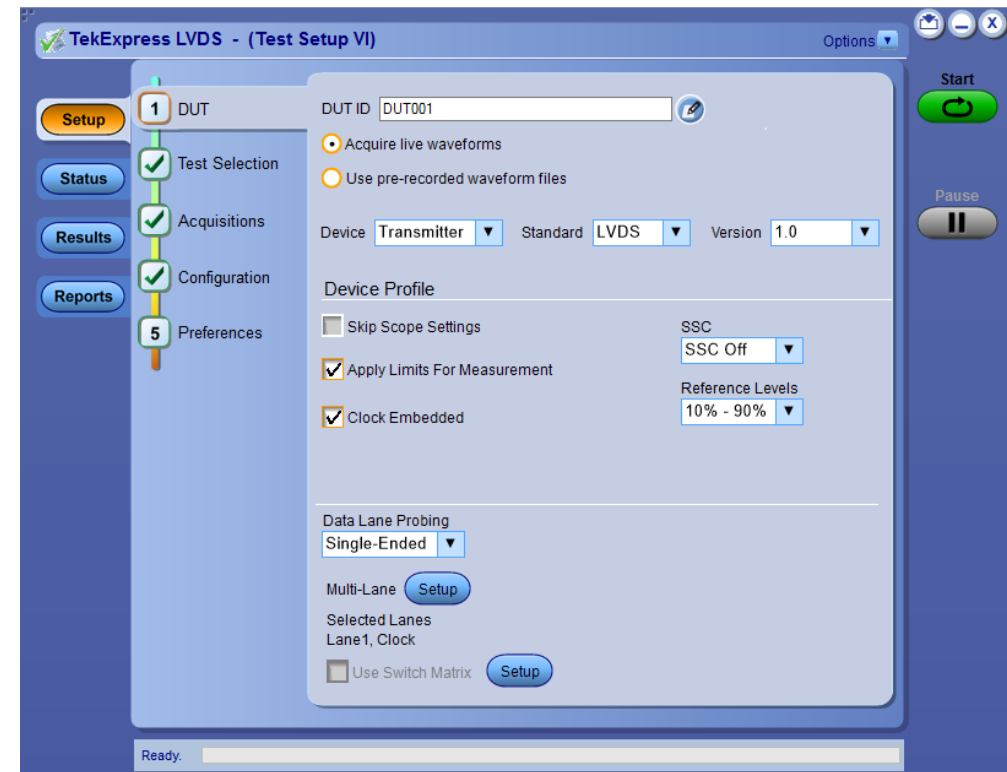
- 更好探测方式
- LVDS种类多
- 时钟恢复方式多

Measurement number	List of measurements			
	Measurement	LVDS Legacy	mini LVDS	
1	Clock (SS Off)	Frequency	Yes	Yes
2		Period	Yes	Yes
3		Duty Cycle	Yes	Yes
4		TIE	Yes	Yes
5		TJ@BER	Yes	Yes
6		DJ	Yes	Yes
7		RJ	Yes	Yes
8	Clock (SS ON)	Profile	Yes	Yes
9		Mod Rate	Yes	Yes
10		Freq Dev	Yes	Yes
11		Freq Dev Min	Yes	Yes
12		Freq Dev Max	Yes	Yes
13	Data	AC Timing / Eye Diagram	Yes	
14		TIE	Yes	Yes
15		Data Width	Yes	Yes
16		Clock-Data Setup Time		Yes
17		Clock-Data Hold Time		Yes
18		Rise Time	Yes	Yes
19		Fall Time	Yes	Yes
20		Intra Skew		
21		Vpp / Output Voltage		
22		T/nT / De Emphasis		
23		UI (with Filter)		
24		TJ@BER	Yes	Yes
25		DJ	Yes	Yes
26		RJ	Yes	Yes
27		DDJ		
28	TJ			

TekExpress LVDS

SOLUTION OVERVIEW - TEKEXPRESS LVDS TX

- Fully Automated Tx Solutions
- Works on MSO/DPO70K and MSO5/6
- Supports measurement from Multiple LVDS Standards
- Configurable Test, Test settings and Test limits
- Automatic MASK – Data Rate and MSV
- Generic Clock Recovery configuration
- Reference level and filter file selection.



TekExpress LVDS

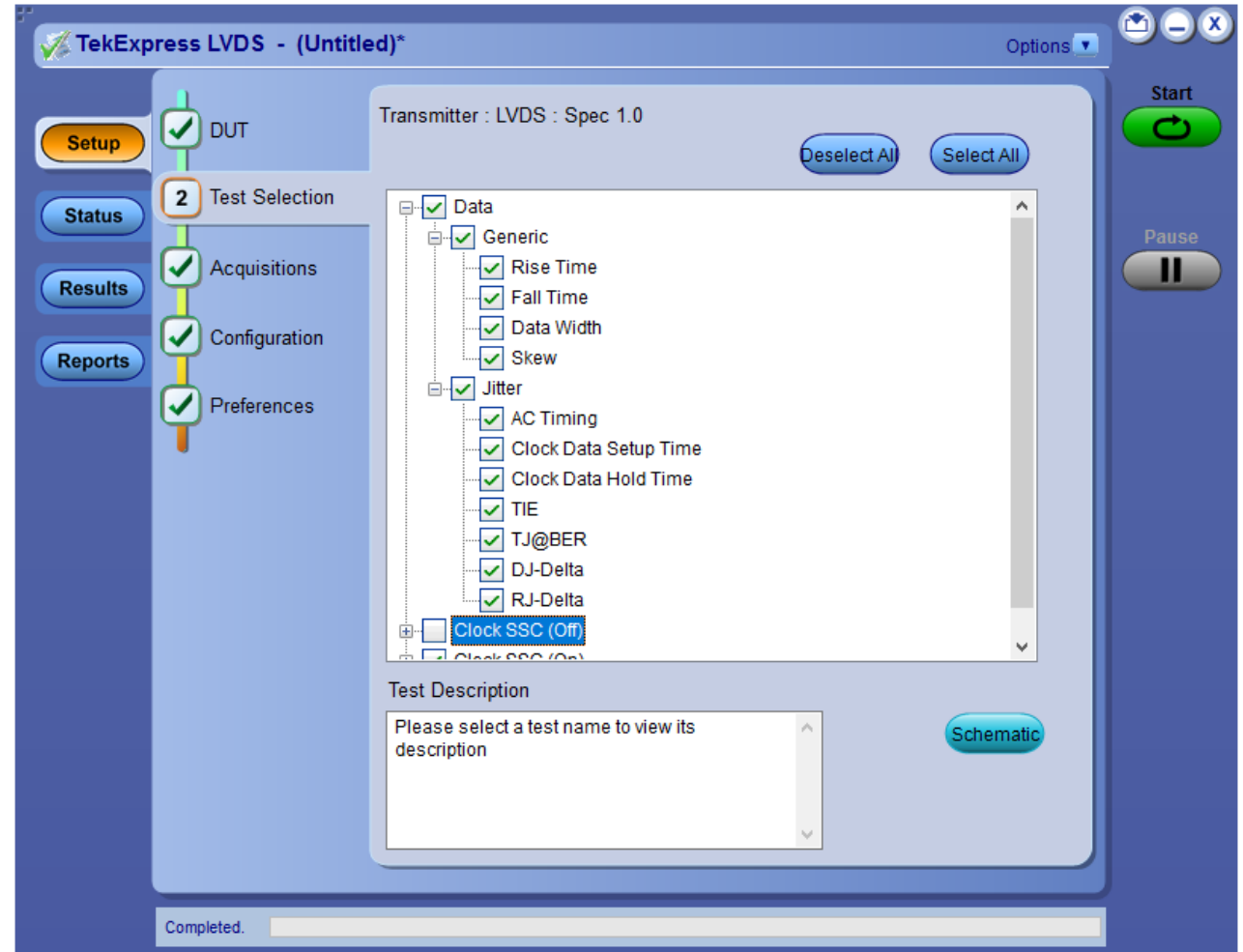
MEASUREMENT SUPPORTED – ON DATA

Generic

- Rise Time
- Fall Time
- Data Width
- Skew (Inter and Intra)

Jitter

- AC Timing/Eye diagram
- Clock Data Setup Time
- Clock Data Hold Time
- Time Interval Error (TIE)
- TJ@BER
- DJ Delta and RJ Delta



TekExpress LVDS

MEASUREMENT SUPPORTED ON CLOCK

Generic

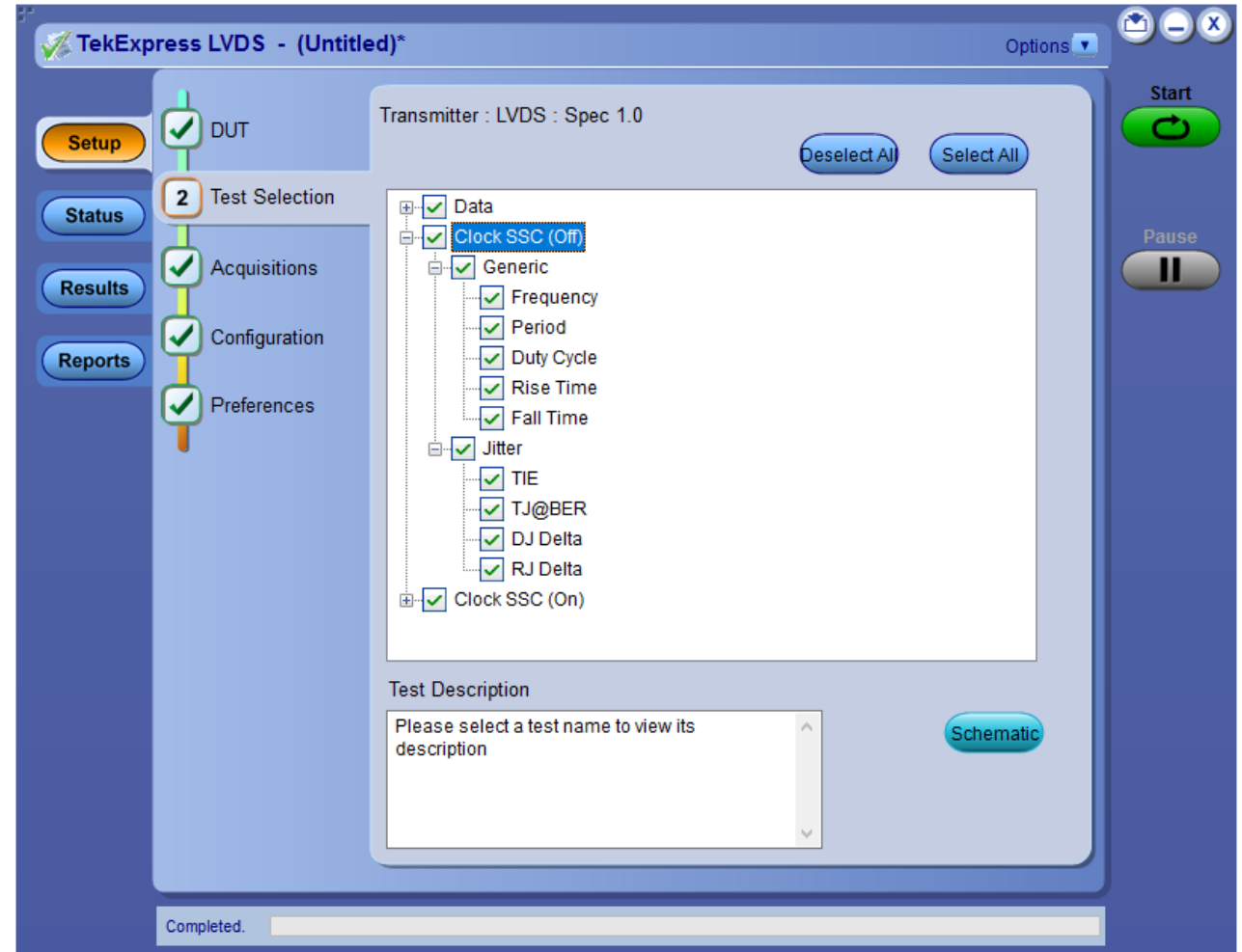
- Rise Time, Fall Time
- Frequency, Period
- Duty Cycle

Jitter

- Time Interval Error (TIE)
- TJ@BER
- DJ Delta and RJ Delta

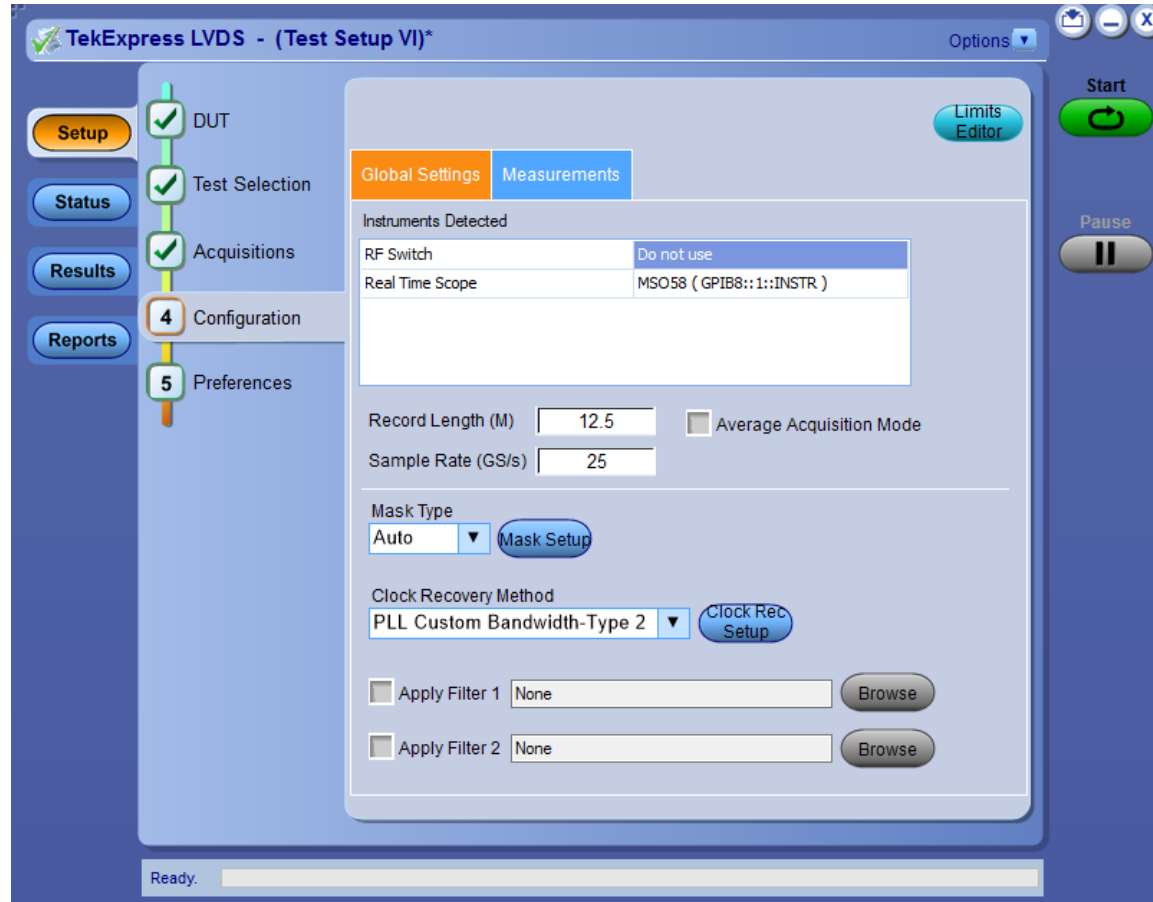
SS ON

- Mod Rate
- Profile
- Frequency Deviation – Min Max



TekExpress LVDS

SNEAK PEAK : MASK AND CDR



Built in Features:

- Auto Mask Generation
- Clock Recovery
- Filters for Standards like GVIF and GMSL2

Auto Mask, Clock recovery and Filters are key differentiators for us

TekExpress LVDS

MASK AND CDR CONTD.

Mask Segment Points

Mask Shape:

Unit Interval (s):

Max Swing Voltage (V):

Scale Factors:

	X Scale Factors	Y Scale Factors
1	<input type="text" value="0.375"/>	<input type="text" value="0"/>
2	<input type="text" value="0.425"/>	<input type="text" value="0.125"/>
3	<input type="text" value="0.625"/>	<input type="text" value="0.125"/>
4	<input type="text" value="0.85"/>	<input type="text" value="0"/>
5	<input type="text" value="0.625"/>	<input type="text" value="-0.125"/>
6	<input type="text" value="0.375"/>	<input type="text" value="-0.125"/>

Diagram labels: X1,Y1, X2,Y2, X3,Y3, X4,Y4, X5,Y5, X6,Y6. Segment 1, Segment 2, Segment 3. 0.5*VSwing, VSwing 0V, 0 UI, 1 UI.

Buttons: Generate Mask, Mask Points, Close, Default Scale Factors

Clock Recovery Setup

Clock Recovery Method:

Nominal Data Rate: Bit Rate (Gb/s):

BandWidth Type: BandWidth (MHz):

Damping Factor:

Buttons: Close

Auto Mask :Generation based on Shape, Data Rate and Voltage levels
Mask Shape Supported: Diamond, Hexagon and Octagon

LVDS RX solution

AWG5200



8 CHANNELS -- FLEXIBILITY

- **Cleanest Signal**
 - Industry's best combination of sample rate and vertical resolution
 - 16 bits of resolution
 - 10 GS/s
 - Extremely low noise floor
 - Build reliable setups with pre-calibration and pre-compensation software
- **Massively Scalable**
 - Best in class! - Up to 8 independent Channels/unit at a low cost/channel
 - Multi-unit synchronization:

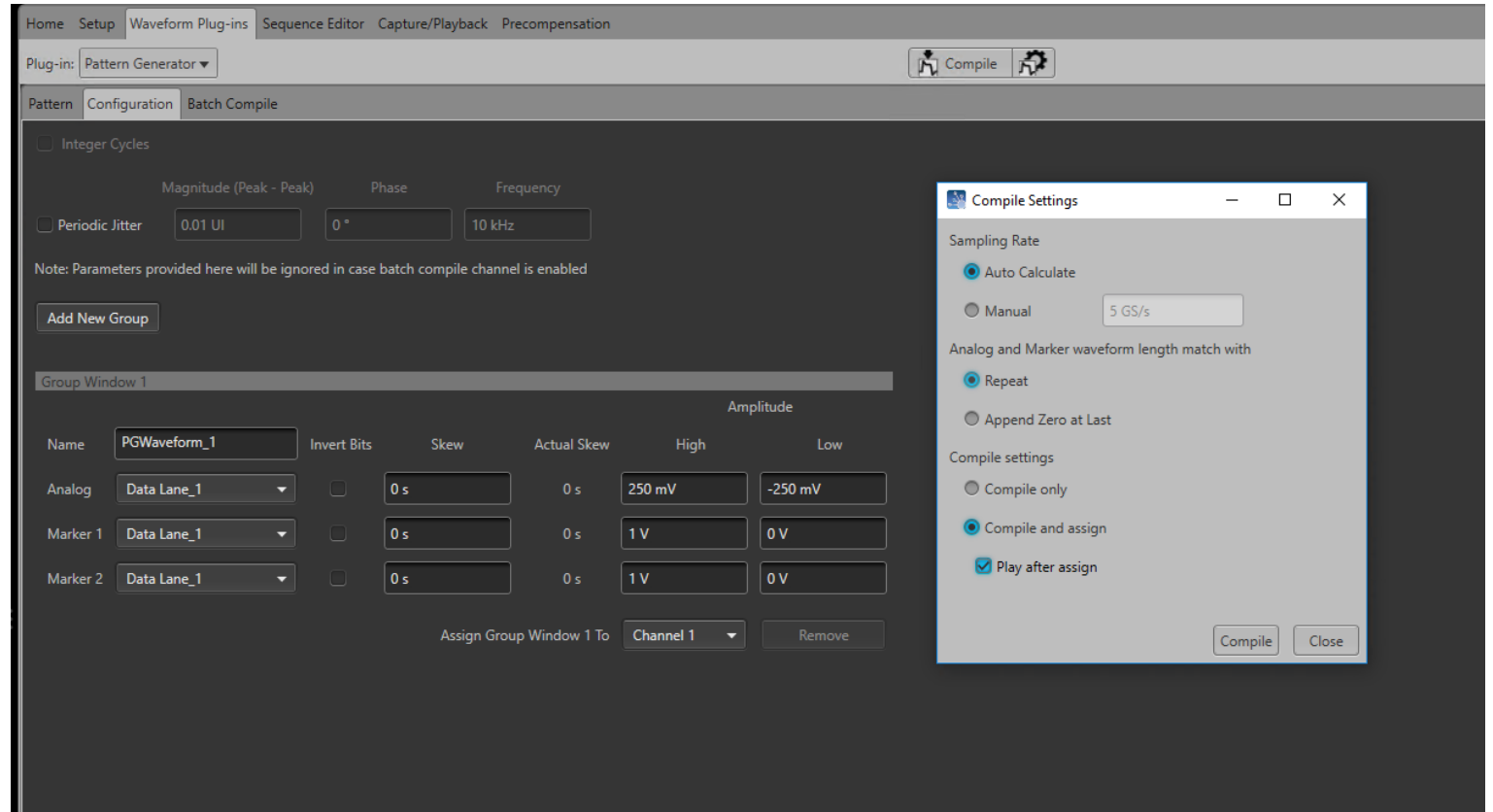
Dual LVDS Bus: 1 CLK + 7 Data



- **10 Gsamples/s sample rate**
- **16 bit vertical resolution**
- **2 GHz (-3 db) bandwidth, usable to 4 GHz**
- **2 GSamples/channel memory**
- **-70 dBc SFDR (In-band, 10 GS/s, DC-1.25 GHz)**
- **1.5 Vp-p Diff @ 2 GHz**
- **-85 to +10 dBm @ 10 MHz to 2 GHz**

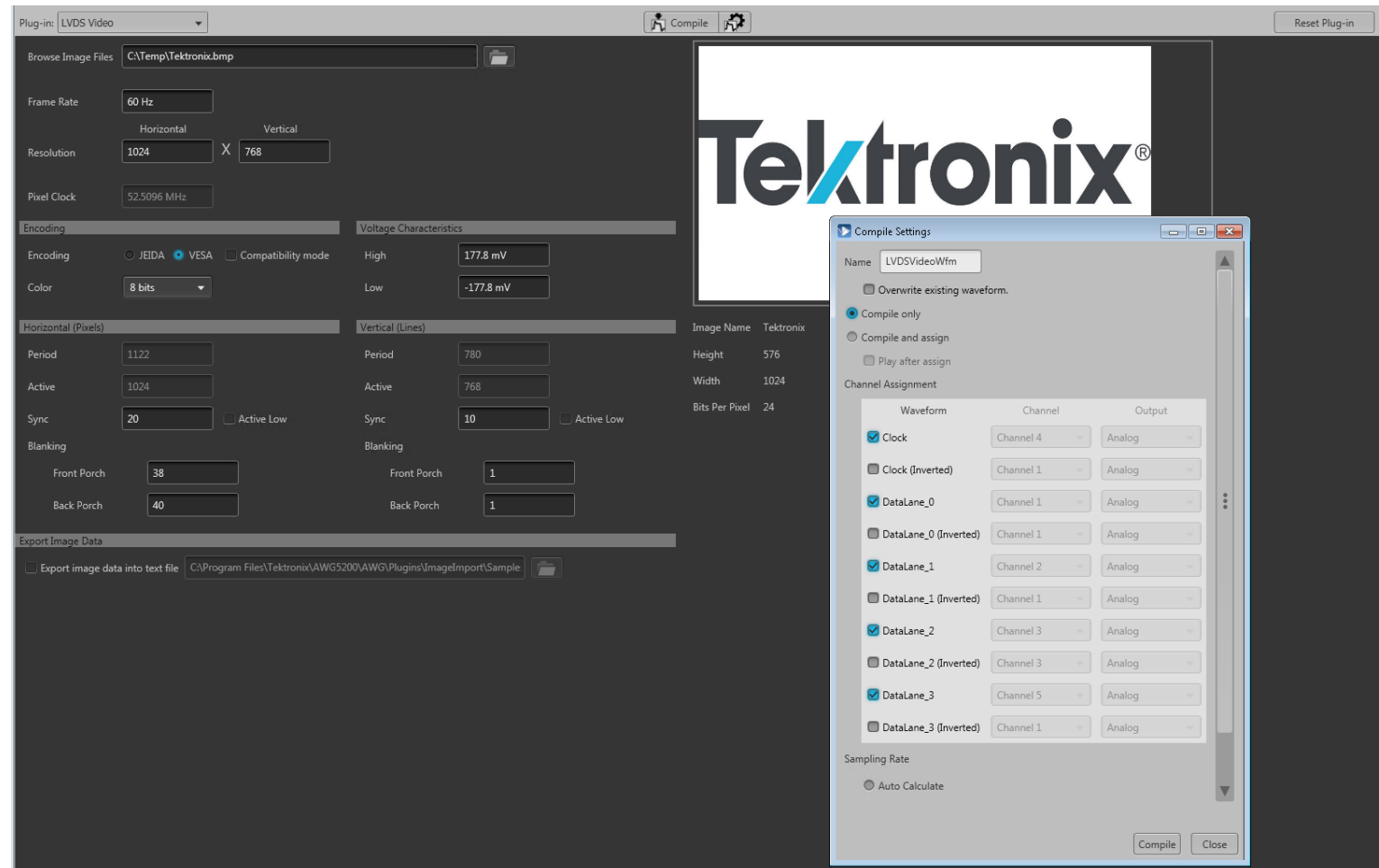
Pattern Editor Plugin

- *Import .txt pattern files*
- *Create, edit, and play out pattern signals*
- *Apply impairments: Skew, Periodic Jitter, Amplitude*
- *Create Batch of Data Patterns for easy stress testing*



LVDS Video Plugin

- *Import .bmp files*
- *Create static video test signals for LVDS display testing.*
- *VESA/JEIDA for 6, 8, 10-bit signals*



RX Test demo



Thank You!
谢谢大家!