Tektronix

半导体材料与器件科学云讲堂

——超快脉冲在先进的NVM测试中的应用及神经元网络测试前瞻

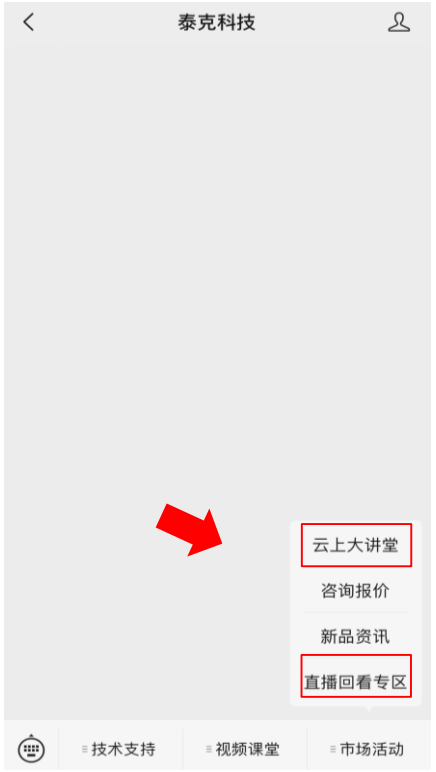
2020/6/12

主讲人：赵咏梅　　——泰克半导体行业开发经理

半导体材料与器件科学云讲堂

- ✓ 专业测试平台
- ✓ 六大类测试流程
- ✓ 剖析、解决半导体新问题

关注“泰克科技”公众号



每月2期专题直播，等您解锁！

直播日程

第一季 直播课程 (4~6月)

纳米材料及纳米电子器件IV和CV测试	4月29日
二维材料/石墨烯及其电子器件IV和CV测试	5月15日
量子材料及超导材料电输运物性表征测试	5月29日
超快脉冲在先进的NVM测试中的应用及神经元网络测试前瞻	6月

番外篇一

测试技巧：半导体参数测试仪使用技巧及案例集锦 6月

第二季 直播课程 (7~9月)

- 宽禁带半导体(GaN/SiC)材料及器件测试
- 功率IGBT器件测试系统及自动化简介
- 微机电系统MEMS测试概述
- MOSFET的准静态CV/超低频CV测试
- 半导体器件可靠性HCI/NBTI测试

番外篇二

测试技巧：快速上手自动化半导体参数测试系统

Tektronix

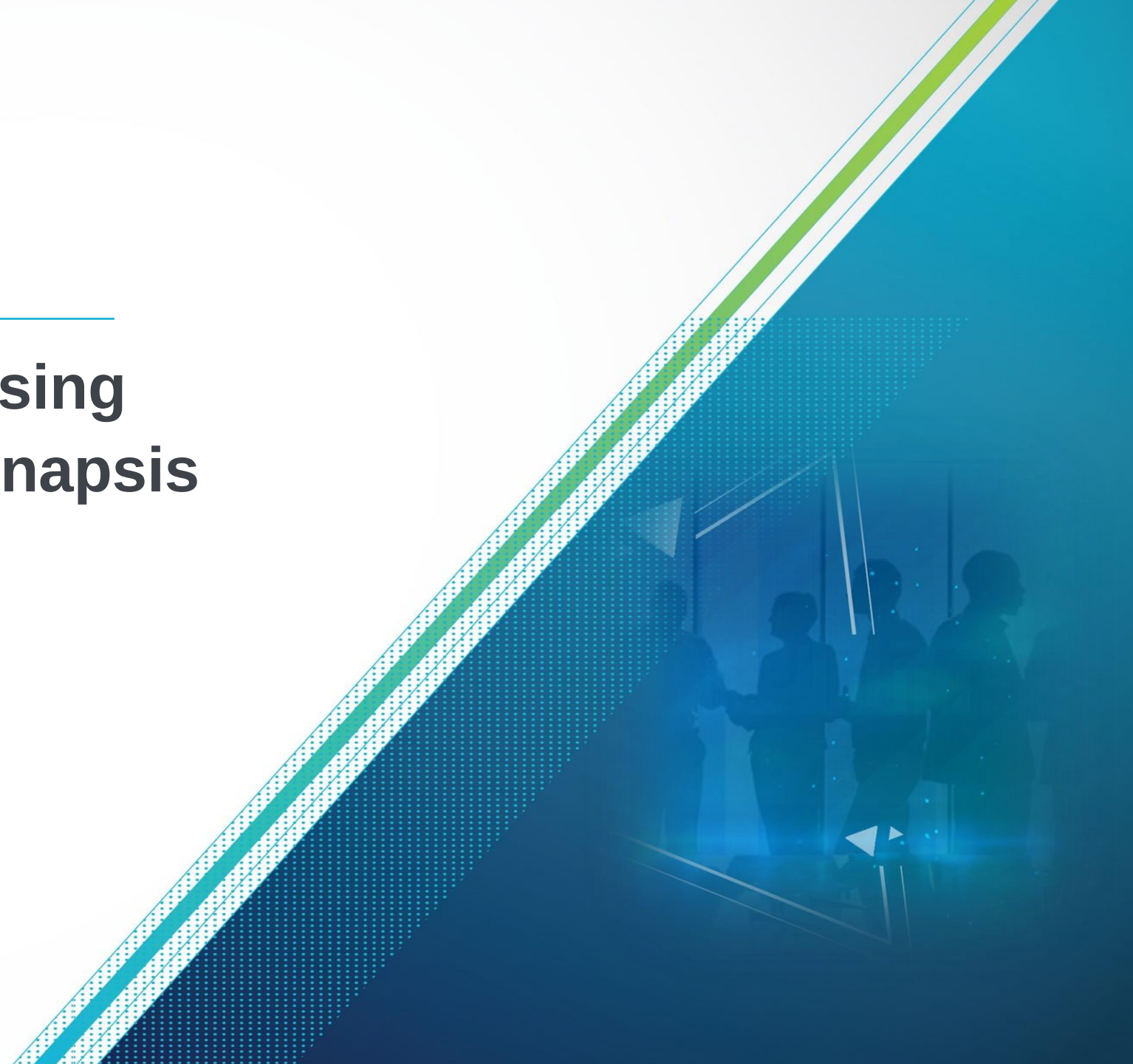
Non-Volatile Memory Using Pulse Techniques & Synapsis networking Tester

11 JUNE 2019

Maggie Zhao

Semiconductor Development Manager

KEITHLEY
A Tektronix Company



Non-Volatile Memory

- Used for storing data
  - Database servers
  - Personal computers
  - Smartphones and other devices
  - Automobiles
  - Home appliances
  - Industrial machines
- Traditional technologies
  - Hard Disk Drives (magnetic)
  - Magnetic tape and floppy drives (magnetic)
  - CD, DVD, BluRay, Laser Disk (Optical)

Non-Volatile Memory

TECHNOLOGIES

- NAND flash has ruled for years
  - Floating gate technology
  - Thumb drives, SSD, Smart phones, etc.
  - Majority of the market still
- Researchers are developing new memory technologies for better performance
  - Phase change memory (PRAM)
  - Resistive memory (ReRAM)
  - Magnetoresistive memory (MRAM)
  - And others!

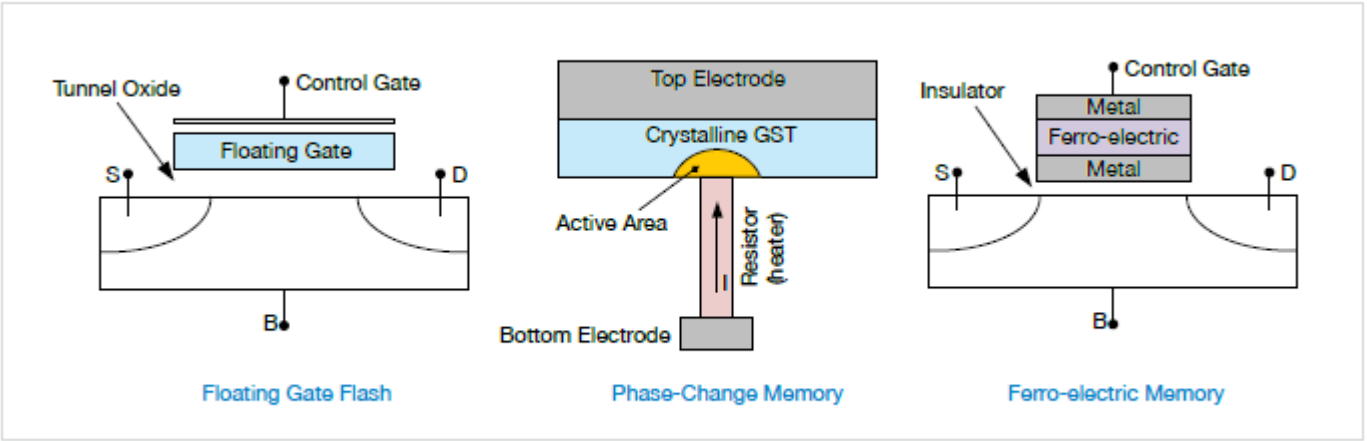


Figure 1. Various non-volatile memory devices.

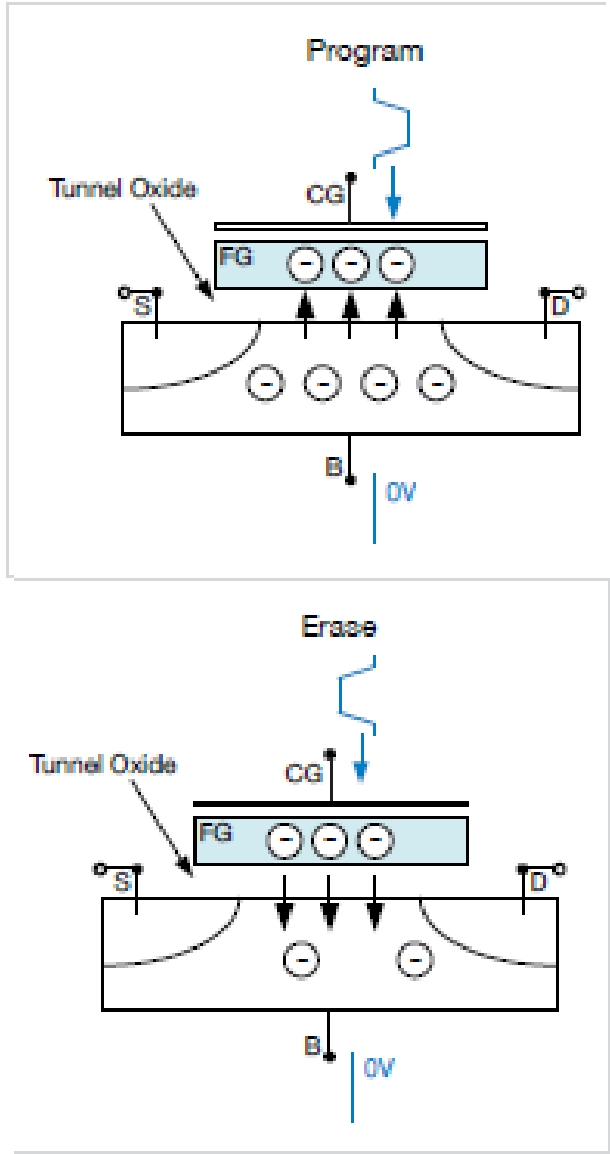
Non-Volatile Memory Emerging Technologies

NVM Type	How it Works
Floating Gate Flash	Charges and discharges the floating gate to create the “1” and “0” logic
Phase Change (PRAM)	Cells are switched from an ordered crystalline phase to a disordered, amorphous phase.
Magnetoresistive (MRAM)	Polarity is changed in one of two ferromagnetic plates to provide memory storage.
Ferro-electric (FeRAM)	The memory mechanism is based on a polarization shift in ferroelectric materials.
Redox (ReRAM)	A filament is formed through a dielectric and can be reset or set by an applied voltage.
Conductive-bridging (CBRAM)	Memory storage is based on the physical re-location of ions within a solid electrolyte.
NanoRAM (NRAM)	Uses Carbon Nanotube Transistors (CNT) which are placed in two or more resistive modes.
SONOS	"Silicon-Oxide-Nitride-Oxide-Silicon“. Closely related to Flash NVM but uses silicon nitride.

Floating Gate Technology

FG NVM

- Similar to a Silicon-Based FET
  - Gate, Drain, Source, Bulk
- Contains a second, floating gate
  - Tunneling or Hot Carrier Injection trap a charge
  - Allows the FET to “remember”
- Can be produced with familiar technology
  - We are very good at creating silicon devices
- Does have some downsides
  - Can be slow
  - Degrades
  - Scalability (Floating gate can only be so small)

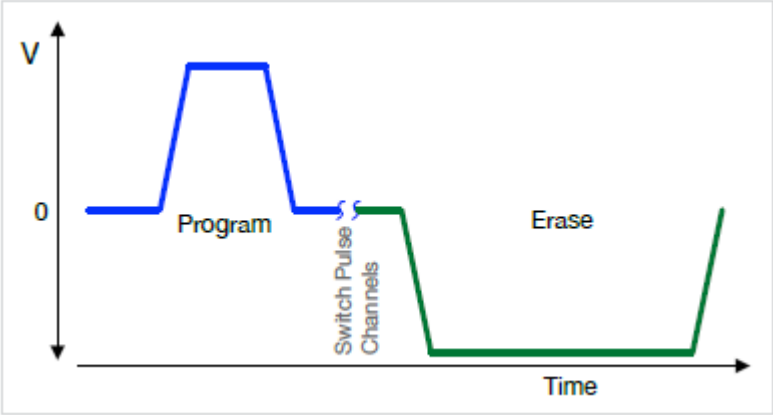


Testing FG NVM with Pulsing

PULSE MEASURE UNIT (PMU) WITH 4200A

- Pulses to perform functions
  - Program, Erase, and Read functions
- PMU allows testing at close to real-world conditions
- Endurance testing
  - Increase number of program/erase cycles logarithmically until memory cell fails
  - PMU can read/write millions of cycles

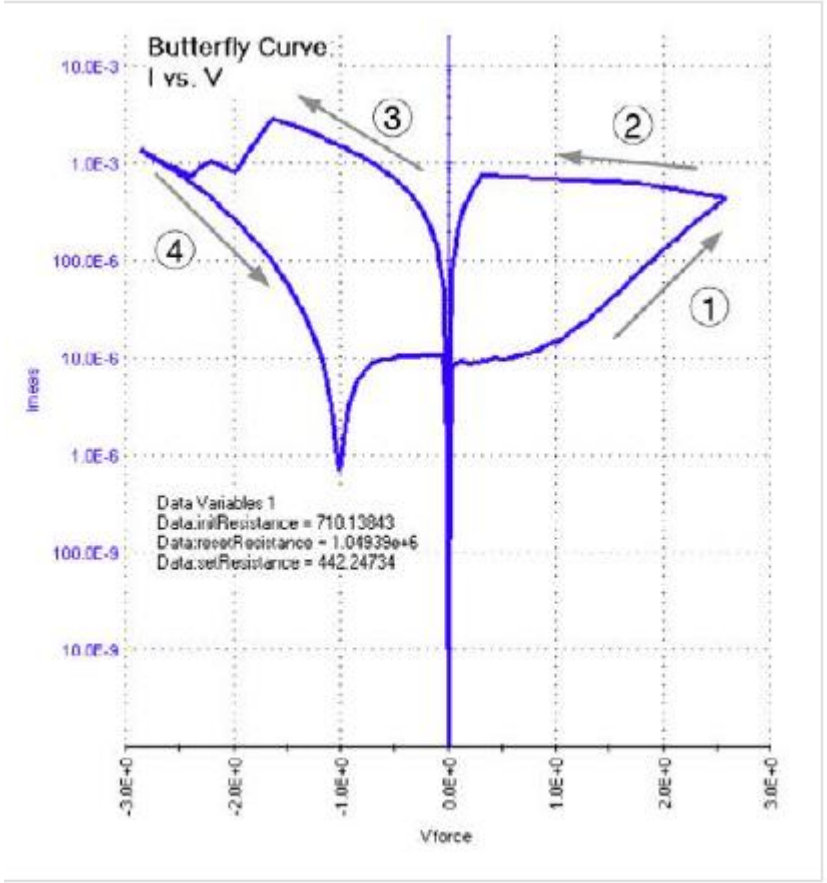
Figure 2. 4225-PMU Ultra-Fast I-V Module and two 4225-RPM Remote Amplifier/Switch Modules.



Testing New Memory Material

RESISTIVE MEMORY (RERAM)

- Similar to testing FG NVM
- Requires different values and timings
- Reliability/Endurance testing is very important
  - These are untested technologies



What if I Need to Go Faster?

- Even the PMU has limitations
  - 70ns pulses at 10V and 200mA
  - 20ns absolute minimum pulse
- Newer FG NVM can go *fast*
  - Below device can be read in ~1ns

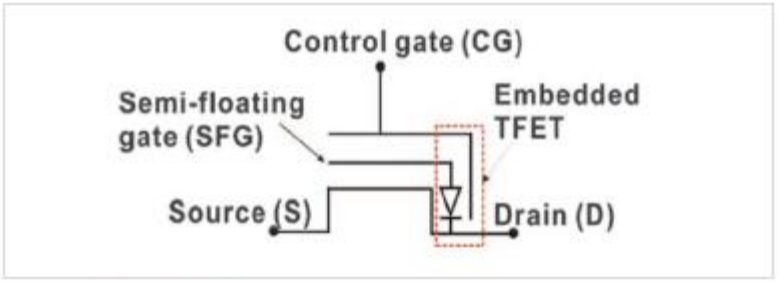


Figure 5: Semi-floating gate memory cell.

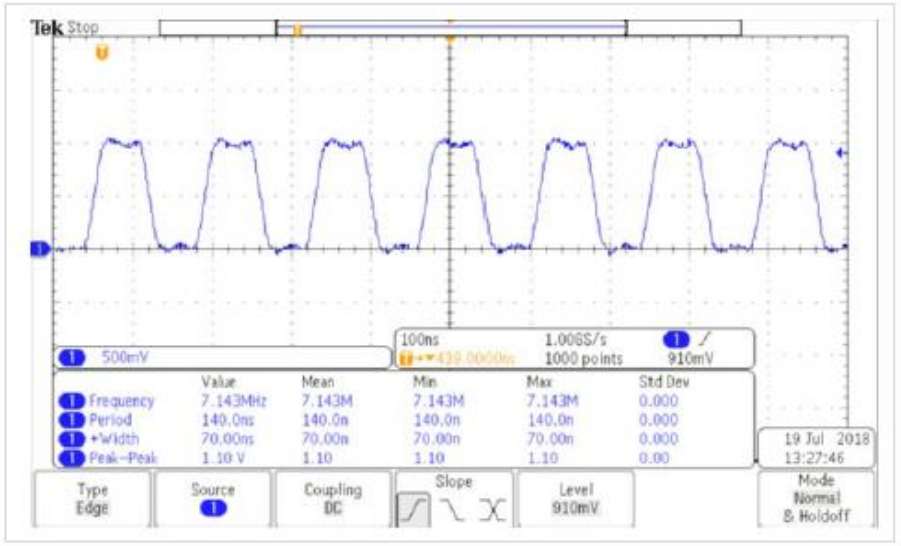


Figure 2: Recommended minimum pulse width using the 4225-PMU.

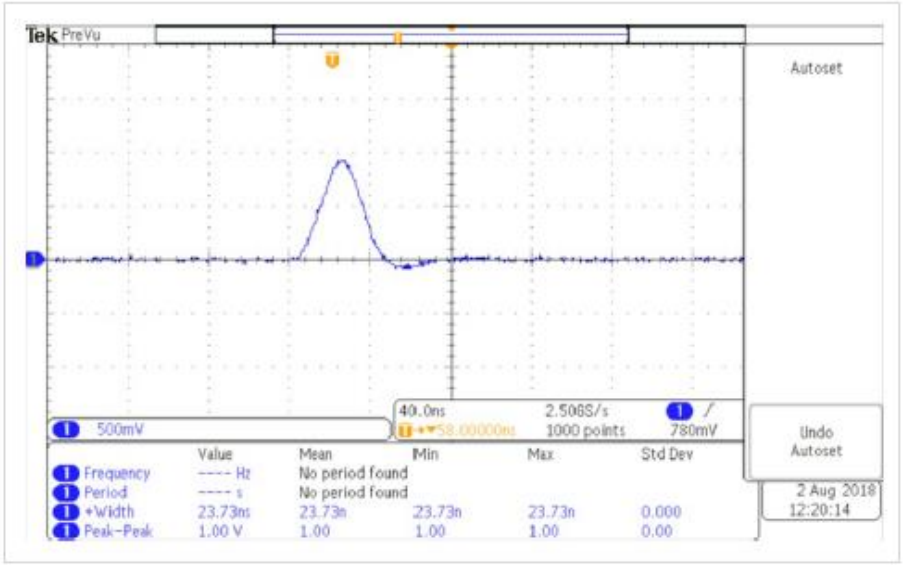
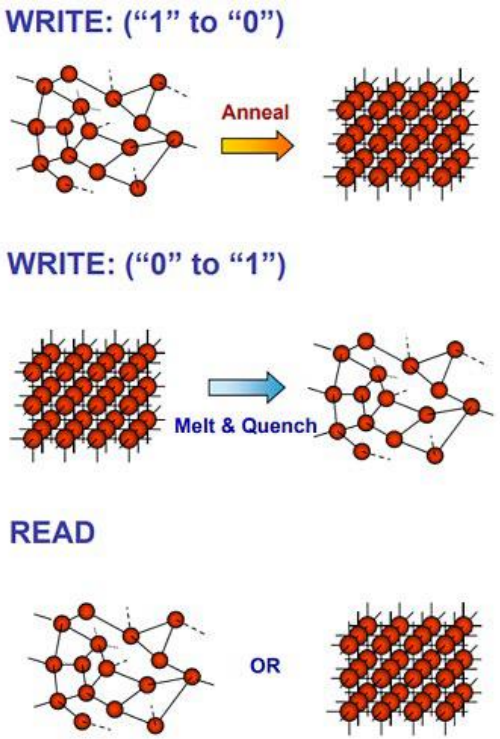
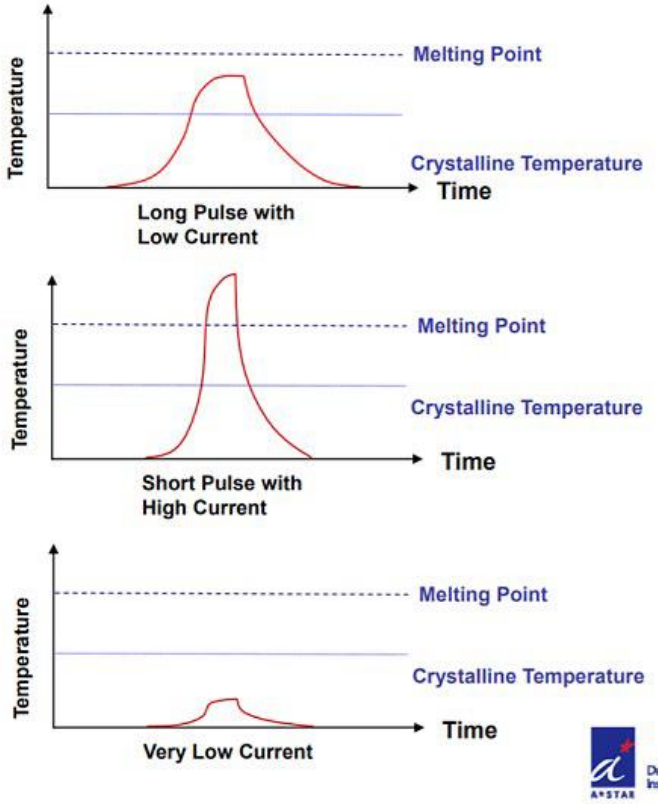


Figure 3: Minimum pulse width allowed by the software.

Phase Change Memory (PCRAM)

- Different functions require different pulses.
- Need to control many factors
  - Pulse duration
  - Off time
  - Pulse voltage
  - Pulse current

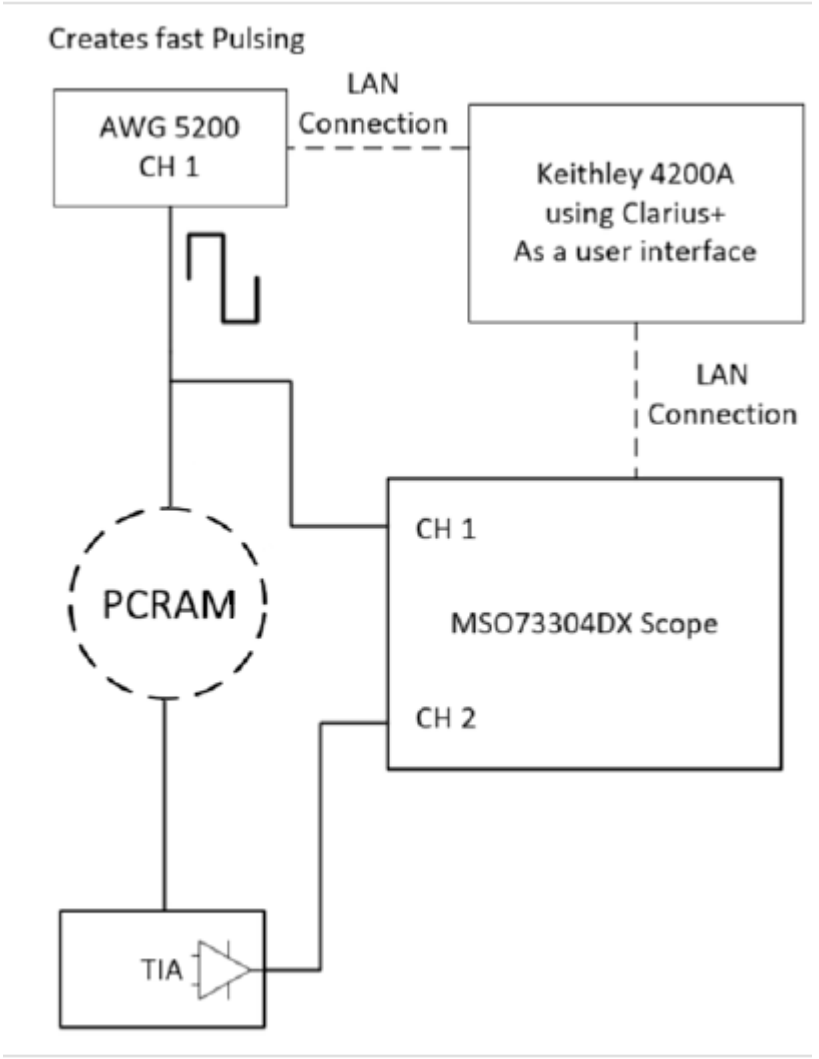




Nanosecond Pulse Setup

2 TERMINAL SETUP

- Good for 2 terminal memory cells like PCRAM, ReRAM, and MRAM.
- This setup is a bit more complicated than the previous with just the PMU
  - 4200A for control and data gathering
  - AWG for pulsing
  - Oscilloscope for measuring response
  - TIA for converting current to voltage

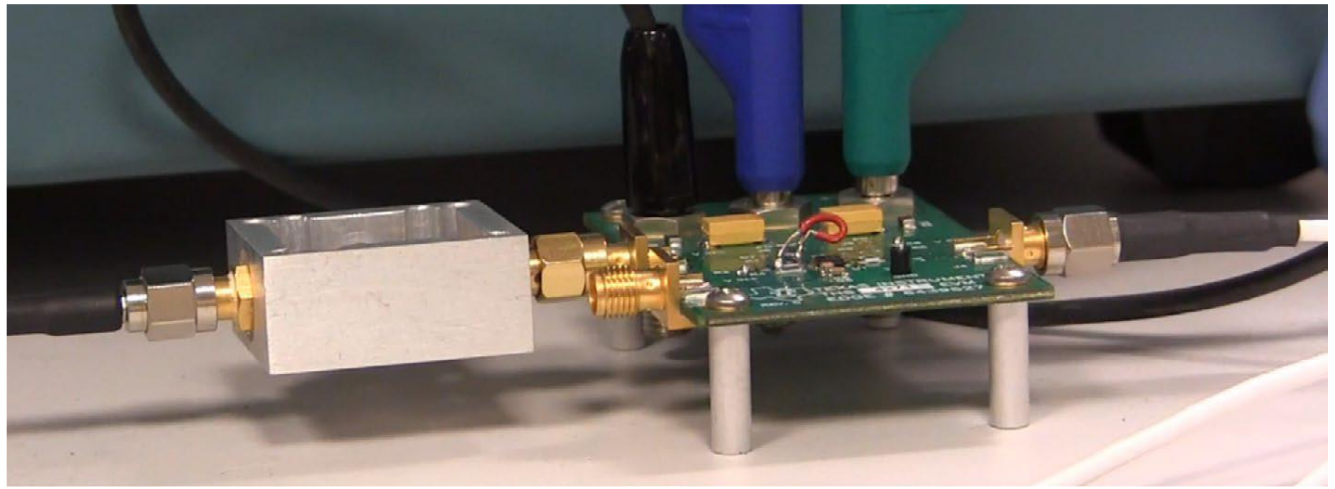


Fast and Low Current

- Very tricky measurements
- Low current measurements are very prone to noise
  - Thermal noise
  - EMI noise
  - Photoelectric effects
- Low current measurements typically require a long integration time

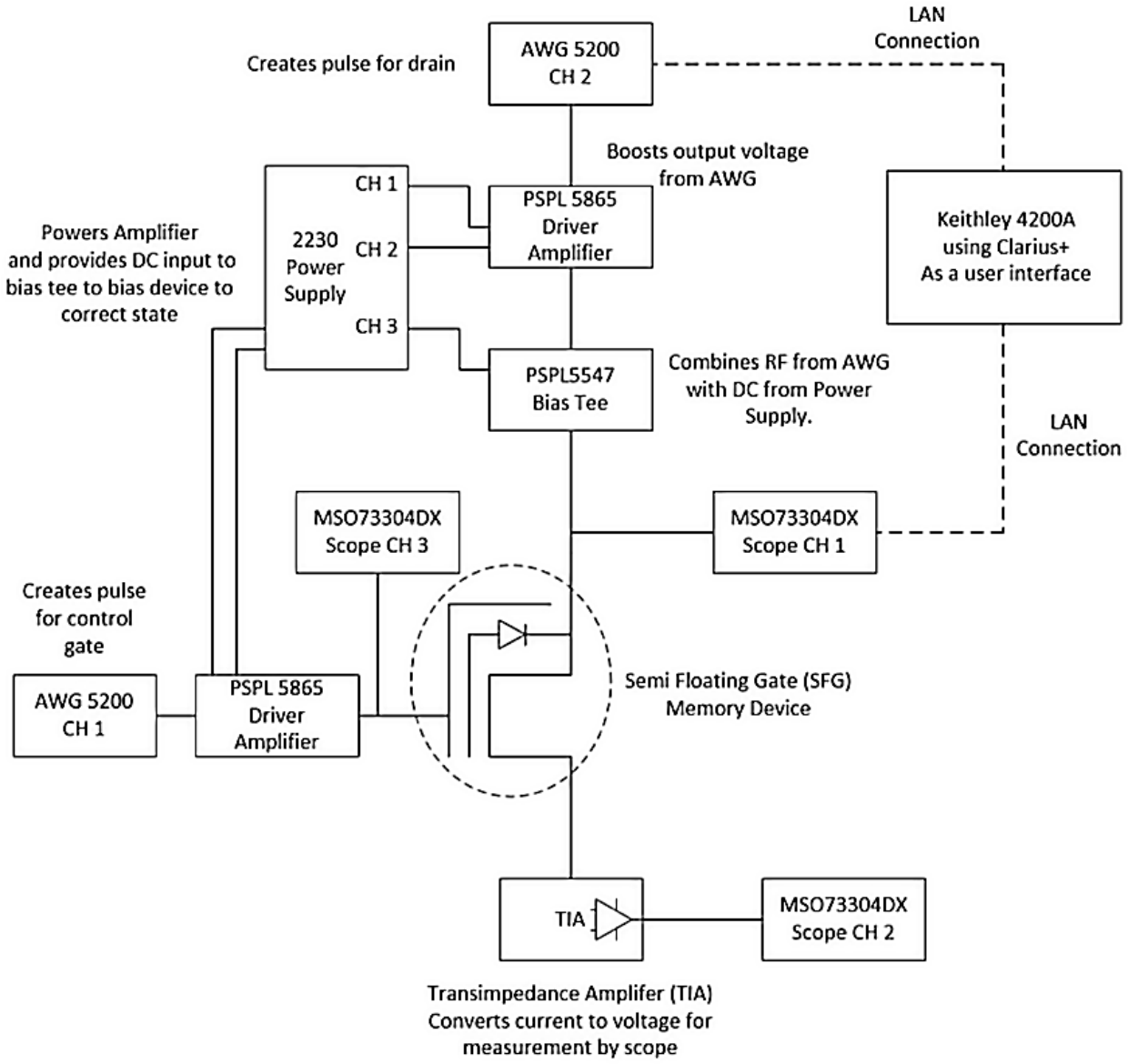
Transimpedance Amplifier

- Current-to-voltage converter
- Typically used in sensor applications to amplify current output
- Need to pick carefully
  - Some are very noisy or have very large offsets
  - Different applications can tolerate different amounts of error



Three Terminal Setup

- This device required three terminals, higher power, and DC biasing
- Required some tweaks
  - Addition of amplifiers
  - Addition of bias tees
  - Upgrade to a 4-channel scope
  - Addition of a 3-channel power supply
- Still used AWG, TIA, and 4200A



Physical test setup

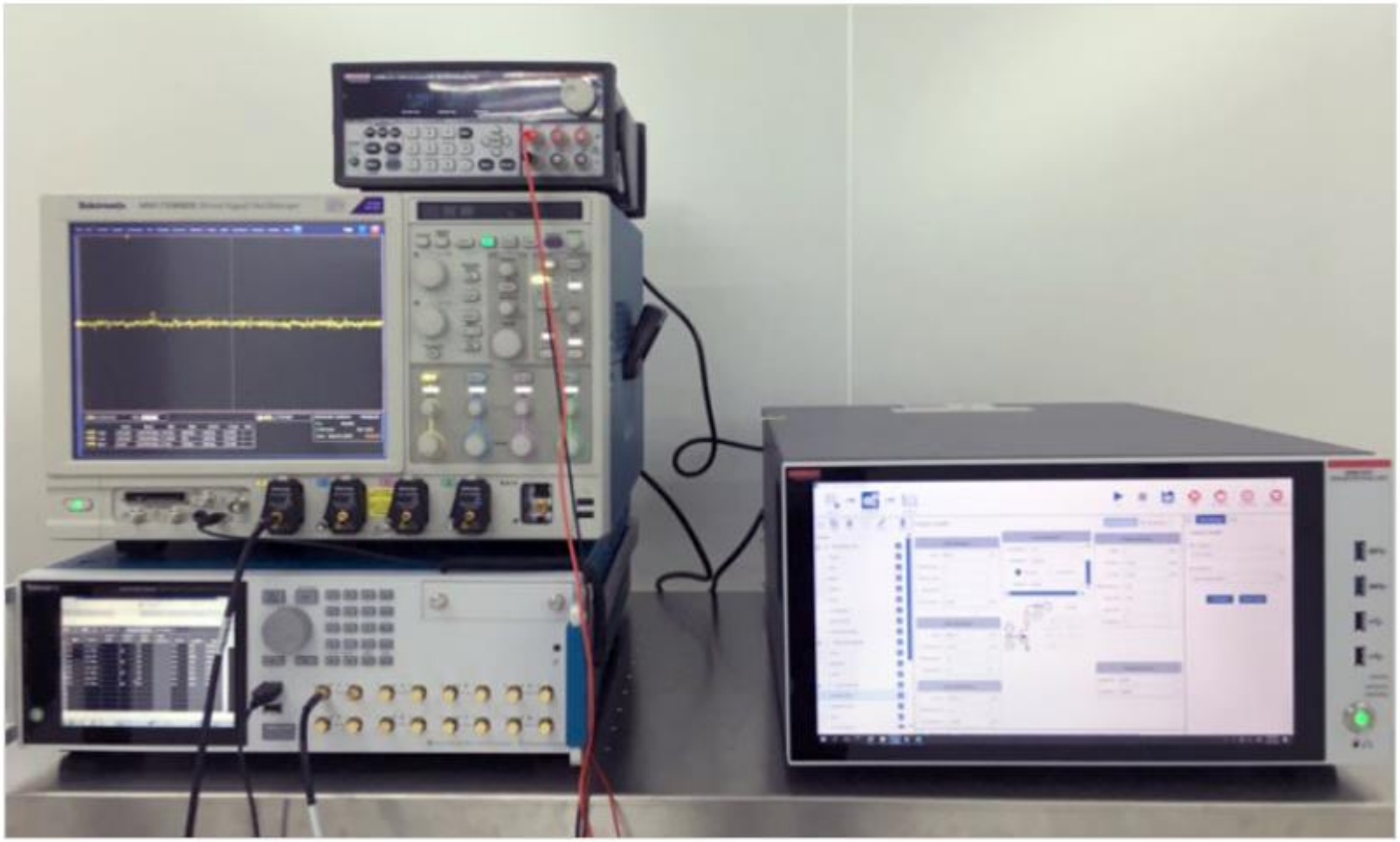
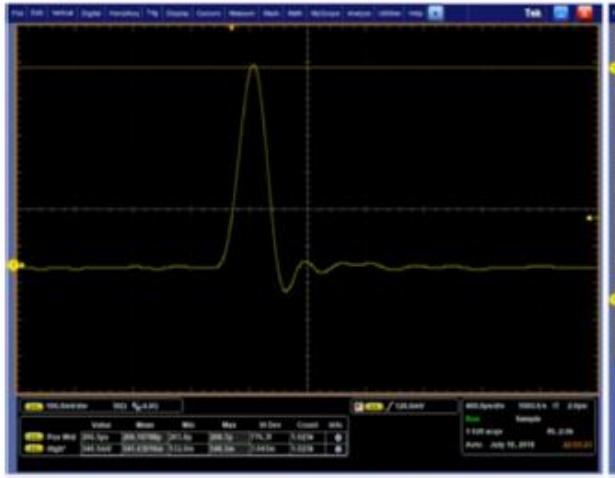


Figure 11: Tektronix solution testing.

Conclusion

- Ultra-fast pulsing is required for the development of new NVM devices
- Keithley 4225-PMU is excellent at this type of testing
- When higher speeds are needed, we need to get creative
- Tektronix's solution allows memory pulse testing down to <1ns

200 ps Write1 Pulse Width



1 ns Write1 Pulse Width

1 These pulses represent the Write1 pulse, also known as the Set Pulse. 1 ns pulse width is shown here, as well as a 200 ps pulse width to show the AWG capabilities.

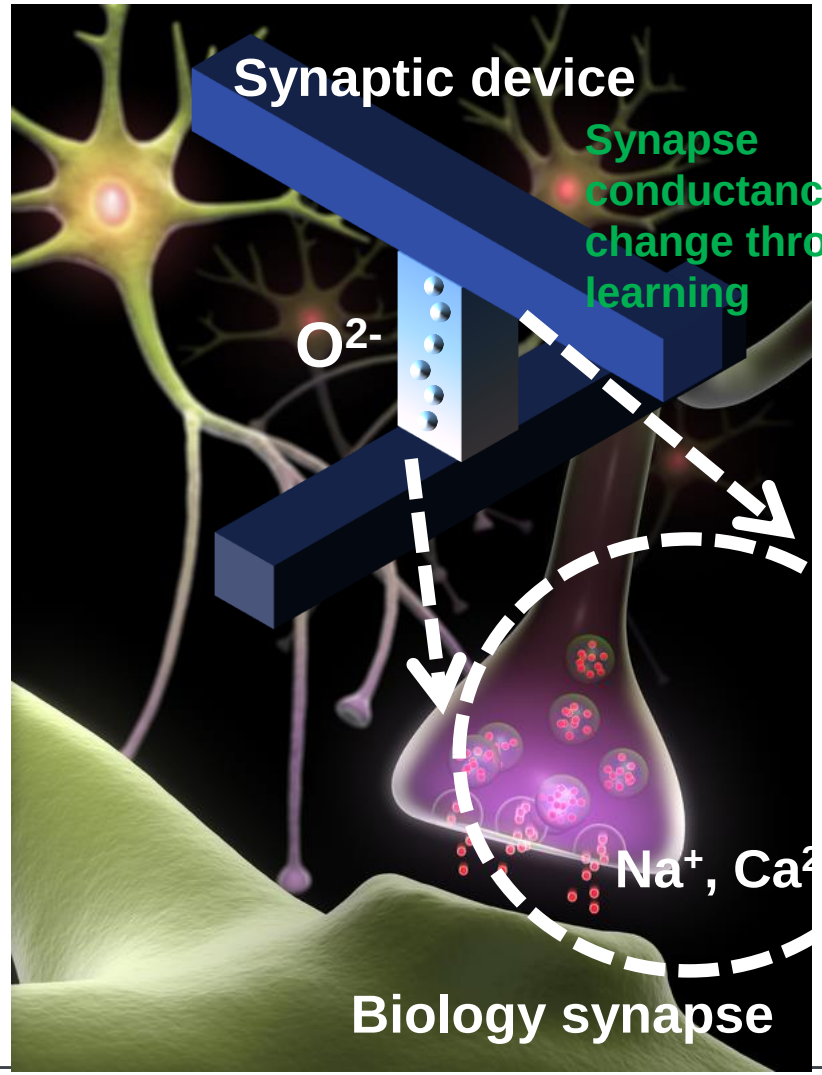
1 µs Read Pulse Width

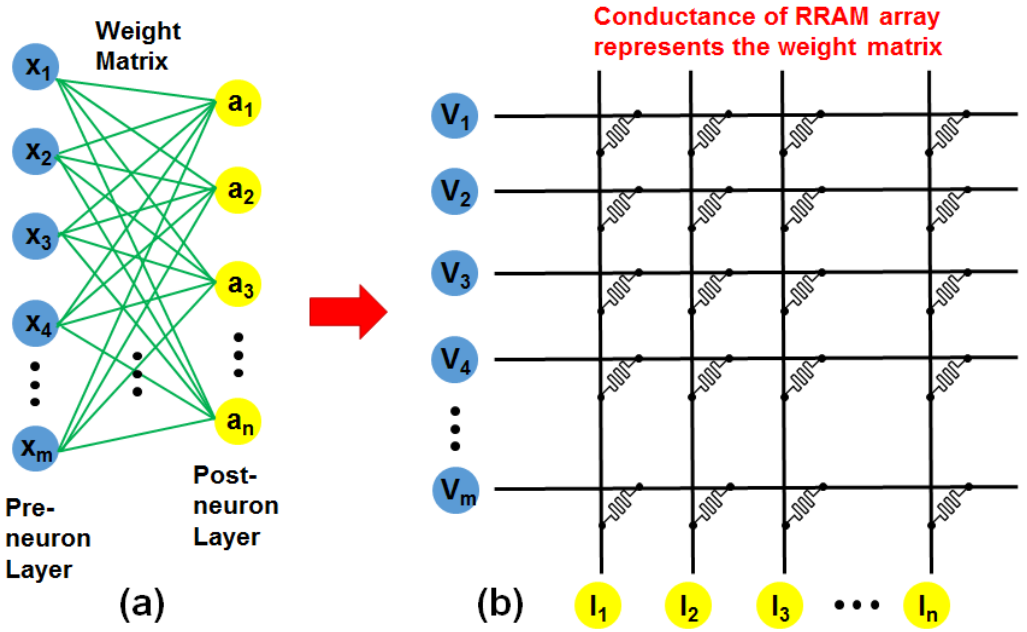
1 ns Write0 Pulse Width

2 and 4 These pulses represent the Read pulses. Read pulses are where the measurement is performed, and they're usually long pulses.

3 This pulse represents the Write0, also known as the Reset or Erase.

RRAM Properties is similar to Synapse
- From Tinghua University Prof. GaoBin





- RRAM properties is similar to synapse → electronic synapse
- RRAM can realize in-memory computing, solving von Neumann bottleneck
- Crossbar or 3D architecture could support large RRAM in parallel

Device Cell characterization Steps

01

Forming

Verify the resistor before and after forming, higher voltage than Vset, typical no specified testing step and being combined with Cell IV Characterization

02

Cell I-V-t characterization

Testing the set/reset HRS/LRS I-V character, with slow t for basis memristor testing.

03

High speed pulse testing

Device cell set/reset testing, opt. with verification steps

04

Data Retention

After write the cell, keep reading with time/temperature conditions

05

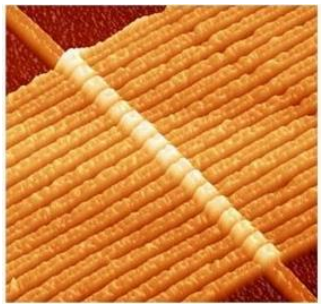
Cell Endurance

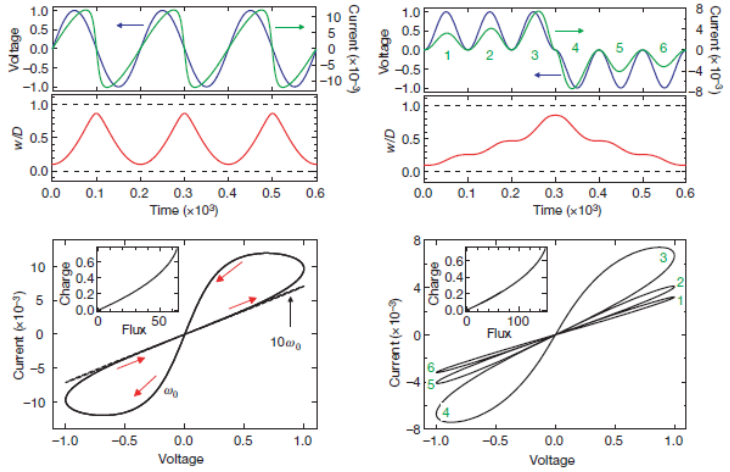
High frequency write (set/reset) and keep reading for cell performance variation checking

Device Cell I-V-t Characterization

- I-V-t Test Condition
  - 1x SMU, Opt. 1x PMU
  - $V_{Set/Reset}$ @<10V, I @>nA range, t @>50ns interval
  - I-V Sweep, Opt. Pulsed I-V
- Solution
  - HW: Parameter Analyzer
    - 4200A-SCA
    - 4200-SMU
    - 4225-PMU
    - Manual Probe Station
  - SW: Clarius

Type of analog RRAM	Ag:a-Si [2]	TaO_x/TiO_2 [3]	PCMO [4]	$AlOx/HfO_2$ [5]	ETML/HfO_x (0.8mΩ·cm)	ETML/HfO_x (4.4mΩ·cm)	ETML/HfO_x (30.4mΩ·cm)	ETML/HfO_x (2 parallel)	Ideal analog RRAM
Nonlinearity (SET)	2.40	0.66	3.68	1.94	0.96	0.93	0.04	0.08	0
Nonlinearity (RESET)	-4.88	-0.69	-6.76	-0.61	-3.26	-2.63	-0.63	-0.63	0
On-state resistance	26 MΩ	5 MΩ	23 MΩ	17 KΩ	10KΩ	30kΩ	100kΩ	50kΩ	High
ON/OFF ratio (analog region)	12.5	2	6.8	4.4	10	10	10	10	Large
SET pulse	3.2V/300µs	3V/40ms	2V/1ms	0.9V/100µs	1.7/50ns	1.5V/50ns	1.6V/50ns	1.6V/50ns	Low voltage Fast speed
RESET pulse	2.8V/300µs	3V/10ms	2V/1ms	1V/100µs	1.5V/50ns	1.5V/50ns	1.5V/50ns	1.5V/50ns	Low voltage Fast speed
Variation	3.5%	<1%	<1%	5%	3%	3.35%	3.7%	1.5%	0%

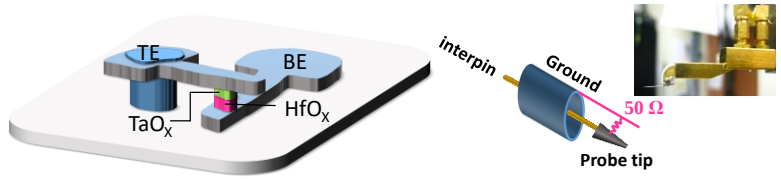


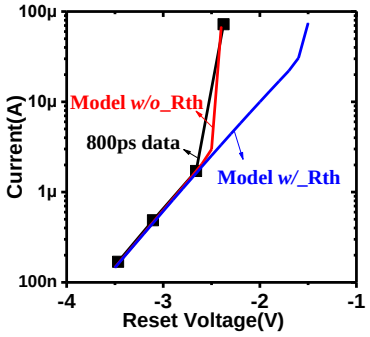


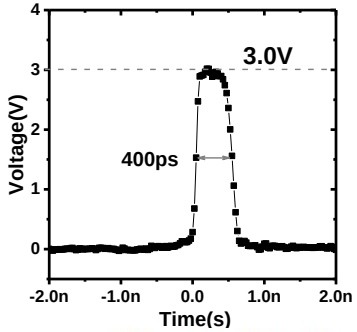
Device Fast Pulse Set/Reset

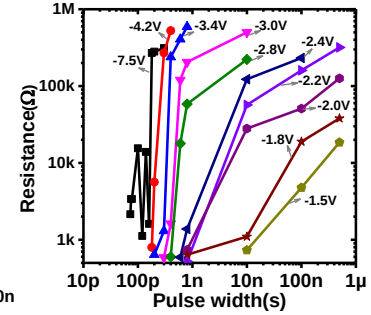
- Fast Pulse Set/Reset
  - Device speed performance
  - Removing the self-heating effect by longer set/reset time
- Solution:

Solution	~50ns Pulse	<1ns Pulse
HW	4200A-SCS, 4200-SMU, 4225-PMU	AWG5200, MSO/DPO70000
SW	Clarius	Customized SW
Pulse Width Typ.	70ns @ 10V, 200mA range	<1ns
Pulse Width Min.	20ns	200ps
Reading Speed	200MSa/s	100GSa/s
TIA	N/A	Opt. from FEMTO









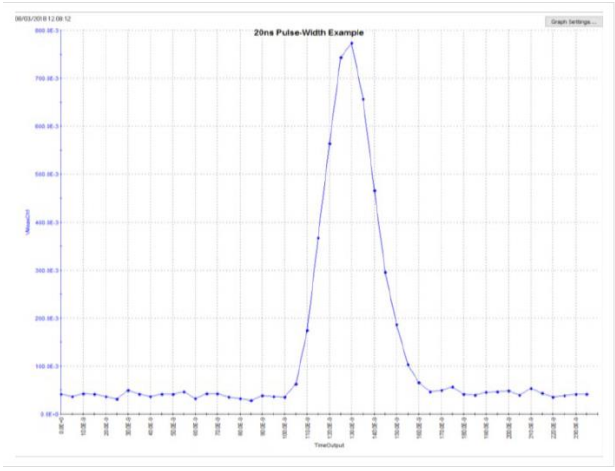
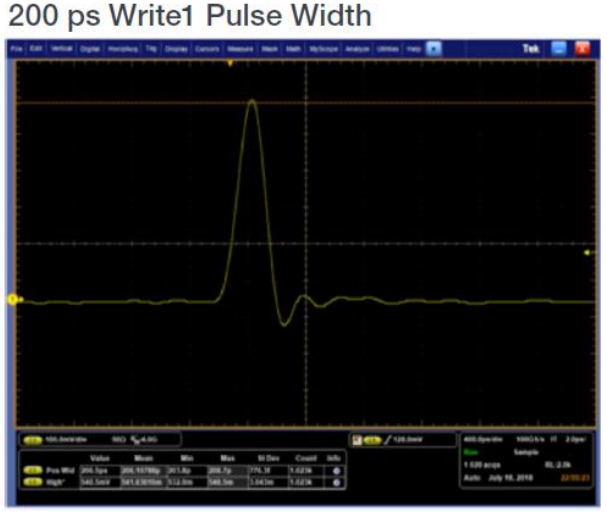


Figure 4: Measurement taken at 5 ns sample interval with the PMU.

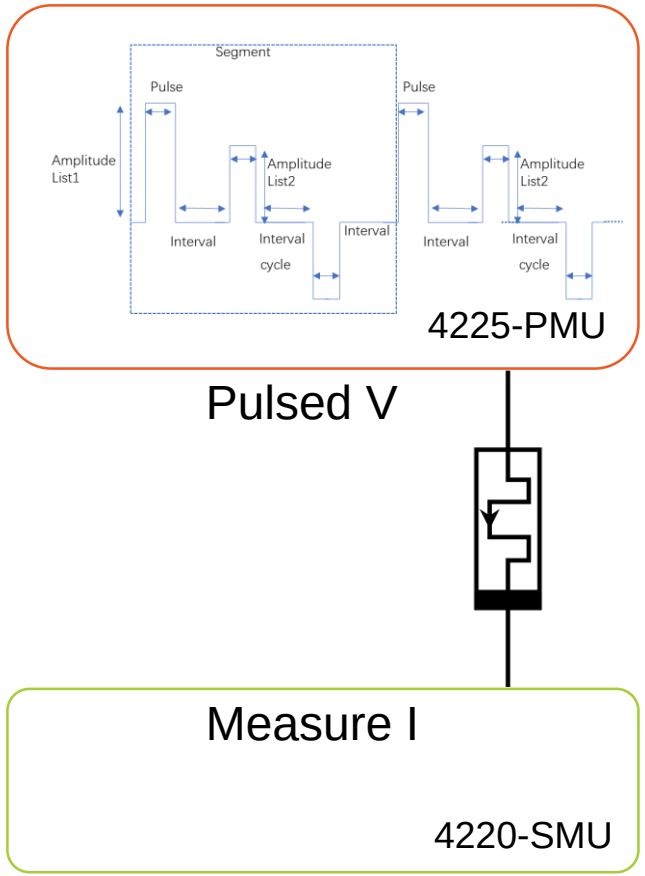


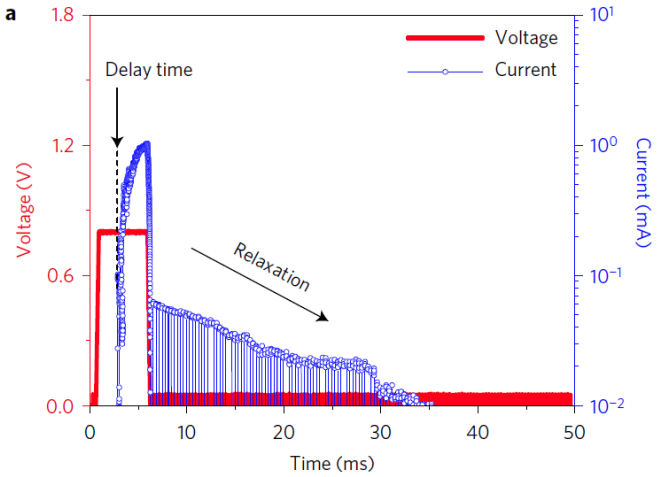
KEI 4225-PMU
- Min 20ns pulse generating
- Fast 200MSa/s (5ns interval) Reading

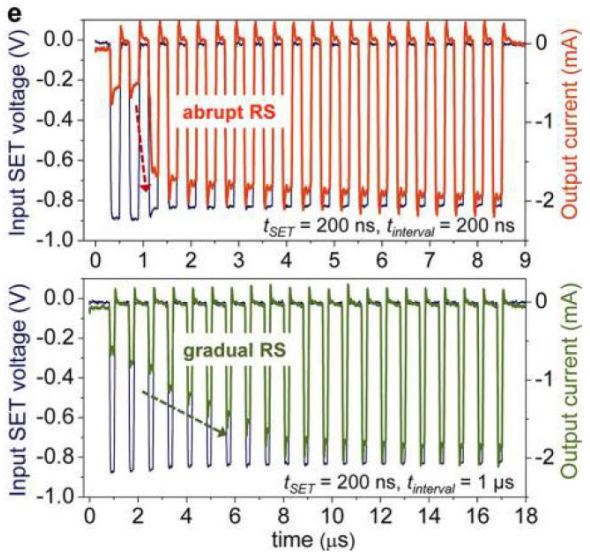
TEK AWG5200, MSO/DPO70000
- Min 200ps pulse generating
- Fast 100GSa/s (10ps interval) Reading

Device Resistance Dynamics Test

- Synapsis Cell Charaterization
- Pulsed I-V-t, lower self-heat
- Solution
  - HW: Parameter Analyzer
    - 4200A-SCA
    - 4200-SMU
    - 4225-PMU
    - Manual Probe Station
  - SW: Clarius w/ customized project





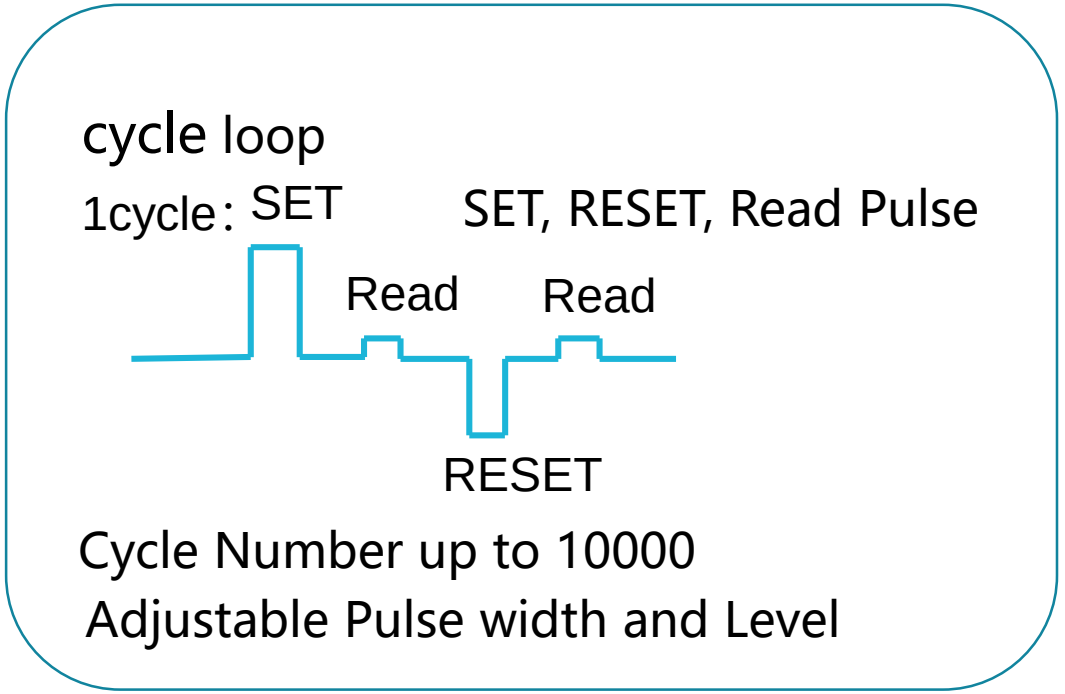


Z. Wang, et al, Nature Materials, 2017
C. Du et al, Nano Letters, 2015, 15, 2203

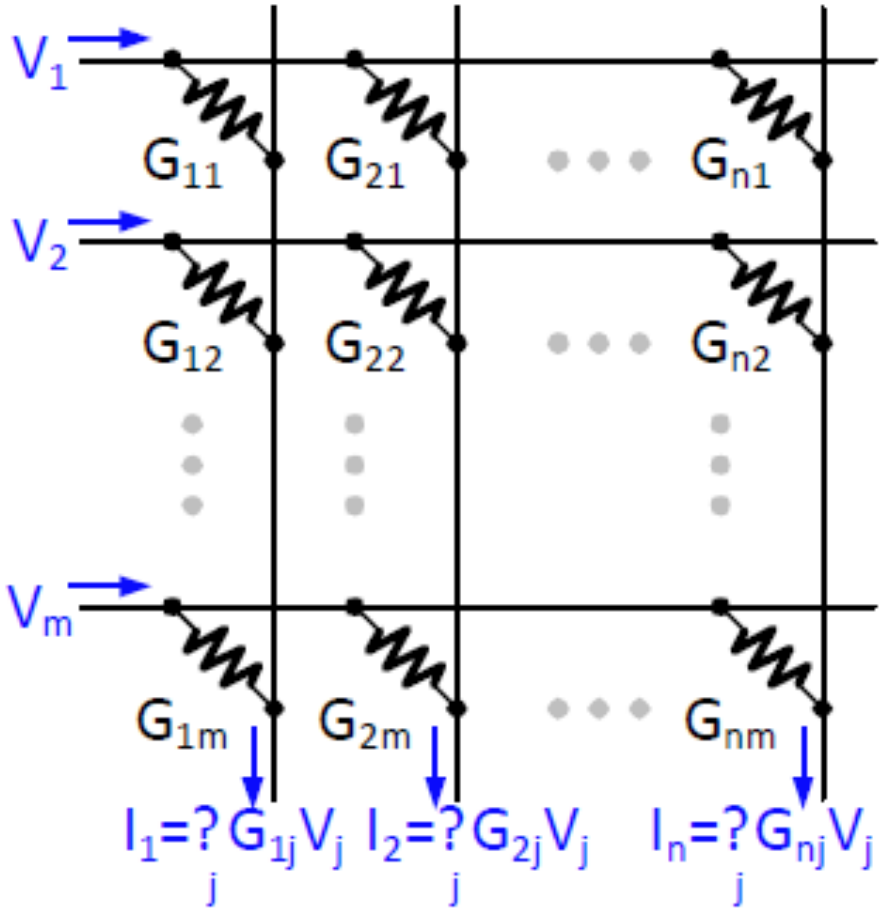
Device Endurance Test

- RRAM Cycling R/W
  - Set/Reset
  - Pulse Set/Reset
  - Memory Retention, long time pulse

- Solution:
  - HW: Parameter Analyzer
    - 4200A-SCA
    - 4200-SMU
    - 4225-PMU
    - Manual Probe Station
  - SW: Clarius w/ customized project



Array Testing & Synapsis networking

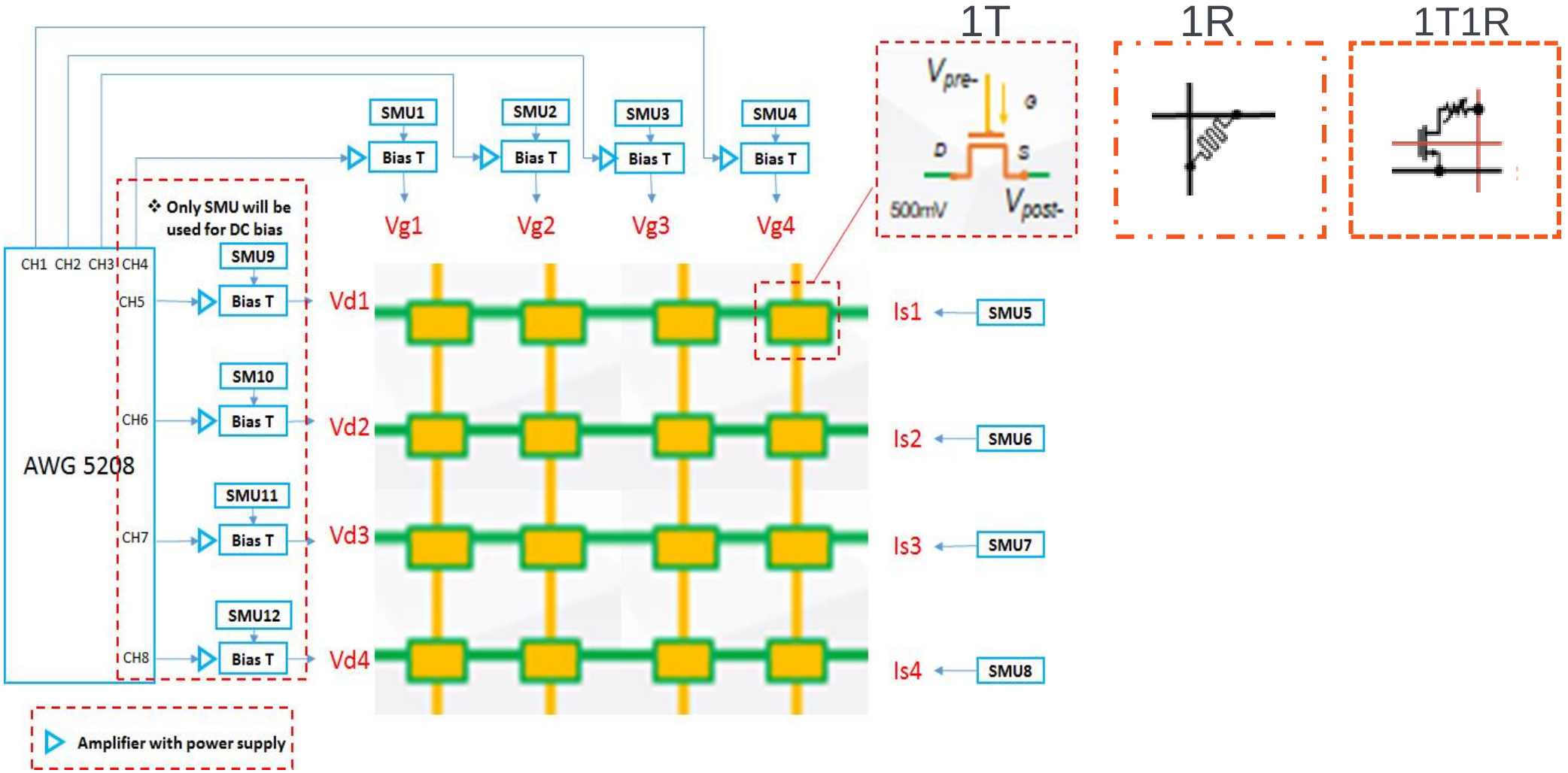


Array and Synapsis networking testing is challenge and hot application in near future.

The basic concept of Synapsis networking testing is to apply different pattern on WL simultaneously, and read back current on BL at same time. The tester need pure parallel testing capability with high synchronism, high quality pulse waveform from nS - mS and low level measurements capability.

To achieve in-lab device characterization testing, We try to set up “ Per- Pin” structure and integrate instruments to meet all challenges.

Array Tester Concept

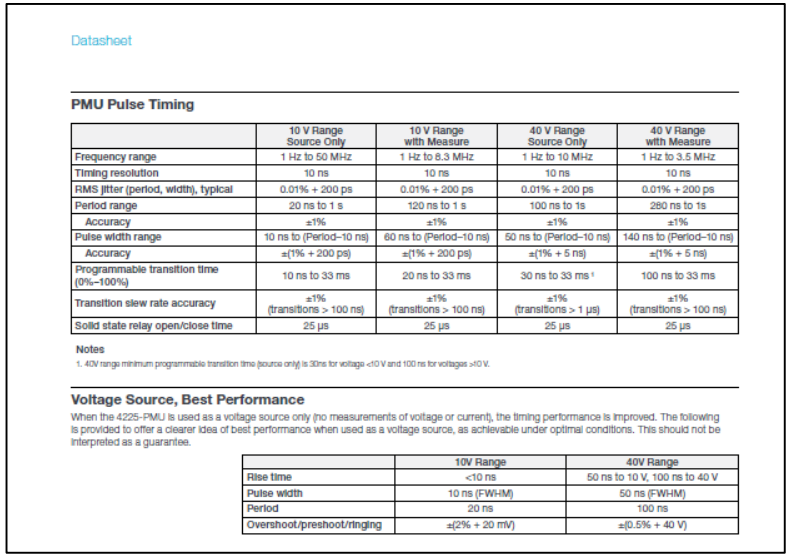


Array Tester Concept

- Wafer level semiauto leading research Synapses networking – Array Testing
- SMU Per-Pin test structure
- From <1nS to mS customized pulse Train
- Outstanding integration capability include prober driver, test sequence control, complex instruments integration and Expertise to handle Low Level to RF testing

Additional Material and Documentation

- *1 ns Pulsing Solutions for non-Volatile Memory Testing*
- *Pulse I-V Characterization of Non-Volatile Memory Technologies*
- *4200A Datasheet*
- Documentation in Clarius+ software



Datasheet

PMU Pulse Timing

	10 V Range Source Only	10 V Range with Measure	40 V Range Source Only	40 V Range with Measure
Frequency range	1 Hz to 50 MHz	1 Hz to 8.3 MHz	1 Hz to 10 MHz	1 Hz to 3.5 MHz
Timing resolution	10 ns	10 ns	10 ns	10 ns
RMS jitter (period, width), typical	0.01% + 200 ps	0.01% + 200 ps	0.01% + 200 ps	0.01% + 200 ps
Period range	20 ns to 1 s	120 ns to 1 s	100 ns to 1s	280 ns to 1s
Accuracy	±1%	±1%	±1%	±1%
Pulse width range	10 ns to (Period–10 ns)	60 ns to (Period–10 ns)	50 ns to (Period–10 ns)	140 ns to (Period–10 ns)
Accuracy	±(1% + 200 ps)	±(1% + 200 ps)	±(1% + 5 ns)	±(1% + 5 ns)
Programmable transition time (0%–100%)	10 ns to 33 ms	20 ns to 33 ms	30 ns to 33 ms [1]	100 ns to 33 ms
Transition slew rate accuracy	±1% (transitions > 100 ns)	±1% (transitions > 100 ns)	±1% (transitions > 1 µs)	±1% (transitions > 100 ns)
Solid state relay open/close time	25 µs	25 µs	25 µs	25 µs

Notes

1. 40V range minimum programmable transition time (source only) is 30ns for voltage <10 V and 100 ns for voltages >10 V.

Voltage Source, Best Performance

When the 4225-PMU is used as a voltage source only (no measurements of voltage or current), the timing performance is improved. The following is provided to offer a clearer idea of best performance when used as a voltage source, as achievable under optimal conditions. This should not be interpreted as a guarantee.

	10V Range	40V Range
Rise time	<10 ns	50 ns to 10 V, 100 ns to 40 V
Pulse width	10 ns (FWHM)	50 ns (FWHM)
Period	20 ns	100 ns
Overshoot/preshoot/ringing	±(2% + 20 mV)	±(0.5% + 40 V)