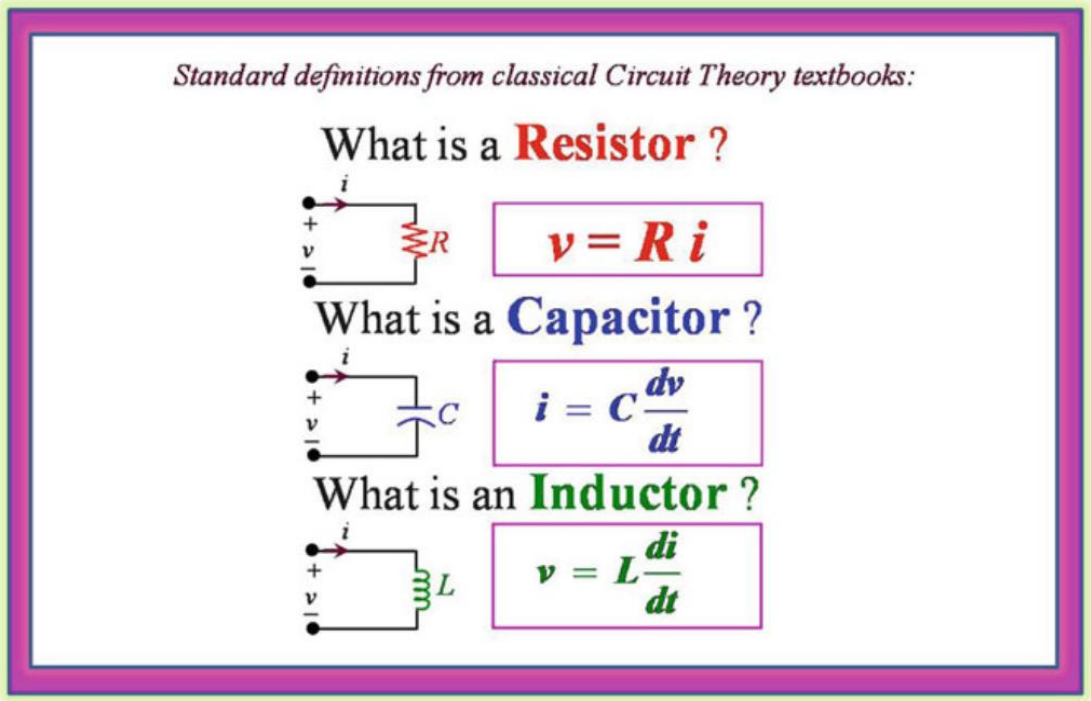
Tektronix

新一代高速存储单元及神经元网络阵列测试方案

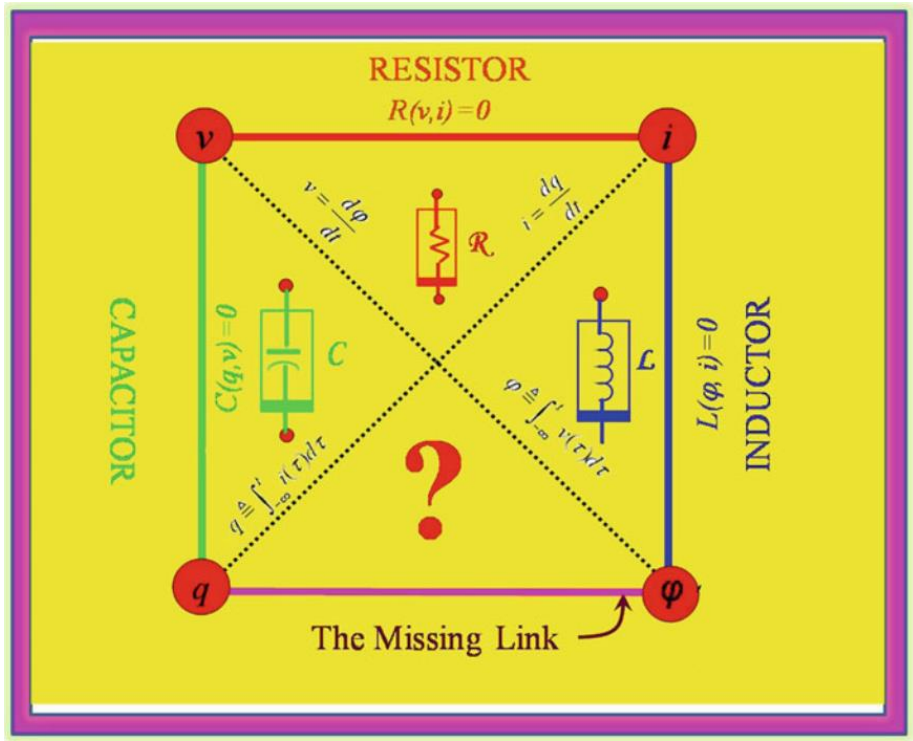
忆阻器基础

忆阻器（Memristor）的概念

- 无源电路基本原件



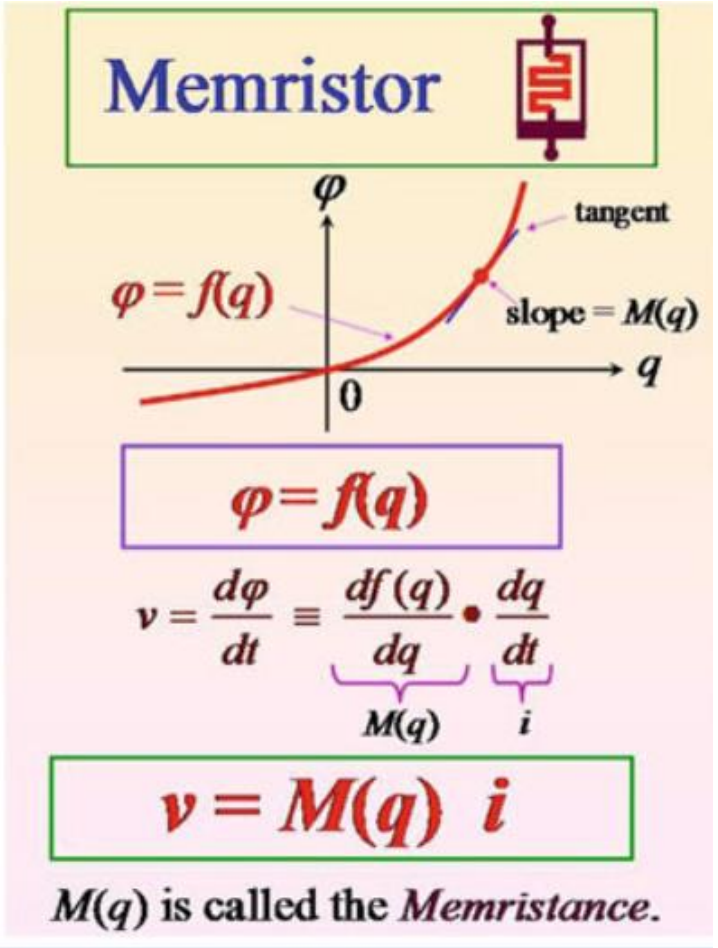
- R
  - v(t) = R(t) * i(t)
- C
  - q(t) = C(t) * v(t)
- L
  - φ(t) = L(t) * i(t)
- ?

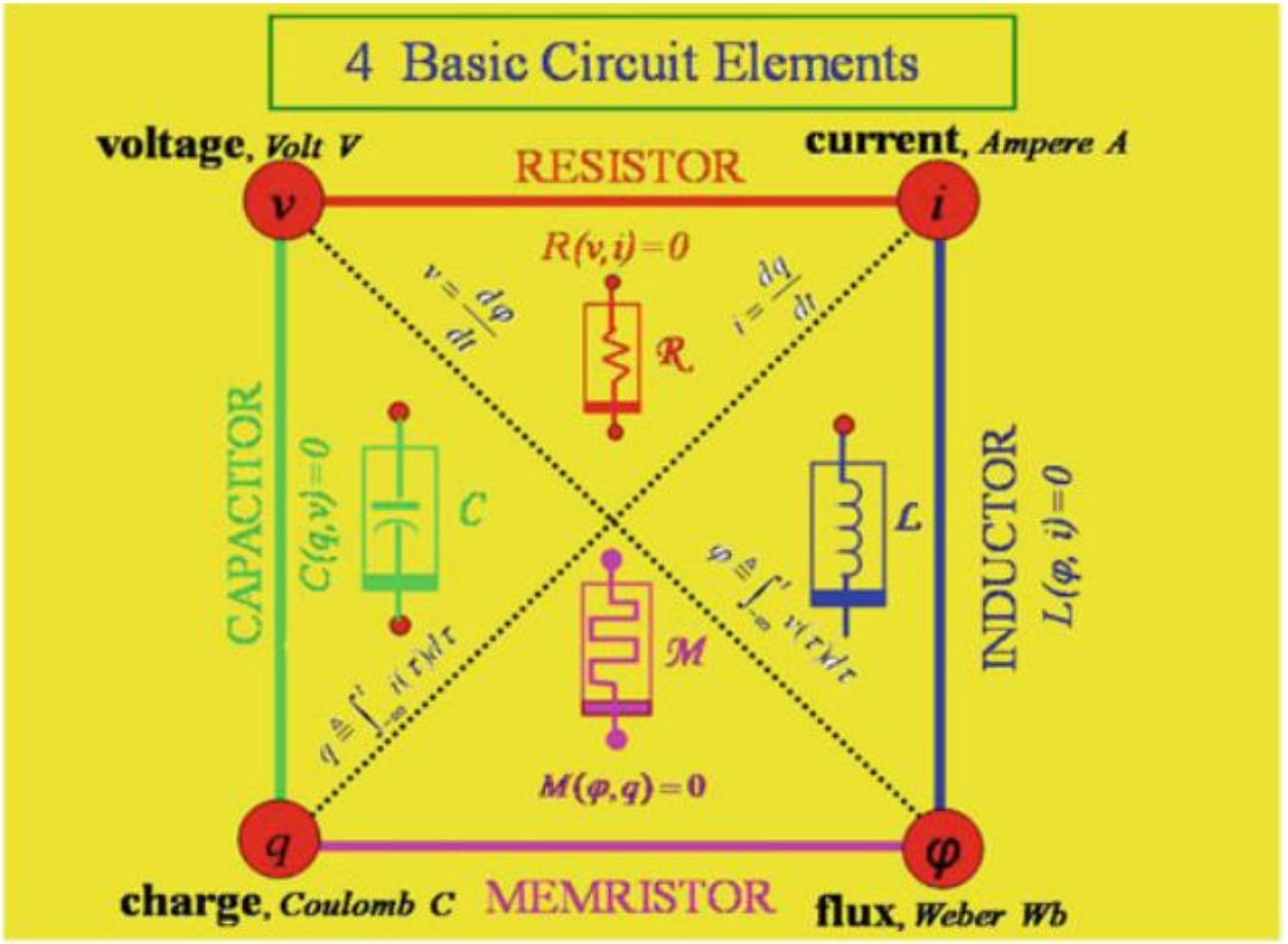


忆阻器（Memristor）的概念

纯数学推导

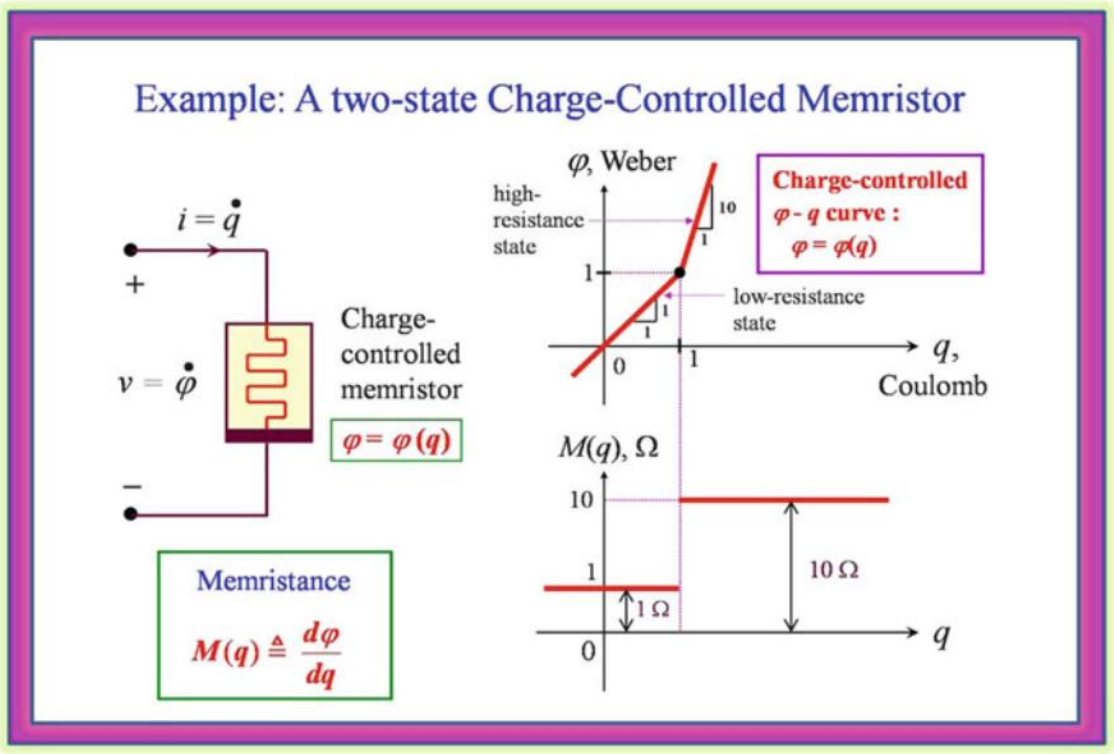
- 1971年华裔科学家蔡少堂首先在数学上给出忆阻器的概念

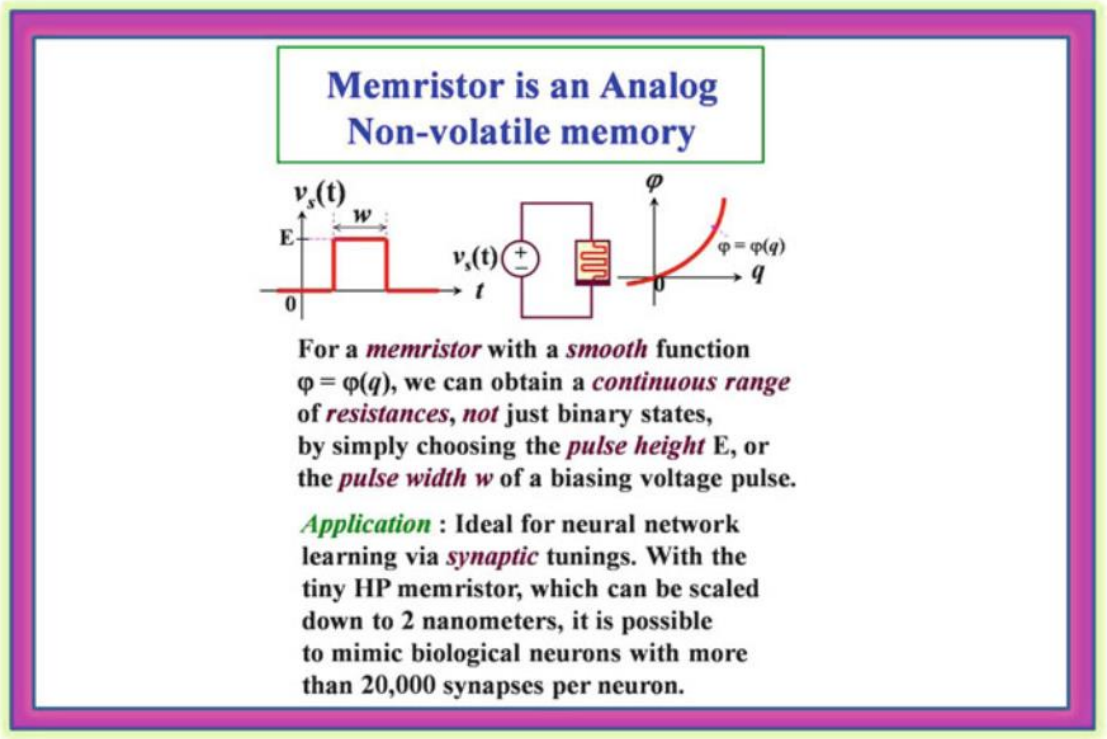




忆阻器（Memristor）的应用

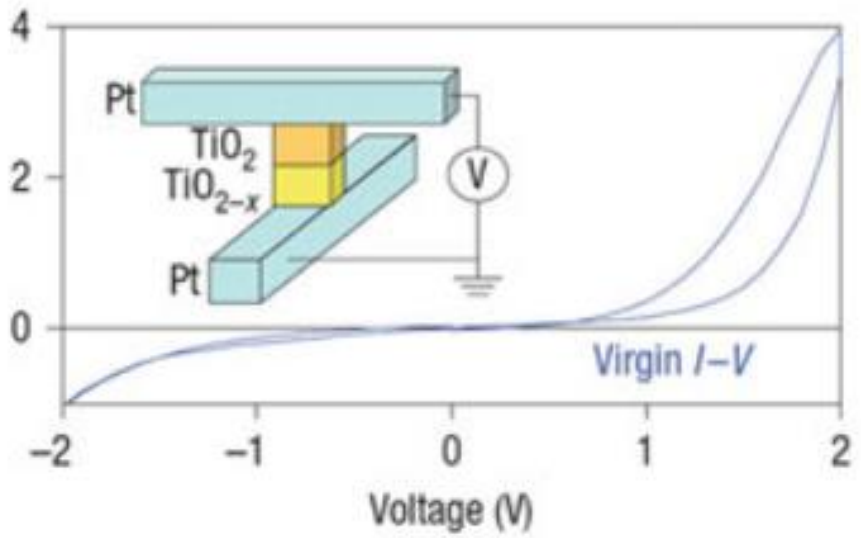
- 用于存储
  - 无功耗
  - 纳米级体积
- 用于模拟人脑
  - 神经元突触
  - 类脑/边沿计算

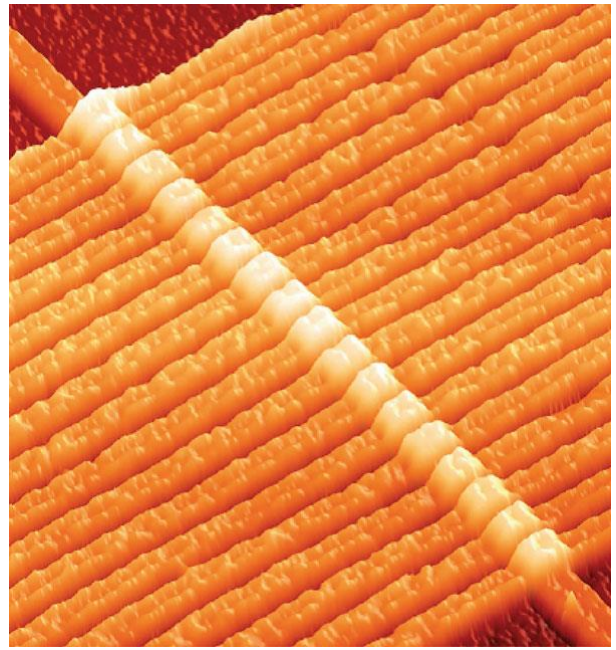




忆阻器（Memristor）的实现

- 2008年 HP 实验室证明了 Crossbar RRAM,即忆阻器的存在



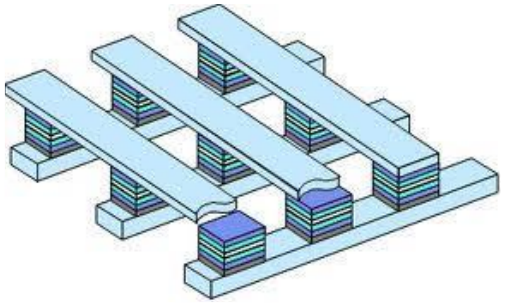


Crossbar Architecture: A memristor's structure, shown here in a scanning tunneling
microscope image, will enable dense, stable computer memories. *Image: R. Stanley Williams/HP Labs*

忆阻器（Memristor）的特性及应用

- 单器件特性
  - 速度快：转变时间 <1 ns
  - 可靠性高：循环次数>10^{12}，保持时间>10年/@200℃
  - 非挥发、多值存储
  - 高密度：器件尺寸<10 nm，可三维集成

- 电路特性
  - 同时兼备高速度、高密度和非挥发性
  - 融合计算与存储
  - 常关（normal off），功耗低
  - 非常适合神经形态计算



忆阻器（Memristor）的分类

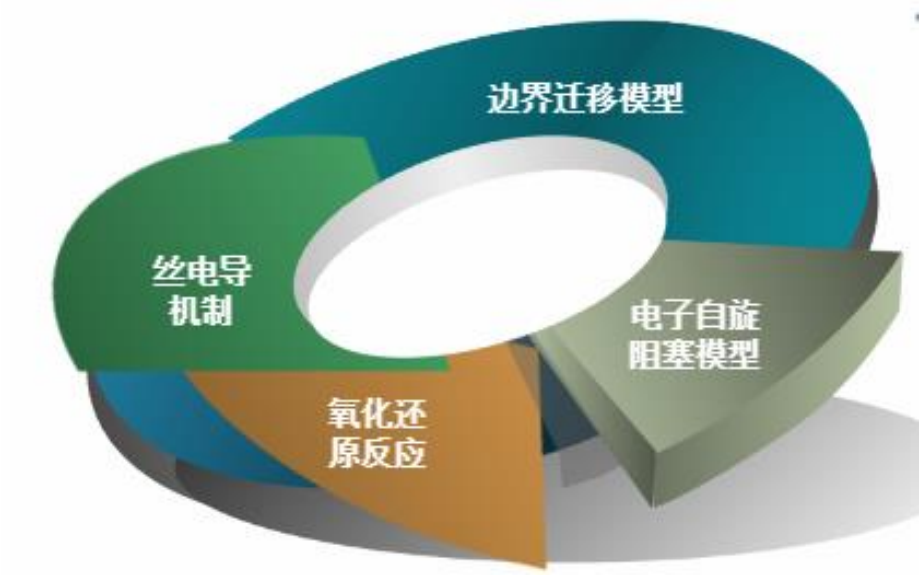


TABLE I
SWITCHING PARAMETERS FOR METAL-OXIDE MEMRISTORS

Parameter \ Devices (mean)	TaO_x [9]	HfO_x [20]	TiO_x [21]	Parameter variance
HRS	$10k\Omega$	$300k\Omega$	$2M\Omega$	$\pm 20\%$
LRS	$2k\Omega$	$30k\Omega$	$500k\Omega$	$\pm 10\%$
V_{tp}	0.5V	0.7V	0.5V	$\pm 10\%$
V_{tn}	-0.5V	-1.0V	-0.5V	$\pm 10\%$
t_{swp}	105ps	10ns	10ns	$\pm 5\%$
t_{swn}	120ps	$1\mu s$	10ns	$\pm 5\%$

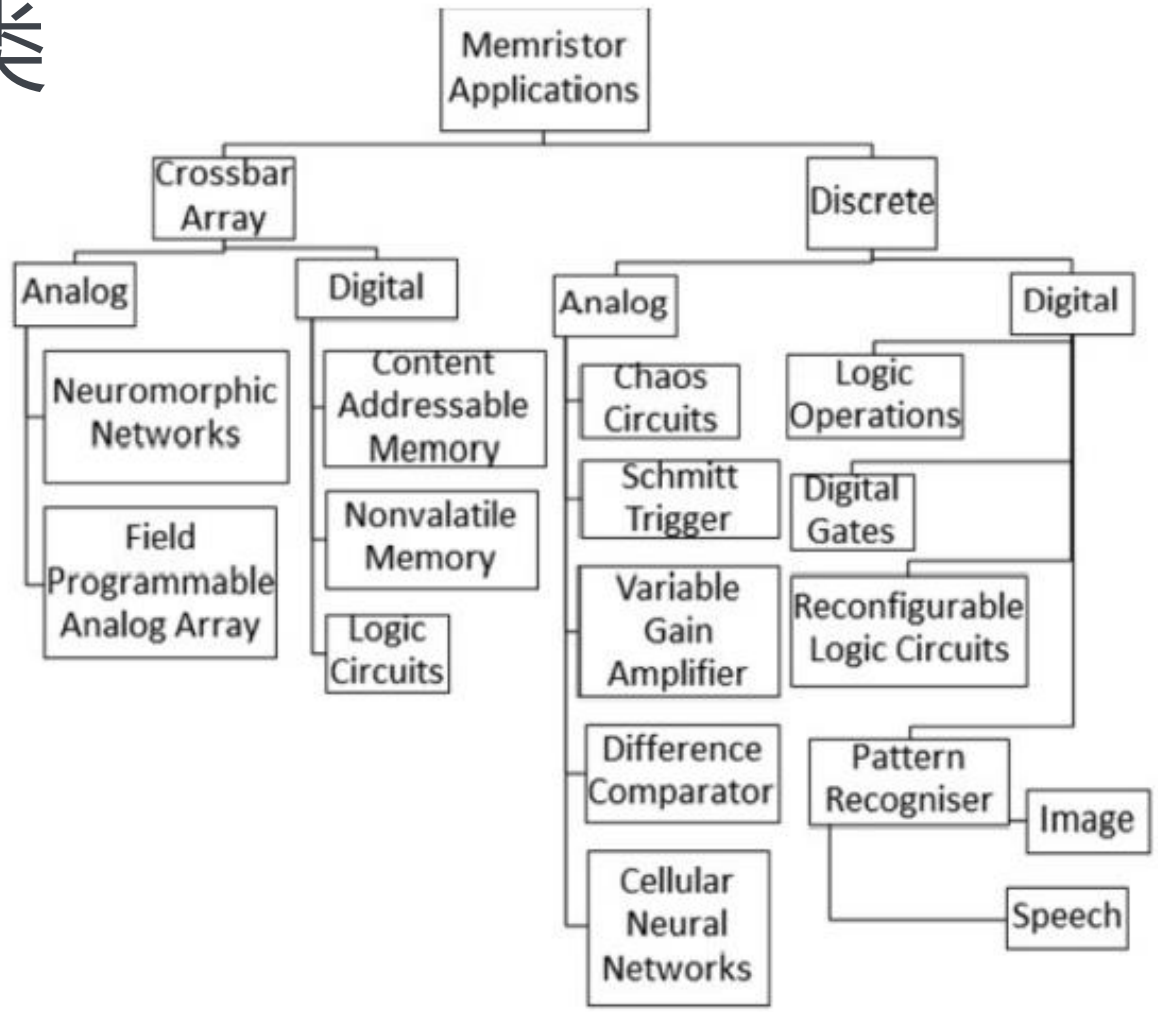
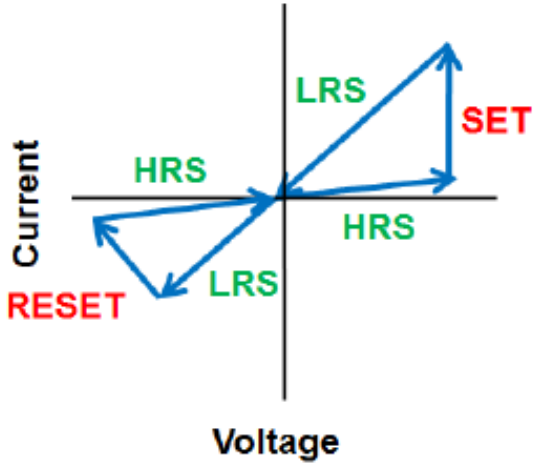


Fig. 3. Modified taxonomy of memristor circuit applications from that reported in [62] to the incorporating emerging applications such as in imaging and speech.

忆阻器（Memristor）的工作状态

- Forming
  - 忆阻器件要想实现高低阻态切换的功能,必须在这之前对其进行一次激发阻变材料的操作,这个激发操作之后,忆阻器件才具有正常的忆阻特性
- SET
  - 忆阻器由高阻态(HRS “0”)转变到低阻态(LRS ”1”)的过程
- RESET
  - 忆阻器由低阻态(LRS ”1“)转变到高阻态(HRS ”0“)的过程



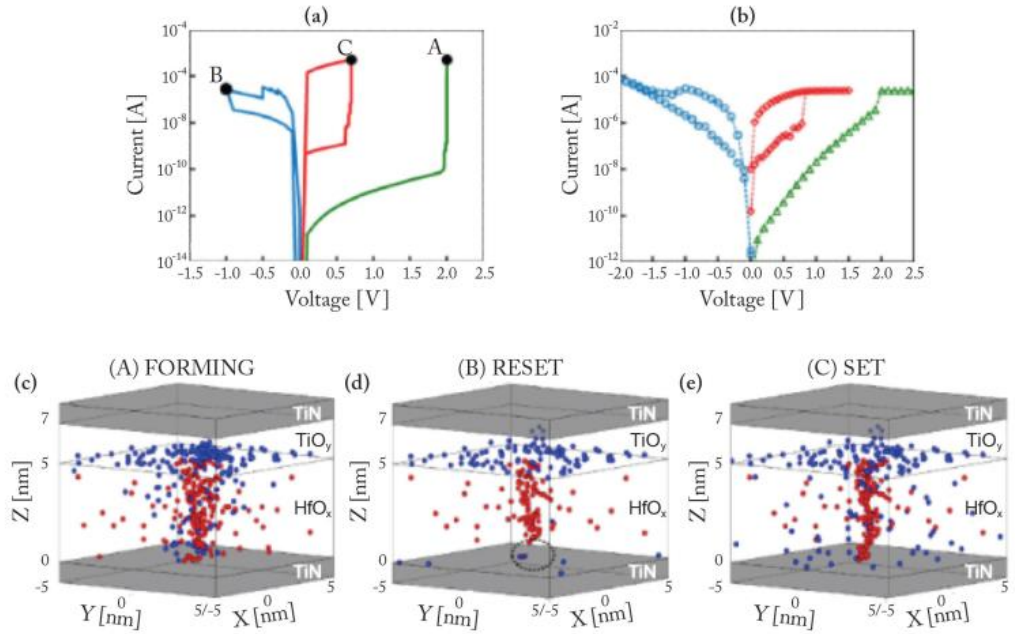
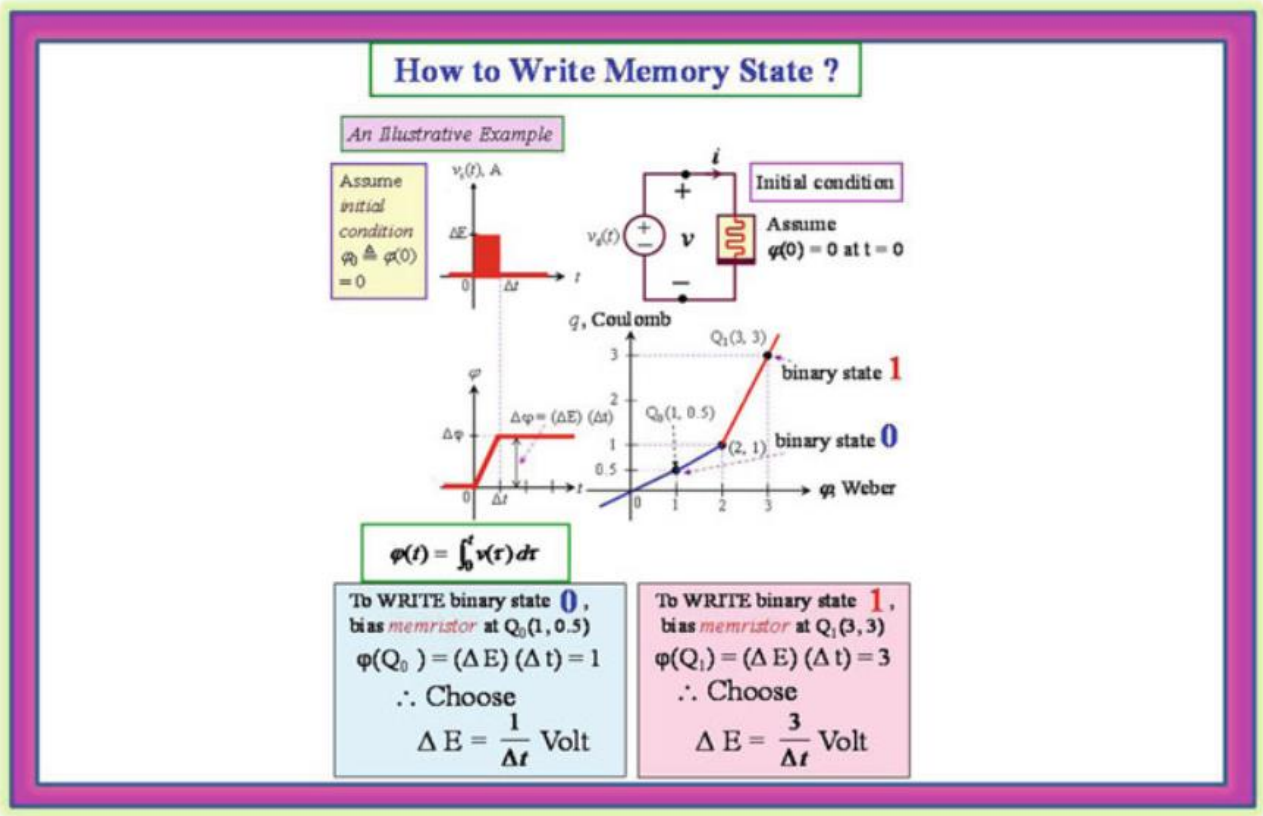
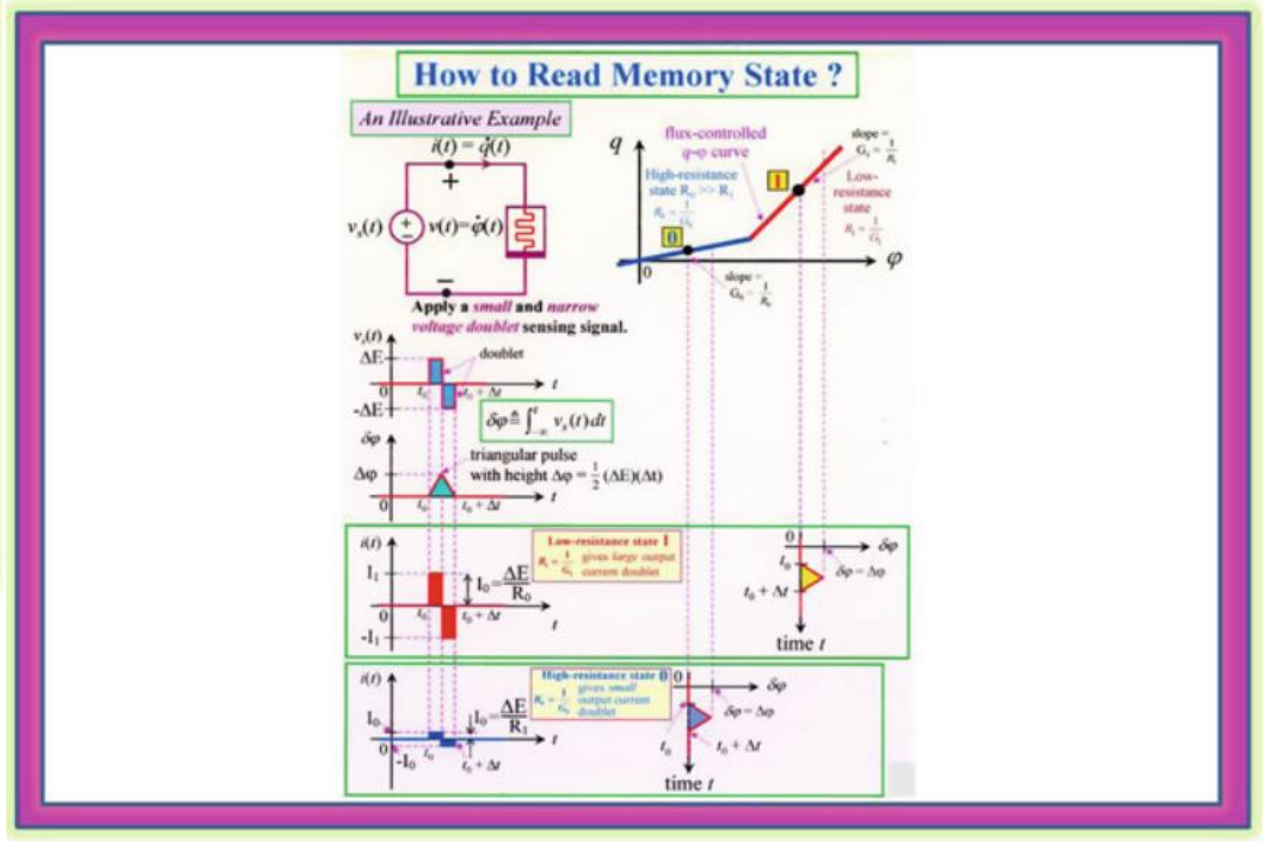


Figure 3.8: Simulated forming-reset-set process for a TiN/Ti/HfO_x/TiN RRAM device using the 3D KMC simulator. (a) Simulated (b) experimental I-V characteristics. Vo (red) and O^{2-} (blue) distributions at the end of (c) forming, (d) reset, and (e) set operations. Adapted from [64].

忆阻器的读写


How to Write Memory State ?
An Illustrative Example
Assume initial condition $\varphi_0 \triangleq \varphi(0) = 0$
Initial condition
Assume $\varphi(0) = 0$ at t = 0
q, Coulomb
binary state 1
binary state 0
φ, Weber
$\varphi(t) = \int_0^t v(\tau)\,d\tau$
To WRITE binary state 0, bias memristor at $Q_0(1, 0.5)$
$\varphi(Q_0) = (\Delta E)(\Delta t) = 1$
∴ Choose
$\Delta E = \frac{1}{\Delta t}$ Volt
To WRITE binary state 1, bias memristor at $Q_1(3, 3)$
$\varphi(Q_1) = (\Delta E)(\Delta t) = 3$
∴ Choose
$\Delta E = \frac{3}{\Delta t}$ Volt

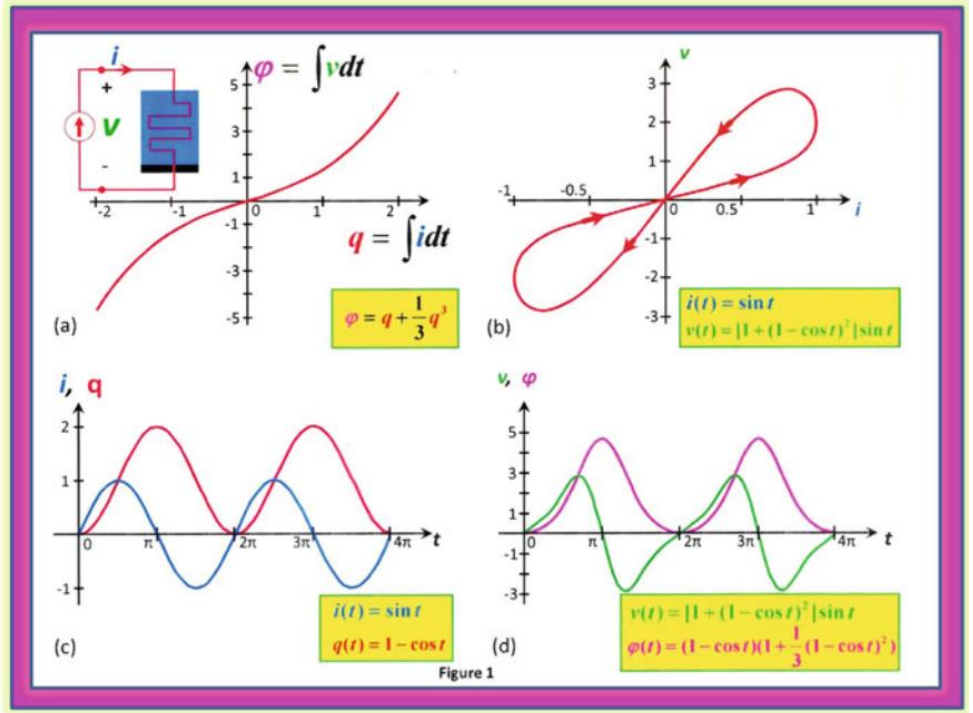

How to Read Memory State ?
An Illustrative Example
flux-controlled φ-q curve
High-resistance state
Low-resistance state
Apply a small and narrow voltage doublet sensing signal.
doublet
triangular pulse with height $\Delta\varphi = \frac{1}{2}(\Delta E)(\Delta t)$
Low-resistance state 1
High-resistance state 0
time t

忆阻器测试方案

忆阻器研究面临的挑战

- 研究方面
  - 机理不清
  - 涨落大
  - 可靠性不足
  - 工艺集成问题
  - 模拟阻变特性优化

- 测试表征方面
  - **RRAM器件**
    - ✓ 瞬态测量
    - ✓ 循环次数测试
    - ✓ 微观原位表征
  - **RRAM阵列**
    - ✓ 自动测试方法
    - ✓ 读取速度



- **RRAM表征技术需要向极端化发展**
  - 原子级的原位表征
  - **ps级脉冲擦写及信号捕捉**
  - 快速读写阵列单元
  - 大规模阵列的自动测试

忆阻器测试流程

01

Forming

验证 Forming 前后的电阻。 通常没有特殊的测试步骤，一般与 Cell IV 特性测试结合在一起

02

Cell I-V-t characterization

测试 set/reset HRS/LRS I-V 特性, 忆阻器的基本测试

03

High speed pulse testing 高速脉冲测试

用不同的 Erase/ Program或 SET/RESET 脉冲序列进行读写测试

04

Data Retention 数据存留测试

数据保存后，在不同的环境条件（温度，湿度等）下，持续读出，测试忆阻器单元保存数据的持久力

05

Cell Endurance 循环次数测试

高频率写 (set/reset)，持续读，验证忆阻器单元可以耐受的读写次数

01 02 **为关键且必需的测试步骤**
- 忆阻器初级研发必需

03 **为极限测试步骤**

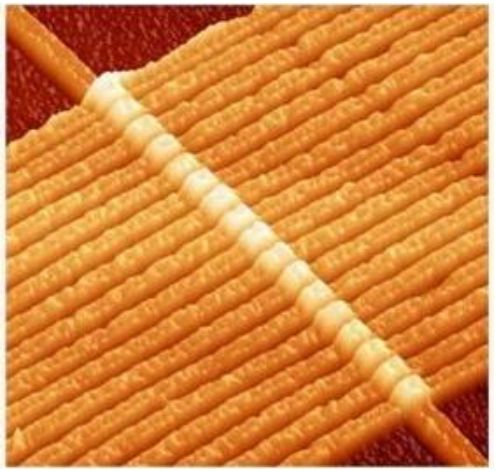
04 05 为深入研发测试步骤

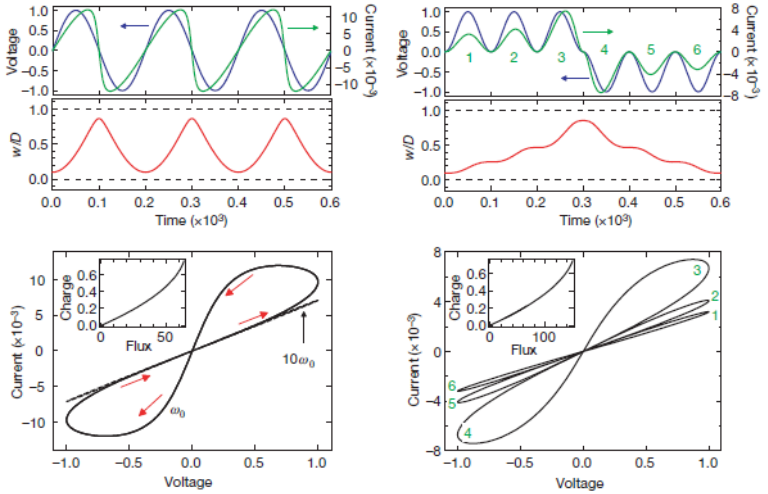
01 02 Device Cell I-V-t 特性测试

- I-V-t 测试条件
  - 1x SMU, Opt. 1x PMU
  - $V_{Set/Reset}$ @<10V, I @>nA 量程, t @>50ns 间隔
  - I-V Sweep, Opt. Pulsed I-V

- 解决方案
  - HW: 参数分析仪
    - 4200A-SCA
    - 4200-SMU
    - 4225-PMU
    - Manual Probe Station
    - SW: Clarius
  - 低成本 HW: SMU
    - 26xx 带脉冲功能
    - 简易探针
    - Kick star 或自行编程

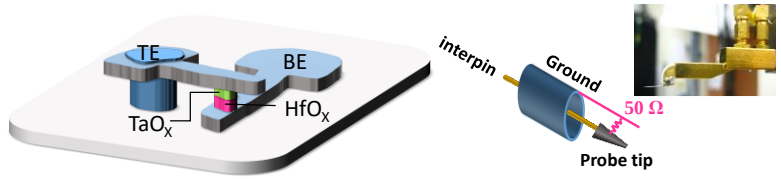
Type of analog RRAM	Ag:a-Si [2]	TaO_x/TiO_2 [3]	PCMO [4]	$AlOx/HfO_2$ [5]	ETML/HfO_x (0.8mΩ·cm)	ETML/HfO_x (4.4mΩ·cm)	ETML/HfO_x (30.4mΩ·cm)	ETML/HfO_x (2 parallel)	Ideal analog RRAM
Nonlinearity (SET)	2.40	0.66	3.68	1.94	0.96	0.93	0.04	0.08	0
Nonlinearity (RESET)	-4.88	-0.69	-6.76	-0.61	-3.26	-2.63	-0.63	-0.63	0
On-state resistance	26 MΩ	5 MΩ	23 MΩ	17 KΩ	10KΩ	30kΩ	100kΩ	50kΩ	High
ON/OFF ratio (analog region)	12.5	2	6.8	4.4	10	10	10	10	Large
SET pulse	3.2V/300μs	3V/40ms	2V/1ms	0.9V/100μs	1.7/50ns	1.5V/50ns	1.6V/50ns	1.6V/50ns	Low voltage Fast speed
RESET pulse	2.8V/300μs	3V/10ms	2V/1ms	1V/100μs	1.5V/50ns	1.5V/50ns	1.5V/50ns	1.5V/50ns	Low voltage Fast speed
Variation	3.5%	<1%	<1%	5%	3%	3.35%	3.7%	1.5%	0%





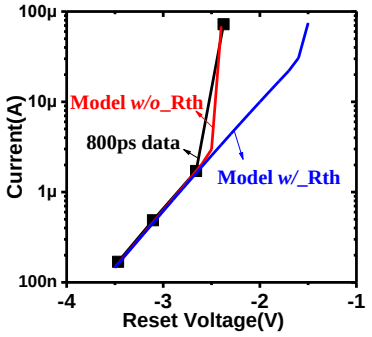
03 Device 高速脉冲 Set/Reset

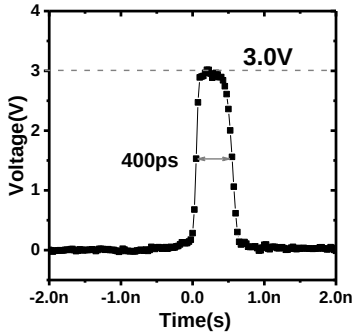
Adv. Ele. Mater. 2017

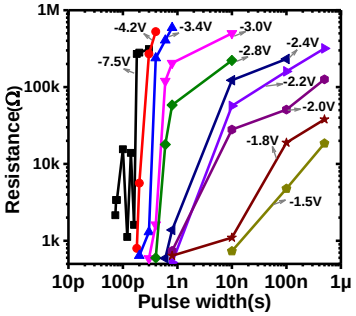


- 高速脉冲 Set/Reset
  - Device 速度性能
  - 通过加长 set/reset 时间去除自热效应

解决方案	~50ns 脉宽 高性价比	<1ns 脉宽 高速（需配放大器）	3ns 脉宽 低成本
硬件	4200A-SCS, 4200-SMU, 4225-PMU	AWG5200/70K MSO/DPO70000	AFG31000/ 4系示波器 5系示波器 6系示波器
软件	Clarius	Customized SW	Customized SW
脉宽 Typ.	70ns @ 10V, 200mA range	<1ns	80ns(AFG3102X) 20ns(AFG3125X)
最小脉宽	20ns	200ps（AWG5200), 20ps(AWG70K)	16ns(AFG3102X) 6ns(AFG3125X)
脉冲输出幅度	10V	0.75 Vp-p(AWG5200) 0.5 Vp-p(AWG70K)	4 Vp-p 50Ohm 8Vp-p 高阻
读取速度	200MSa/s	100GSa/s	依示波器型号
TIA	N/A	Opt. from FEMTO	N/A







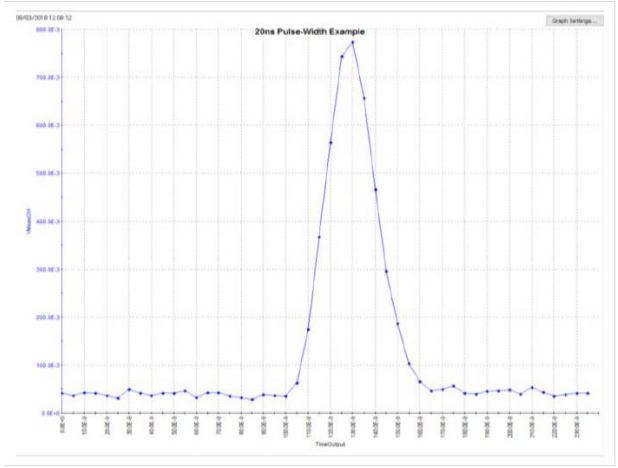
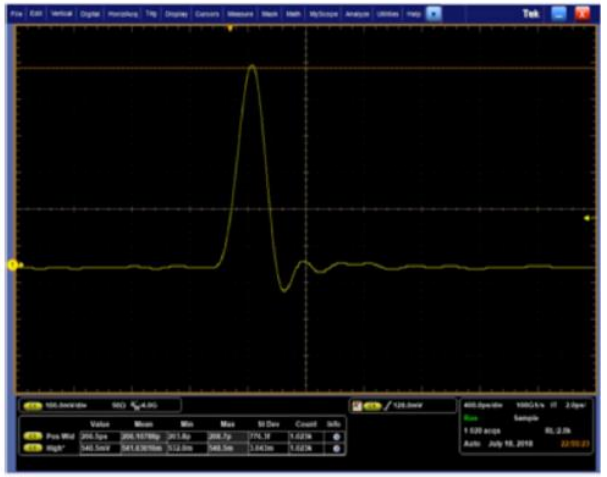


Figure 4: Measurement taken at 5 ns sample interval with the PMU.

KEI 4225-PMU
- Min 20ns pulse generating
- Fast 200MSa/s (5ns interval) Reading

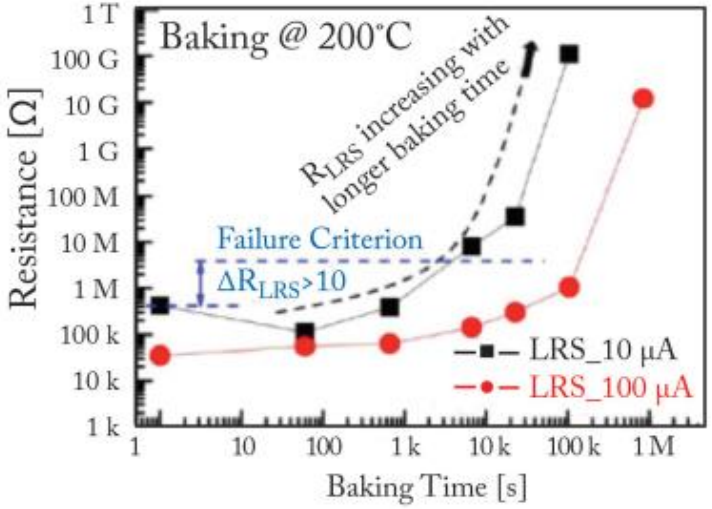
200 ps Write1 Pulse Width

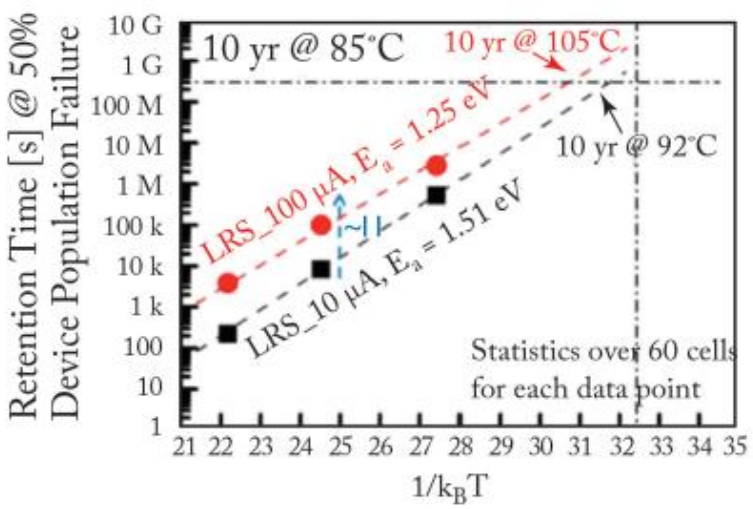


TEK AWG5200,/70K MSO/DPO70000
- Min 200ps pulse generating
- Fast 100GSa/s (10ps interval) Reading

04 数据存留测试 Device Retention Test

- 数据保存后，在不同的环境条件（温度，湿度等）下，持续读出，测试忆阻器单元保存数据的持久力
- 复杂的循环序列，需要反馈环路控制
- 需定制软件





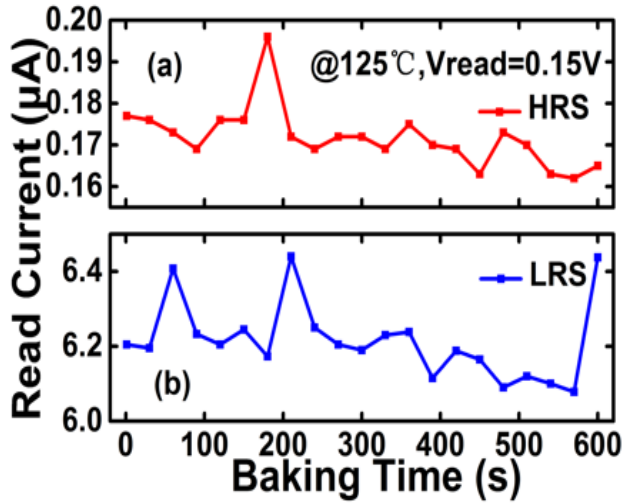
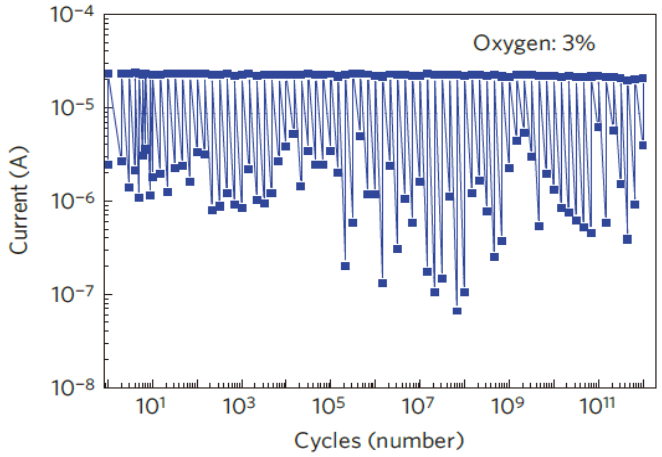


Figure 2.9: (a) Temperature-accelerated retention test for IMEC's HfO_x-based RRAM at 200°C (b) Arrhenius plot of retention time to failure at three temperature 250°C, 200°C, and 150°C. An activation energy (Ea~1.5 eV) was extracted for cells with compliance current = 10 µA. Adapted from [44].

05 循环次数测试 Cell Endurance Test

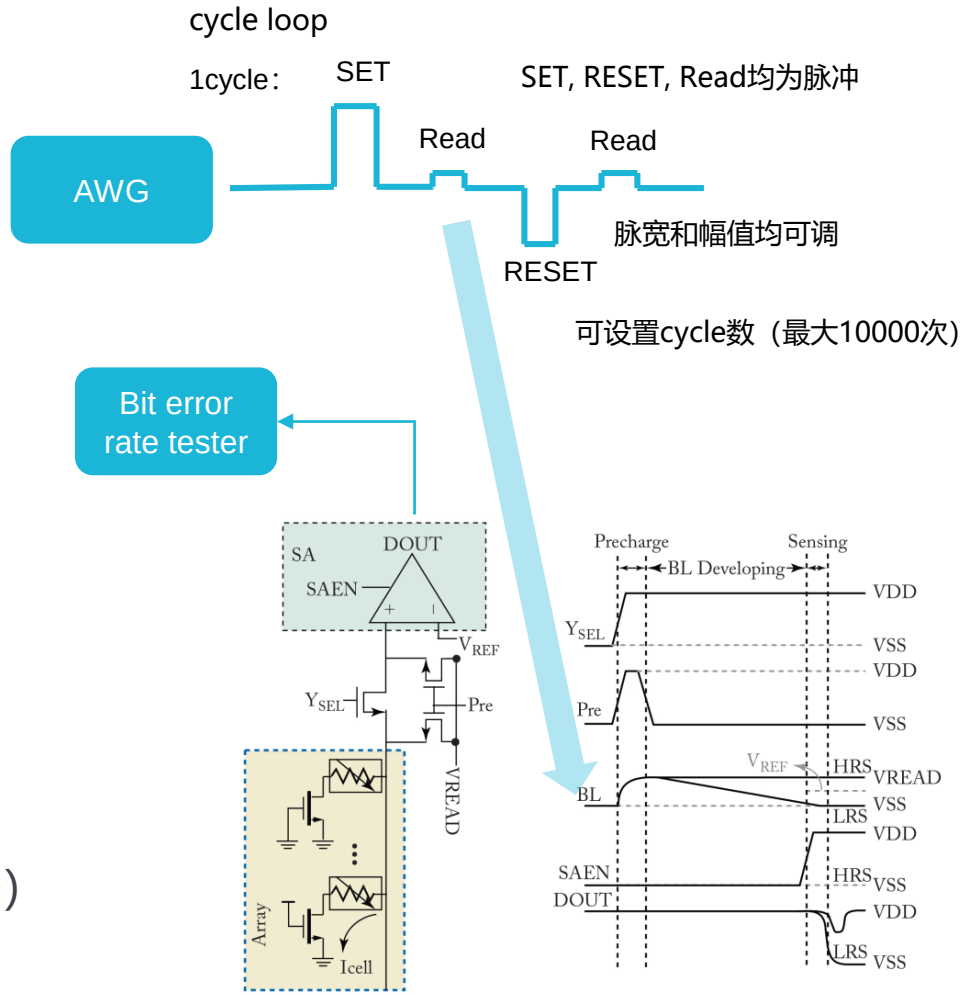
- 高频率写 (set/reset)，持续读，验证忆阻器单元可耐受读写次数
  - 维持 HRS 和 LRS 的比率
- Set/Read/Reset/Read 循环.
  - 复杂的循环序列，需要反馈环路控制
  - 需定制软件
- 验证误码率 BER (数字模式) 或者 LRS/HRS 的变化
- 外部电路匹配 I_{sense} 或者 V_{sense} 连接到测试仪器，如BSX320 误码仪
- 每次读写切换消耗大量的时间。
  - 要准确评估器件的循环次数（endurance），需要对每次擦写后的电阻进行读取，单器件需要10^{12}以上的切换。
  - 阵列上则需要10^{18}以上的读写次数。



05 循环次数测试 Cell Endurance Test

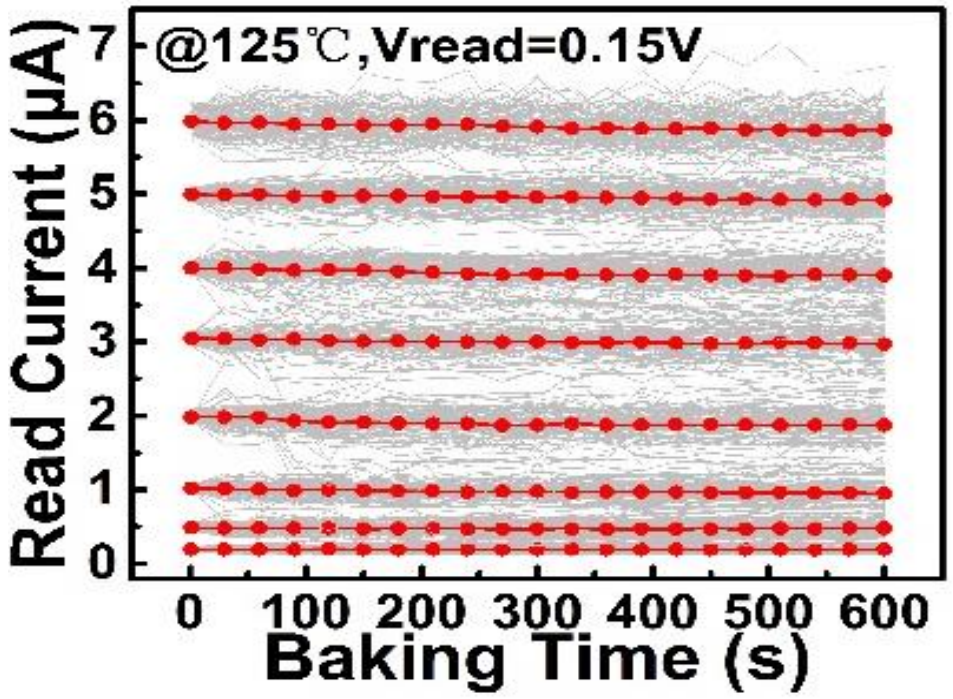
- RRAM 循环读写
  - Set/Reset
  - Pulse Set/Reset
  - Memory Retention, long time pulse

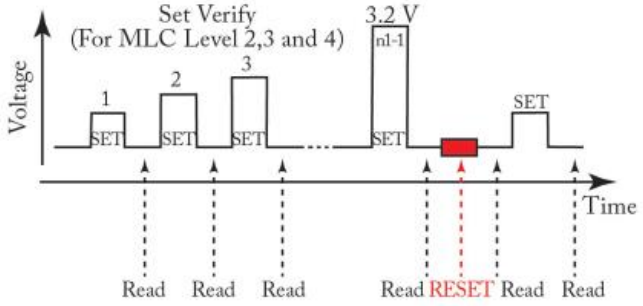
- 方案:
  - HW: Parameter Analyzer
    - 4200A-SCA
    - 4200-SMU
    - 4225-PMU
    - Manual Probe Station
    - AWG 做极限脉冲测试
    - BSX320 做误码测试（需外接匹配电路）
  - SW: Clarius w/ 定制化软件

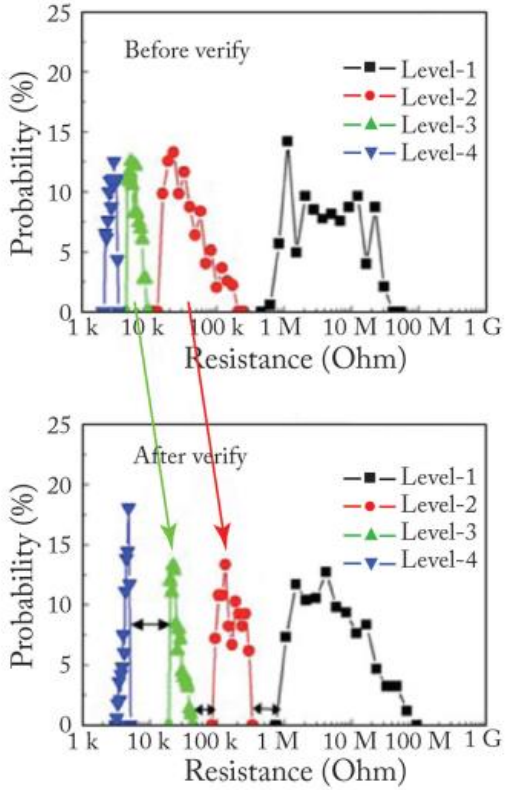


多值忆阻器测试

- 确保多值电阻的比率
- 循环执行多值 Set/Read 对设置多值电阻
- 极其复杂的序列，需要反馈环路控制



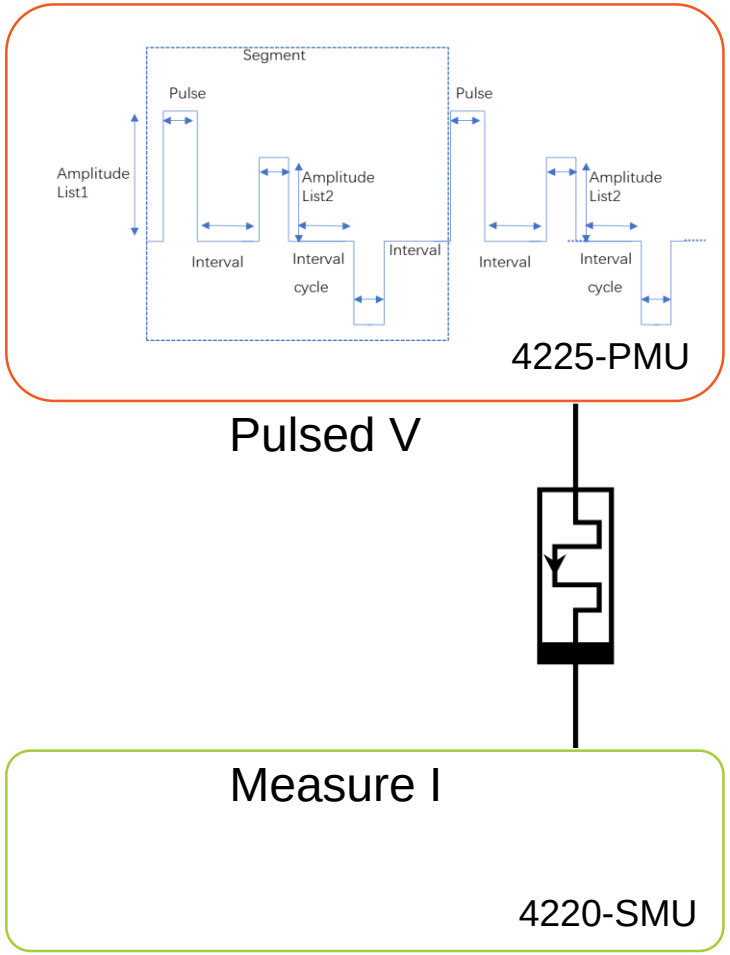


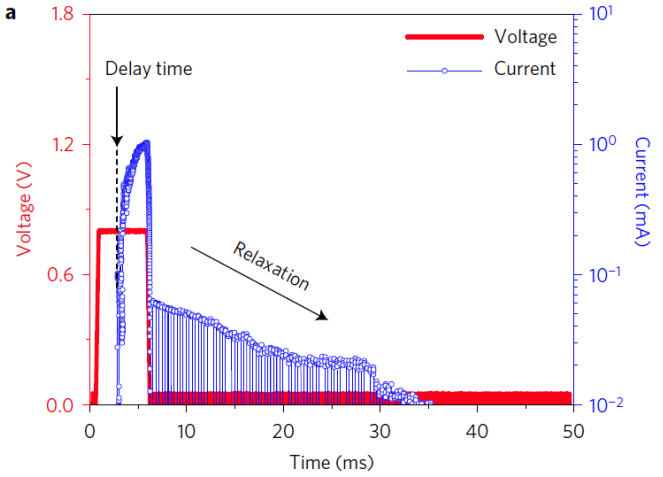


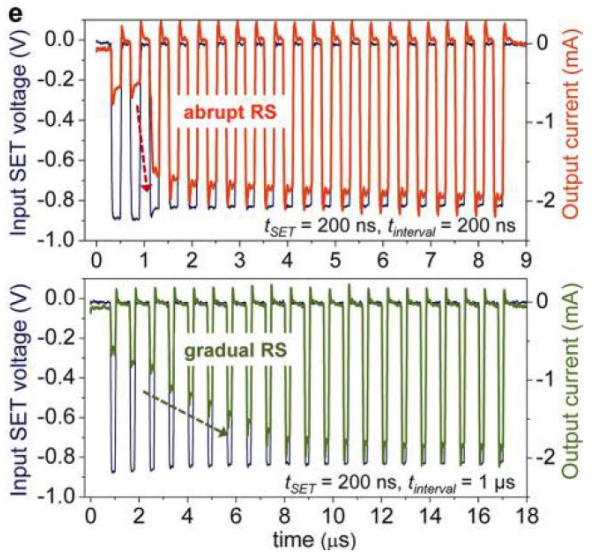
Device Resistance Dynamics Test

阻变动力学测试

- 神经突触特性
- 用脉冲 I-V-t, 降低自热
- 方案
  - HW: 半导体参数分析仪
    - 4200A-SCA
    - 4200-SMU
    - 4225-PMU
    - Manual Probe Station
  - SW: Clarius w/ 定制化软件





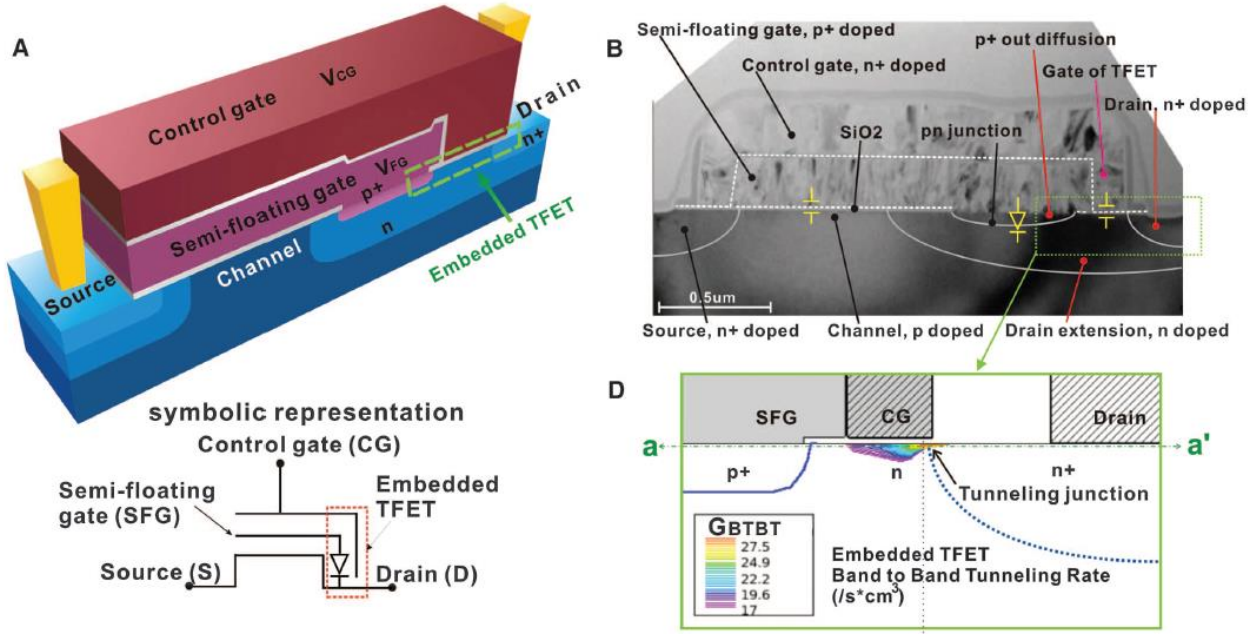


Z. Wang, et al, Nature Materials, 2017
C. Du et al, Nano Letters, 2015, 15, 2203

半浮栅晶体管测试方案

半浮栅晶体管

- 与忆阻器一样，是新一代高速存储单元
- 由复旦大学张卫教授团队于2013年首先研发出来
- 巧妙地通过一个隧穿二极管（TFET）把浮栅和漏极连起来，用隧穿二极管来控制浮栅的充放电，从而构成了一个动态存储器。
  - 速度快、面积小、低功耗，且与标准 CMOS工艺兼容，不需要集成新材料。



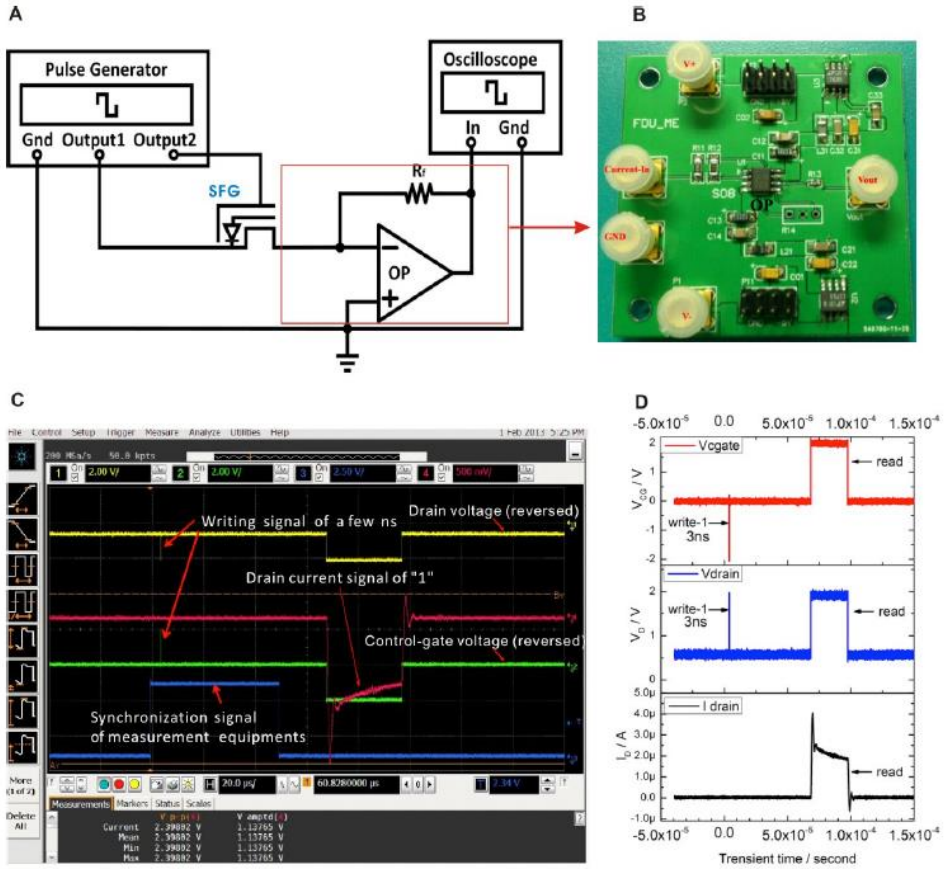
Public at SCIENCE VOL 341 9 AUGUST 2013

半浮栅晶体管测试挑战

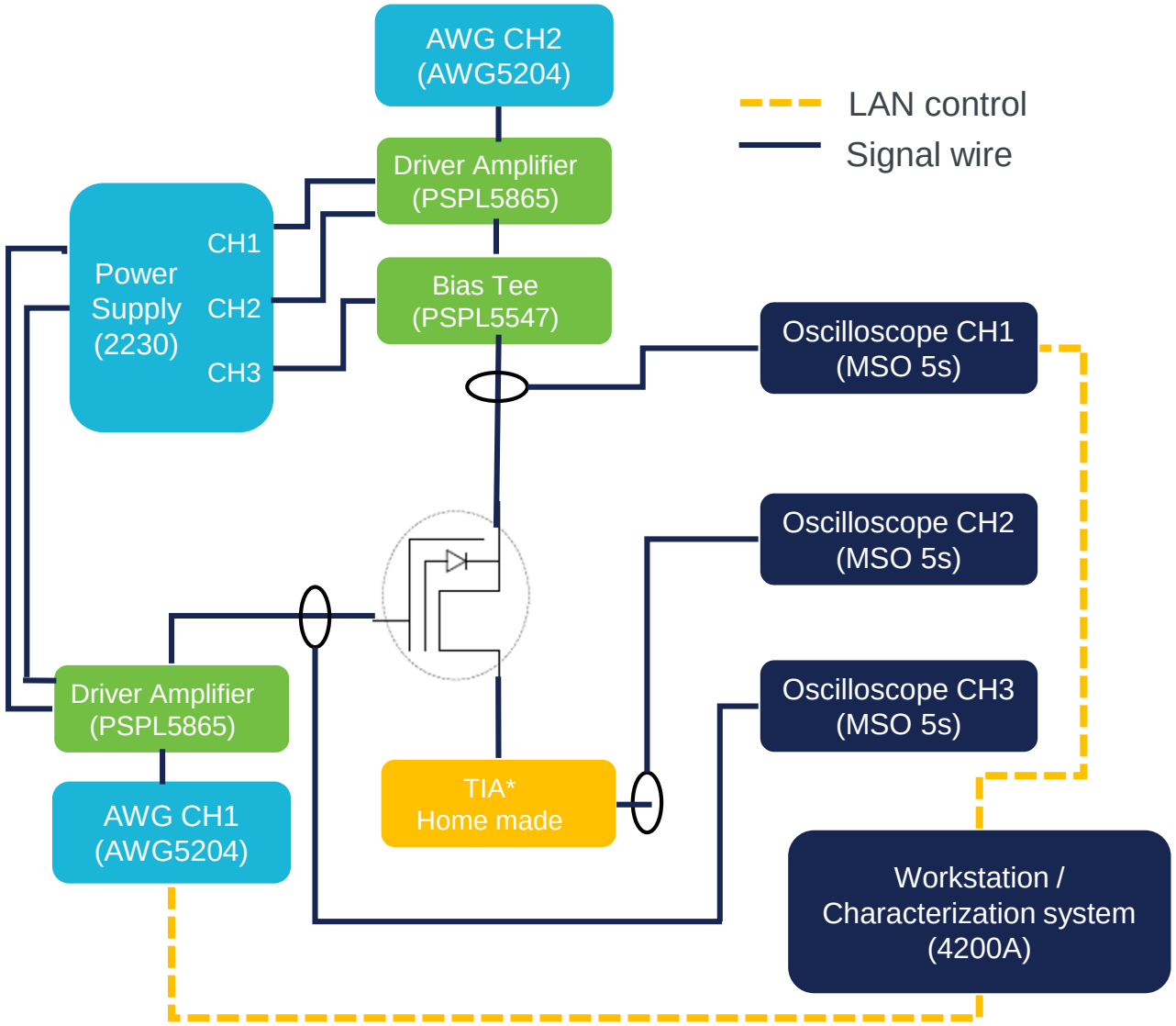
- 本身是一种三极管，同时又具备高速存储特性，
  - 常规的半导体特性参数以及存储器所需的脉冲读写性能都需要

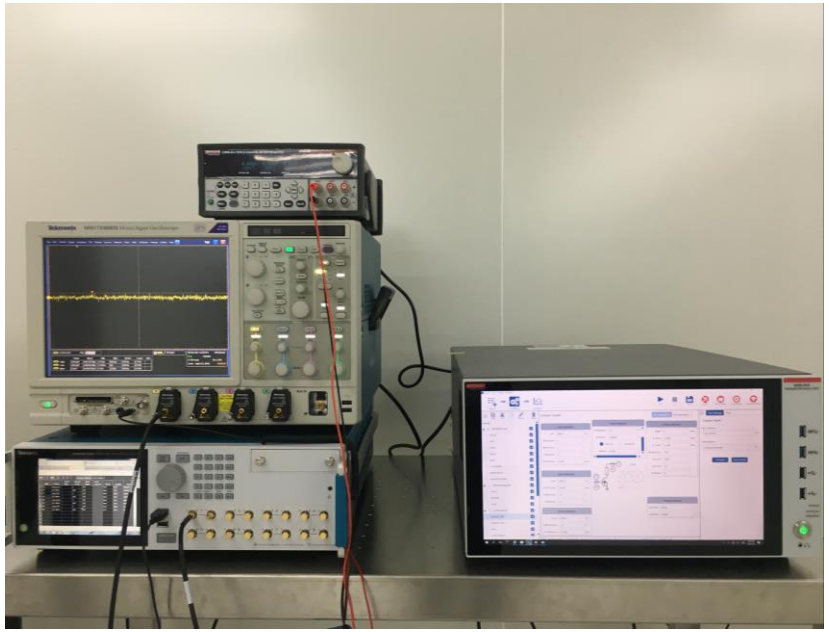
- 半浮栅存储器最突出的特性是速度快，
  - 研发时必须对其高速读写性能进行测试
    - 高速脉冲发生器发出的脉冲宽度需小于1ns，脉冲幅度在1~3V
    - 传统的脉冲发生器无法满足测试需求。

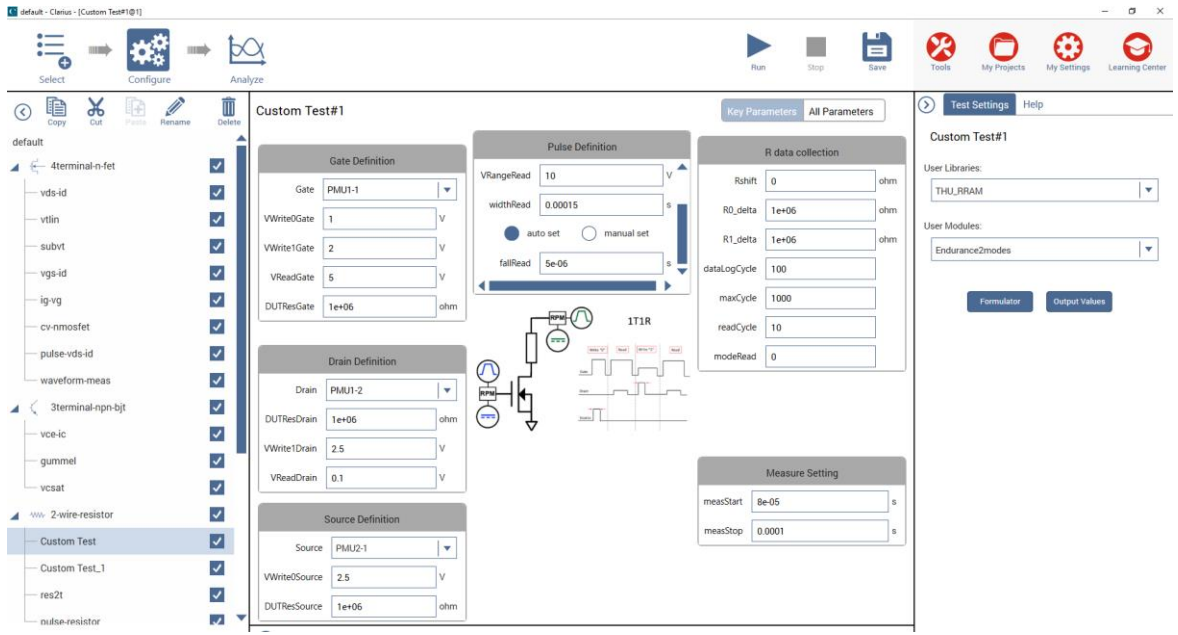
- 测试系统不可能手动操作各台仪器进行测试，必须做相应的系统集成，二次开发定制化软件完成测试。



泰克半浮栅器件测试系统







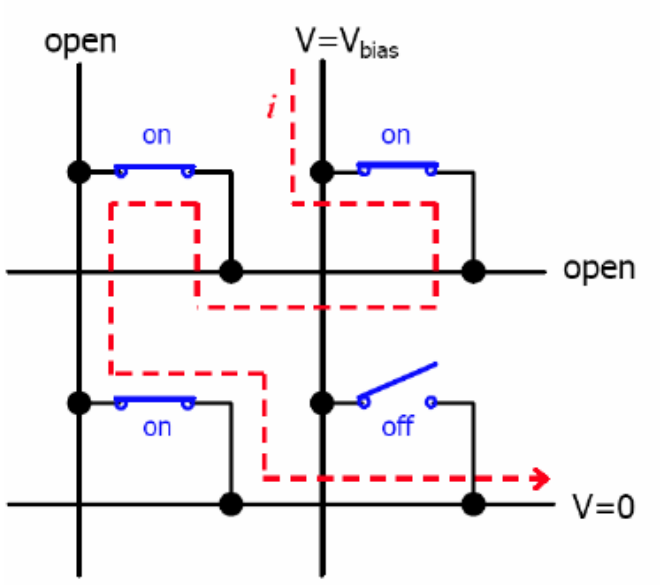
* Transimpedance Amplifier: converting current into voltage

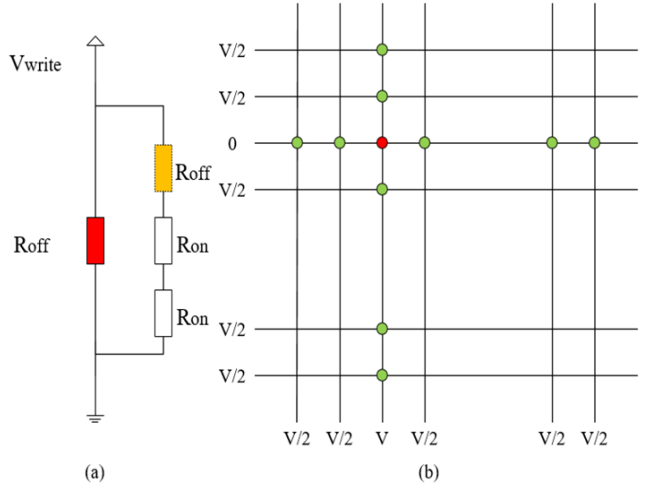
类脑计算/神经元网络测试方案

神经元网络存储阵列测试挑战

通道串扰

- 存储器阵列在操作中存在多种串扰效应，为抑制这些效应，需要对每条BL、WL同时加电压
  - 受器件特性的影响，所加电压可能不同
  - V/2 or V/3-2V/3 to improve the safe write margin
  - 需要开发灵活的阵列测试模块，可以多通道同时加电压。

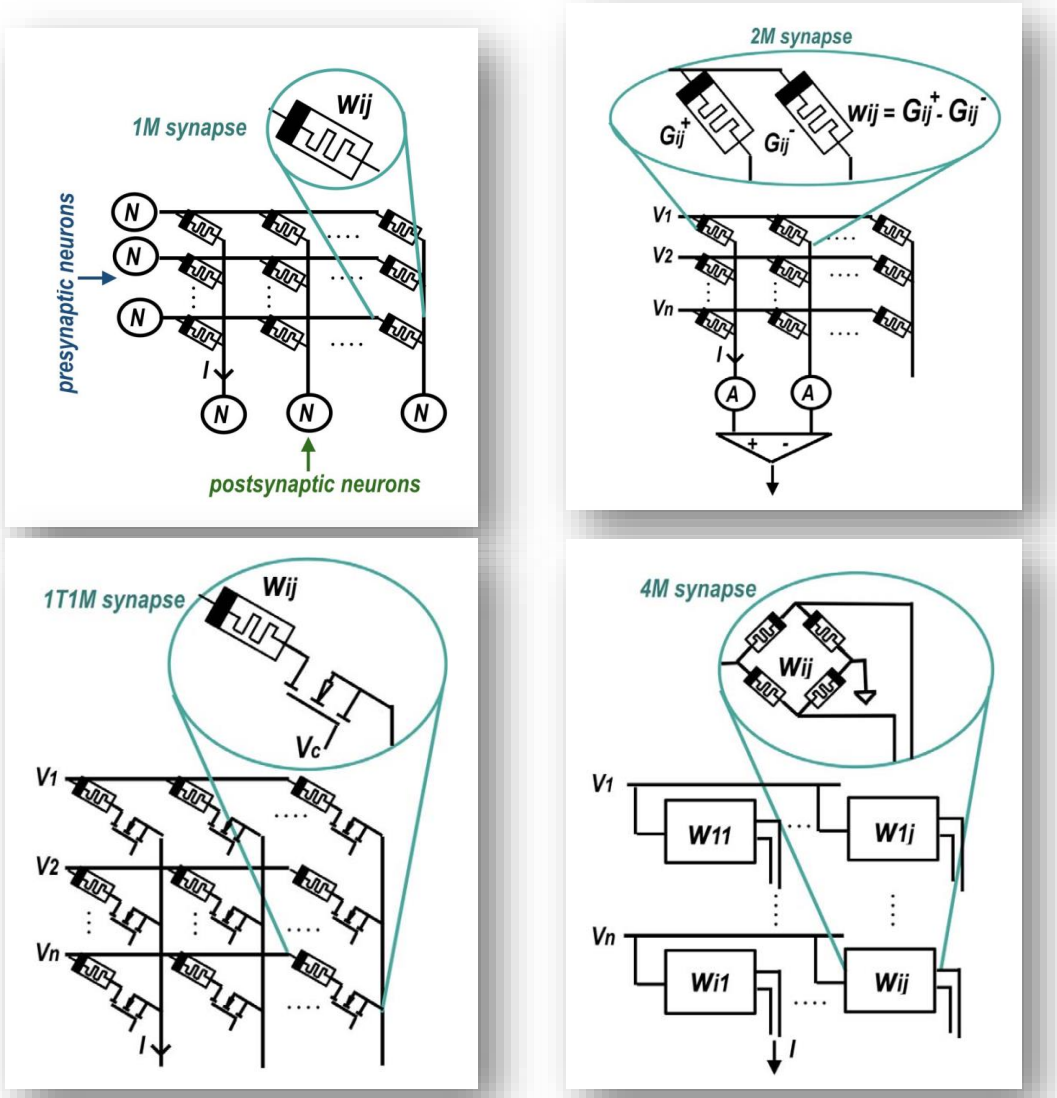




神经元网络存储阵列测试挑战

阵列结构多样

- 阵列节点越多，测试越复杂
  - N X N
- 阵列单元多样，测试连接不同
  - 1M（1个忆阻器）：
    - 无需添加 CMOS 单元
    - 需要额外的控制电路，通道泄露严重
  - 2M （2个忆阻器）
    - Allow negative weight
  - 1T1M（1个晶体管，1个忆阻器）
    - 解决通道泄露问题
    - 引入了复杂的 CMOS 单元
  - 4M （四个忆阻器）
    - Allow to change sign of weight
  - 1T1R (1个半浮栅晶体管，1个电阻)
  - 3T （3个半浮栅晶体管）



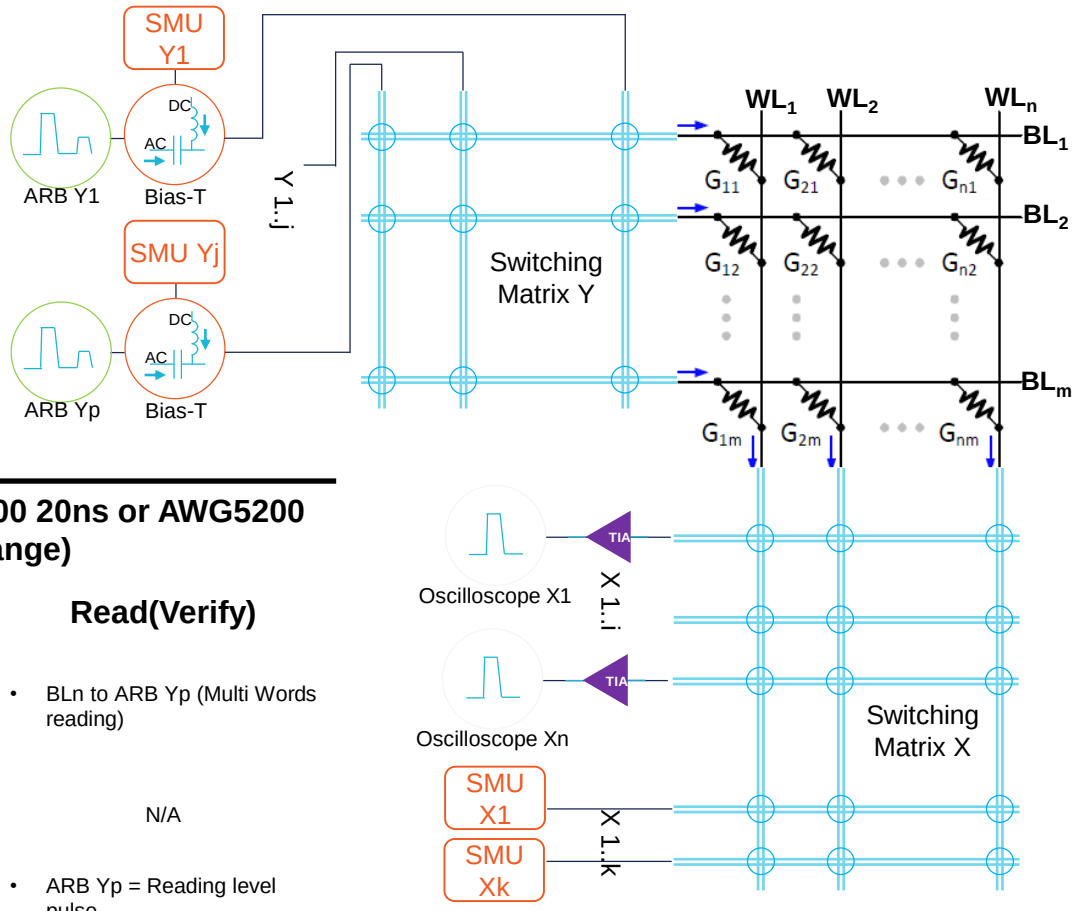
Neuromemristive Circuits for EdgeComputing: A Review

神经元网络忆阻器 RRAM 阵列测试挑战

自动校验与弛豫

- 阻变存储器阵列在擦写过程中需要对每个单元反复校验，以抑制涨落和弛豫效应对tail bits的影响。单器件的测试程序很容易开发，但是阵列级的verify自动测试方法则是未来急需的工具。
- 解决方案

Operations	Low Speed (>150us)		High Speed (AFG31000 20ns or AWG5200 1ns range)	
	Write (Set/Reset)	**Read (Verify)**	**Write (Set/Reset)**	**Read(Verify)**
Switching Matrix Y	• BLn to Pulsed SMU • SMU Yj < BLn, other BLs to SMU(s) = 1/3V	• BLn to Pulse SMU • Single BL for verification • All BLn driving by SMU for inference	• BLn to ARB Yp (single Word write) • Other BLs to SMU(s) = 1/3V	• BLn to ARB Yp (Multi Words reading)
SMU Y	• SMU Yj = Pre Programming Pulse Voltage • Other SMU(s) = 1/3V	• SMU Yj = Reading level pulse	• Other SMU(s) = 1/3V	N/A
ARB Y	N/A	N/A	• ARB Yp = Pre Programming Pulse Voltage	• ARB Yp = Reading level pulse
Switching Matrix X	• WLn to Ground by SMUk • other WLs to SMU(2/3V)	• WLn to SMUk	• WLn to ground by SMUk • Other WLs to SMU(2/3V)	• WLn to Oscilloscope Xn • Single to multi Word reading
SMU X	• SMUk = Ground • Other SMU(s) = 2/3V	• SMUk reading the current for reading result	• SMUk = Ground • Other SMU(s) = 2/3V	N/A
Oscilloscope	N/A	N/A	N/A	• Oscilloscope Xn for Words data reading

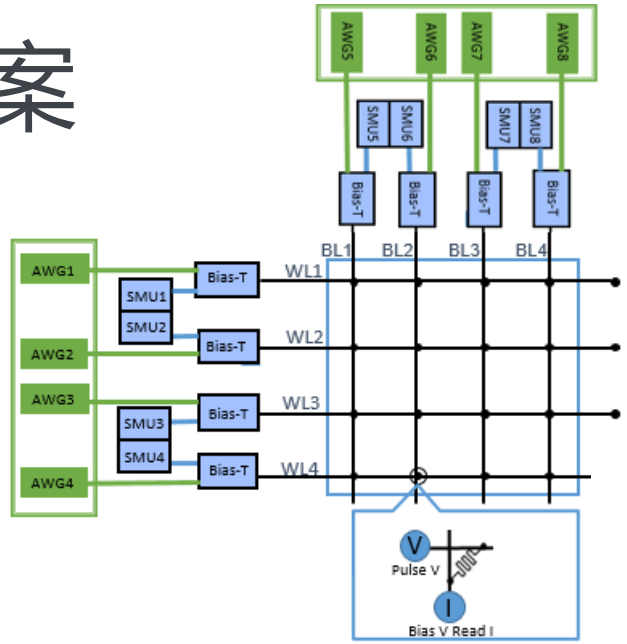


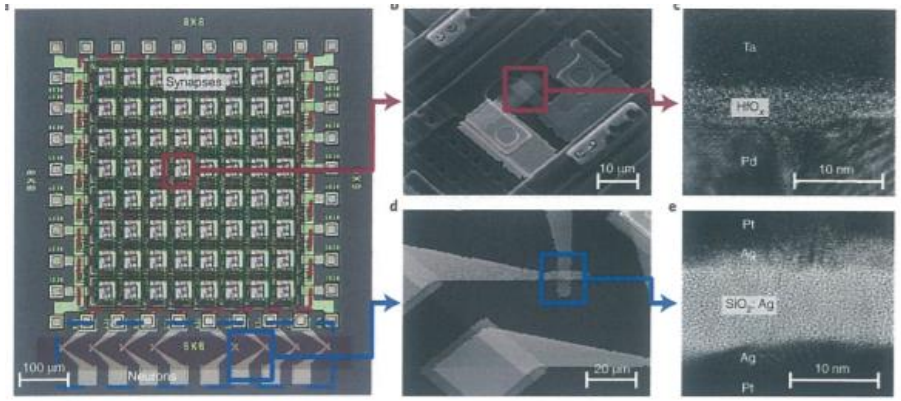
Solution:

- HW: S500 w/ ARB (AFG31000 or AWG5200/70K), 3/4/5/6 Series DSO
- SW: Customized ACS

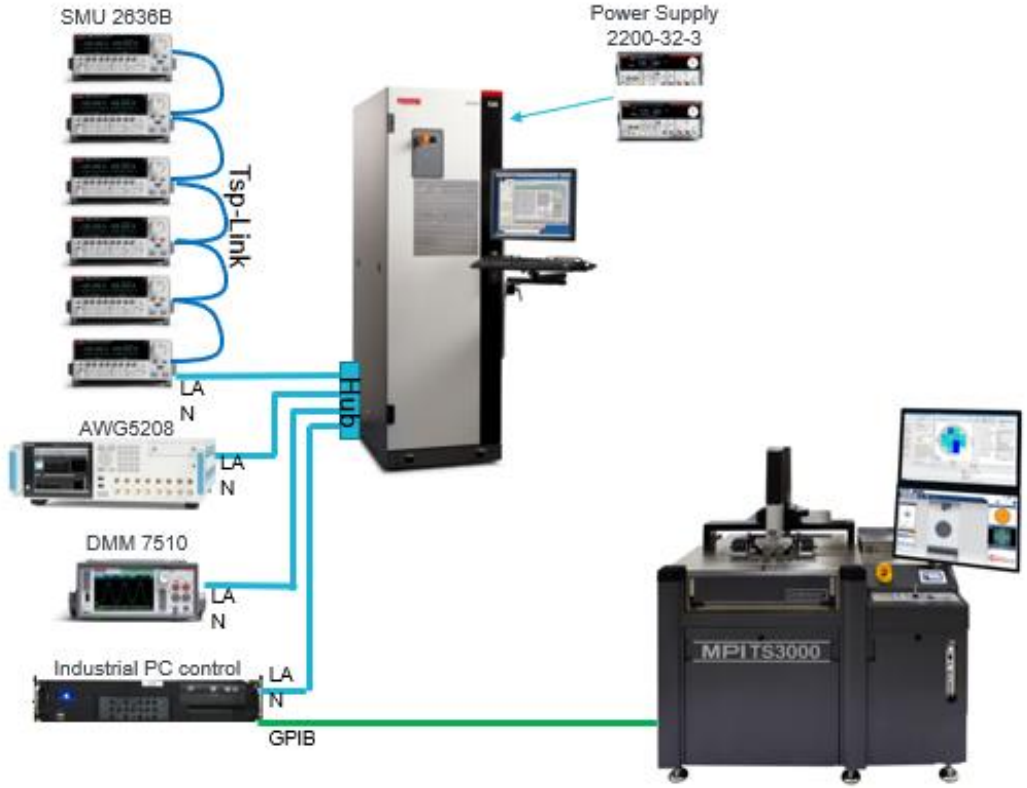
神经元芯片测试方案

- 4X4 晶圆级半自动神经元芯片阵列测试
  - 1M
  - 1T1R Array
  - 3-T Device Array





- 神经元网络特性测试
  - 4路同步输入，4路关联输出
  - 4路输入从亚nS级到mS级定制波形同步触发输入（AWG-SMU）
  - 4路关联小信号输出，用于计算神经元网络的权重特性
  - 同时提供单个神经元的特性分析
    - 读写
    - 数据保持
    - 定制波形反馈



- Solution: S500（AWG5208+SMU*12+DMM*1+Scope*1）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