Tektronix

# Managing the Complexity of PCI Express 5.0 Refclk Measurements

November 2020

# Agenda

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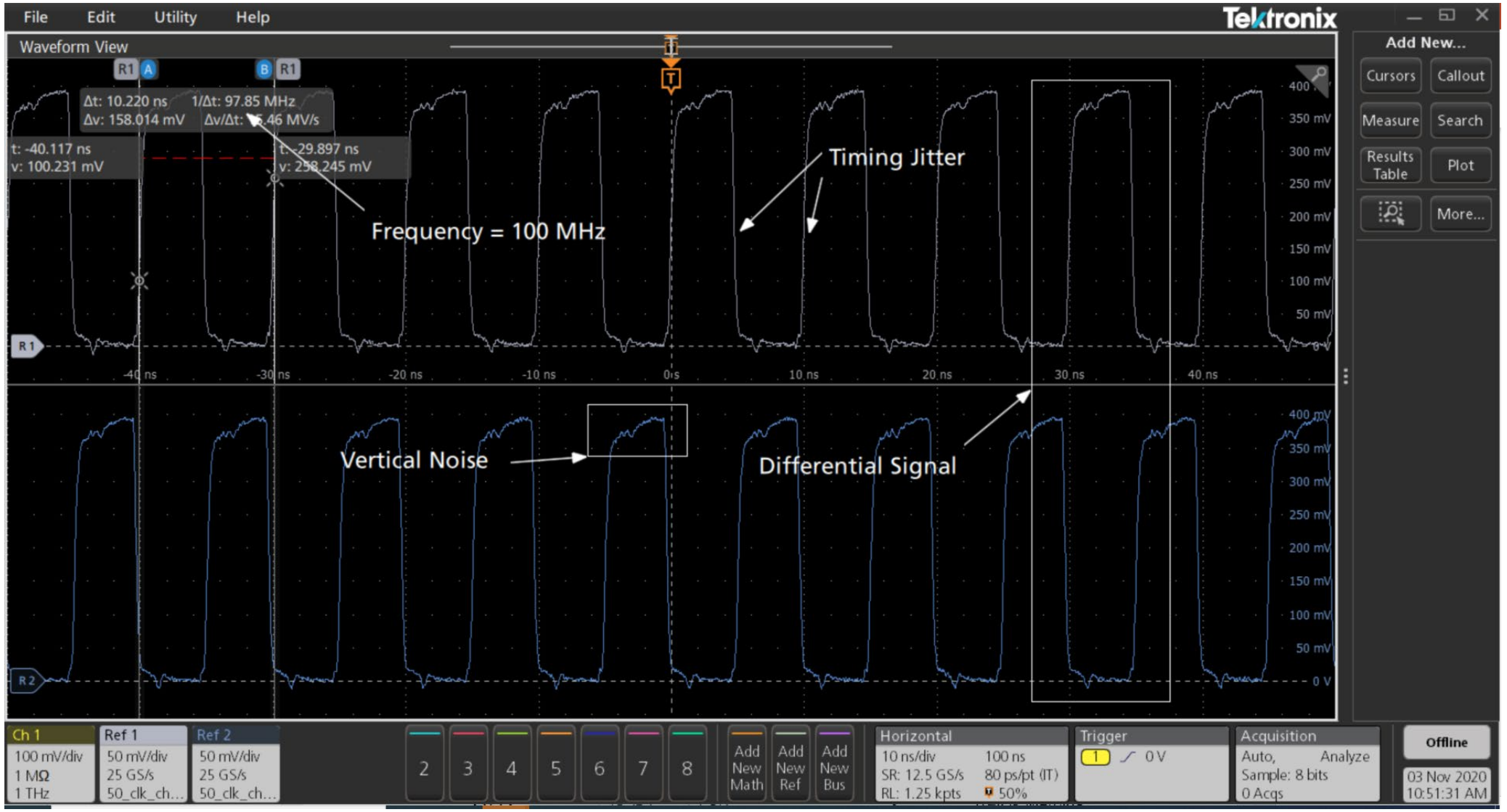
| PCI Express Refclk Basics | PCI Express 5.0 Refclk Jitter Requirements | Evolving Refclk Measurements | Tektronix Refclk Solutions |

# PCI Express Refclk Basics

# PCI Express Refclk Specifications

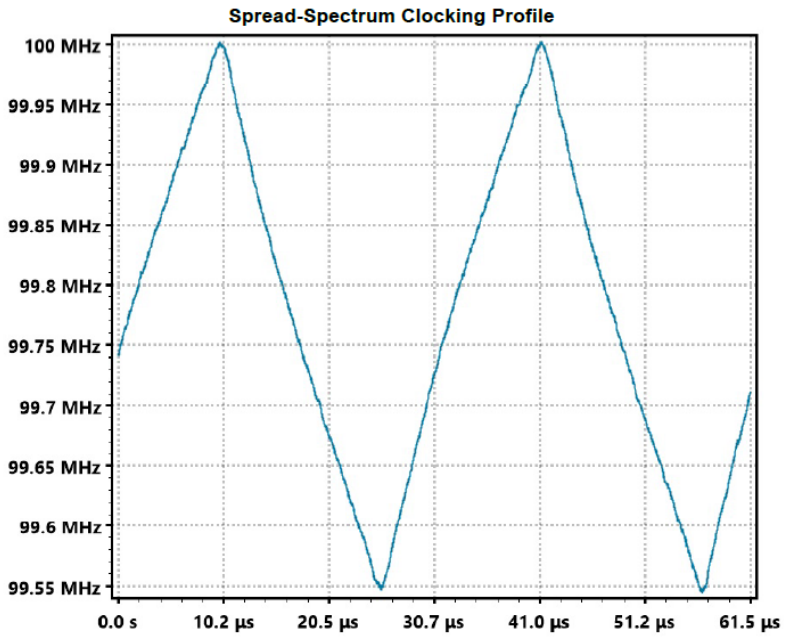
- **PCIe 1.1 / 2.0 / 3.0 CEM Specifications (2005 / 2007 / 2013)**
  - Refclk requirements for 2.5 GT/s
  - Dual Port (data & clock) Tx methodology introduced at 5.0 GT/s
- **PCIe 2.1 / 3.1a  Base Specifications (2009 / 2015)**
  - Refclk requirements introduced for 5.0 & 8.0 GT/s
- **PCIe 4.0 / 5.0 Base Specification (2017 / 2019)**
  - Consolidates 2.5, 5.0, & 8.0 GT/s refclk requirements into one document
- **PCIe 4.0 CEM Specification (2019)**
  - Dual Port (data & clock) Tx methodology for 5.0, 8.0, & 16.0 GT/s
- **PCIe 5.0 CEM Specification (TBD)**
  - Dual Port requirement removed for 32.0 GT/s

# Signal Basics



# Spread Spectrum Clocking (SSC)

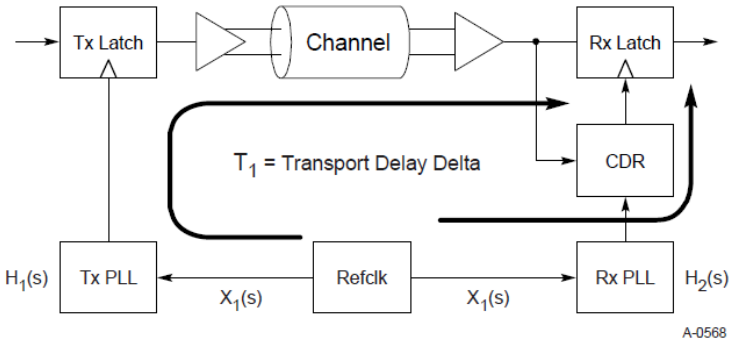
SSC is utilized to spread the radiated electromagnetic energy across a wider frequency band and minimize the potential interference with other electronic devices.




| PCI Express 5.0 SSC Parameters | |
|---|---|
| SSC Frequency Range | 30 to 33 KHz |
| SSC Deviation | -0.5 to 0.0 % UI |
| SSC Deviation (SRIS) | -0.3 to 0.0 % UI |
| SSC Slew Rate | 1250 ppm / us |

- SSC is implemented on the refclk
- Electromagnetic Interference (EMI) reduces on the clock and data routing with SSC
- Most systems have the ability to turn SSC on & off
- No CEM compliance measurement of the SSC parameters up to 32 GT/s
- SSC deviation limit range is reduced when separate refclks with independent (SRIS) is implemented

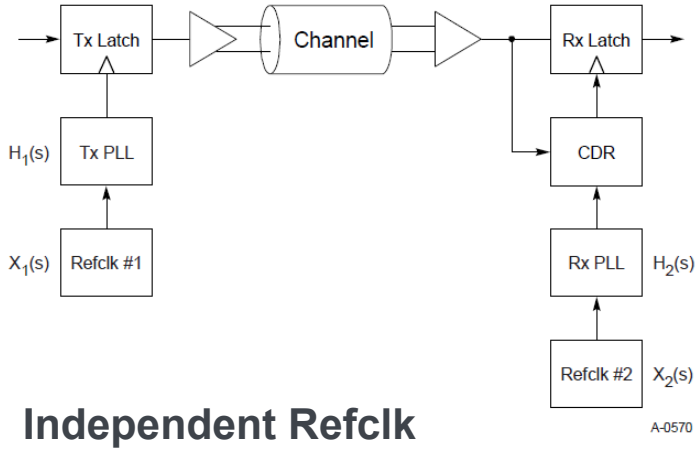
# Clocking Architectures




**Common Clock Architecture (CC)**
Single Refclk distributed to the Tx & Rx

Much of SSC jitter is tracked by the PLLs

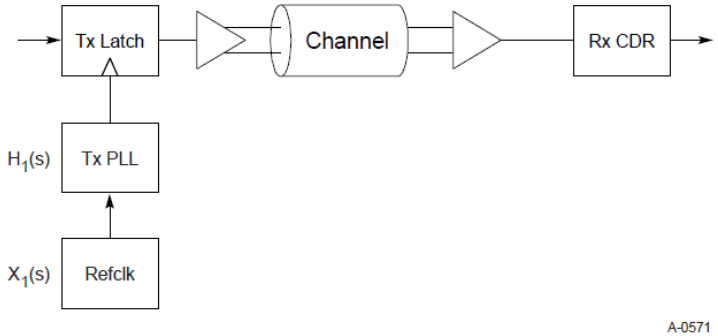
Transfer function defined for noise at the Rx latch (considering PLL combinations, CDR, & transport delay)




**Independent Refclk**
Separate Refclk No SSC (**SRNS**)
Separate Refclk with Independent SSC (**SRIS**)

Jitter at the Rx is the RSS sum of the PLL transfer characteristics & SSC jitter is not tracked

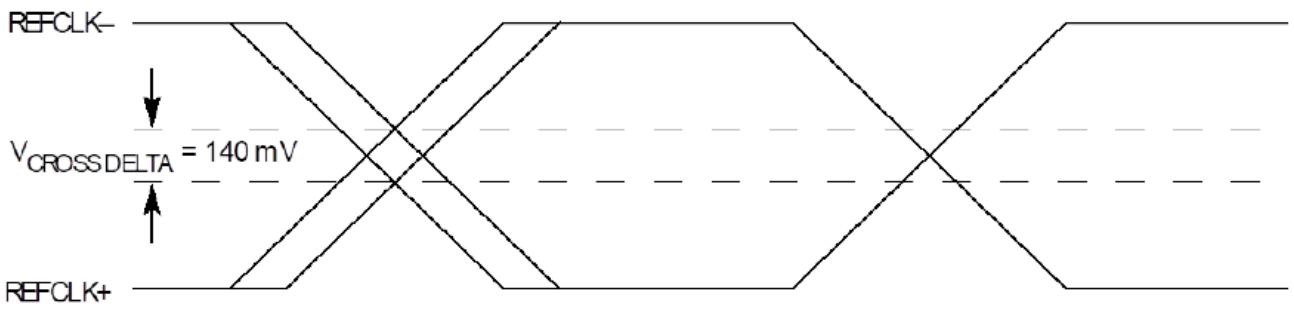
Jitter characteristics for SRNS & SRIS must be considerably tighter

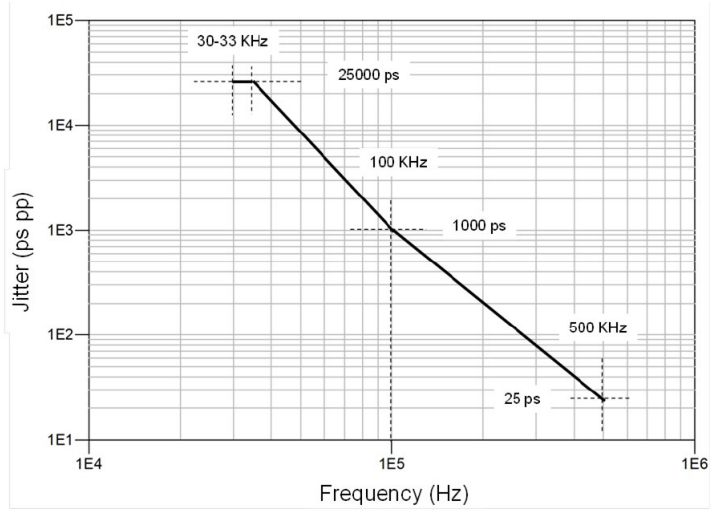



**Data Clocked**
Rx does not use refclk during data recovery

Propagated jitter depends on the maximum PLL bandwidth and CDR must be capable of tracking SSC at a maximum slew rate

# Measurement Categories

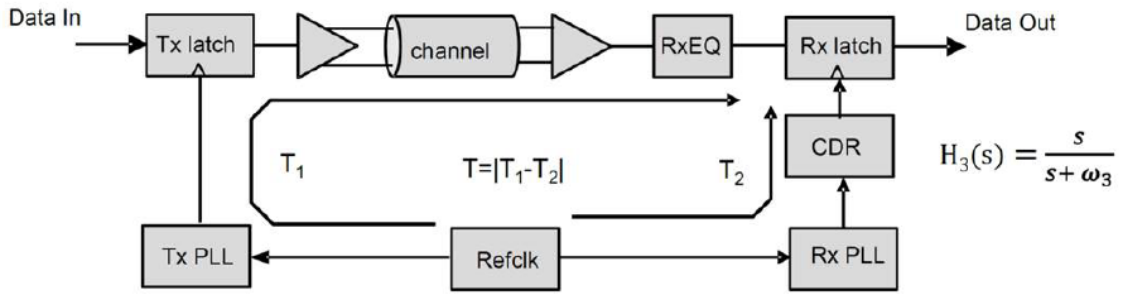



| Categories | Examples | Details |
|---|---|---|
| AC Specifications | Edge Rate, Diff Voltage, Period, Cycle-to-cycle jitter, Duty Cycle, DC Impedance… | Measurements require single-ended & differential waveforms. Pass/fail limits are independent of data rate |
| Data Rate Independent | Refclk Freq, SSC Freq, SSC Deviation, Transport Delay, SSC df/dt, … | Measurements with differential waveforms. Pass/fail limits are independent of data rate. Transport delay only applies to CC |
| Low Frequency Jitter | Low freq jitter mask requirement (above) | Measured from 30KHz to 500KHz |
| High Frequency Jitter | High freq jitter | Limits only provided for CC architecture |

# PCI Express 5.0 Refclk Jitter Requirements

# Common Clock Jitter Requirements




$$H_3(s) = \frac{s}{s+\omega_3}$$

$$H_1(s) = \frac{2s\zeta_1\omega_{n1} + \omega_{n1}^2}{s^2 + 2s\zeta_1\omega_{n1} + \omega_{n1}^2}$$

$$H_2(s) = \frac{2s\zeta_2\omega_{n2} + \omega_{n2}^2}{s^2 + 2s\zeta_2\omega_{n2} + \omega_{n2}^2}$$

Transfer Function: $[H_1(s)e^{-sT} - H_2(s)]H_3(s)$

Jitter at Rx latch: $X(s)[H_1(s)e^{-sT} - H_2(s)]H_3(s)$ and $X(s)[H_2(s)e^{-sT} - H_1(s)]H_3(s)$

Compute both and use the larger of the two

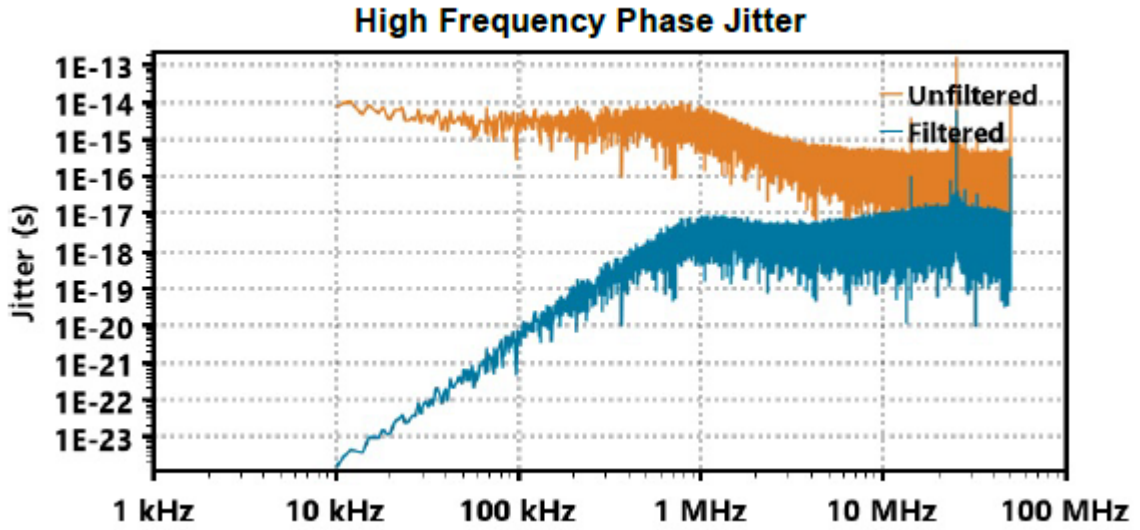
| Data Rate | CC jitter Limit | Notes |
|---|---|---|
| 2.5 GT/s | 86 ps pp | 1, 2 |
| 5.0 GT/s | 3.1 ps RMS | 1, 2 |
| 8.0 GT/s | 1.0 ps RMS | 1, 2 |
| 16.0 GT/s | 0.5 ps RMS | 1, 2, 3, 4 |
| 32.0 GT/s | 0.15 ps RMS | 1, 2, 3, 5 |

| PLL #1, PLL #2 | 0.01 dB peaking | 2.0 dB peaking |
|---|---|---|
| $BW_{PLL}$(min) = 0.5 MHz | $\omega_{n1}$= .112 Mrad/s $\zeta_1$ = 14 | $\omega_{n1}$= 1.51 Mrad/s $\zeta_1$ = 0.73 |
| $BW_{PLL}$(max) = 1.8 MHz | $\omega_{n1}$= .403 Mrad/s $\zeta_1$ = 14 | $\omega_{n1}$= 5.42 Mrad/s $\zeta_1$ = 0.73 |

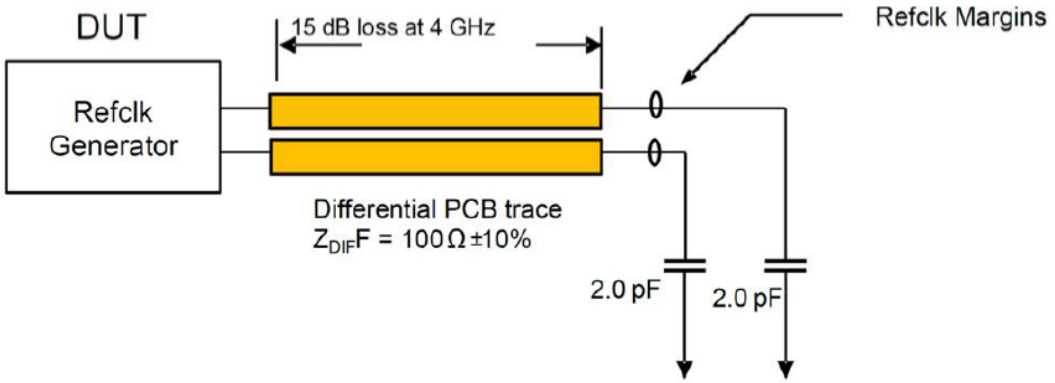
32.0 GT/s CC CDR

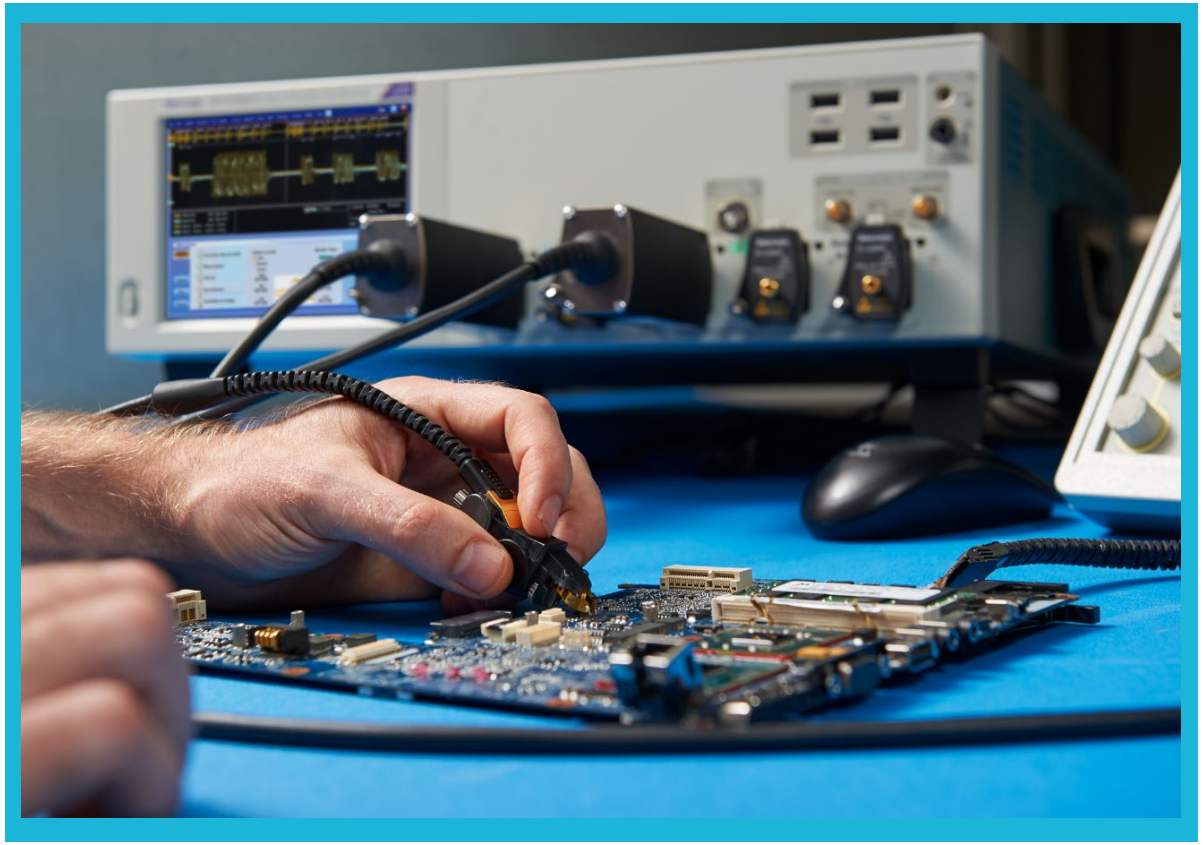
16 combinations

32.0 GT/s



# Signal Access



- Testing at lower data rates requires adding a 15dB channel & AC termination
- An allowance was added for 32 GT/s jitter measurements removing the channel and terminating with 50 Ohms.
- Phase noise analyzers are also now allowed for this measurement but generally don't support measurement with SSC
- When coaxial connections aren't available a probe may be used but at the cost of additional noise from the pre-amp

# Independent Refclk Jitter Limits

- The system clock jitter budget at 16.0 & 32.0 GT/s is larger than the refclk chip jitter budget and is used for full channel simulations during the Base spec development
  - 5.0 GT/s -> 3.1 ps RMS
  - 8.0 GT/s -> 1.0 ps RMS
  - 16.0 GT/s -> 0.7 ps RMS (Chip limit is 0.5 ps RMS)
  - 32.0 GT/s -> 0.25 ps RMS (Chip limit is 0.15 ps RMS)
- This additional jitter at the system level comes from system noise to jitter conversion as the clock edge flattens across a long channel route
- Independent Refclk architectures don't suffer from this penalty (assume no long route)
- The full system budget may therefore be used to characterize a clock chip in IR mode
  - The jitter from Tx & Rx refclks is assumed to add RMS since it's uncorrelated
- This white paper from Silicon Labs describes this topic in more detail: https://www.silabs.com/documents/public/white-papers/PCIe-Clock-Source-Selection.pdf

# 32 GT/s Refclk Lab Measurements

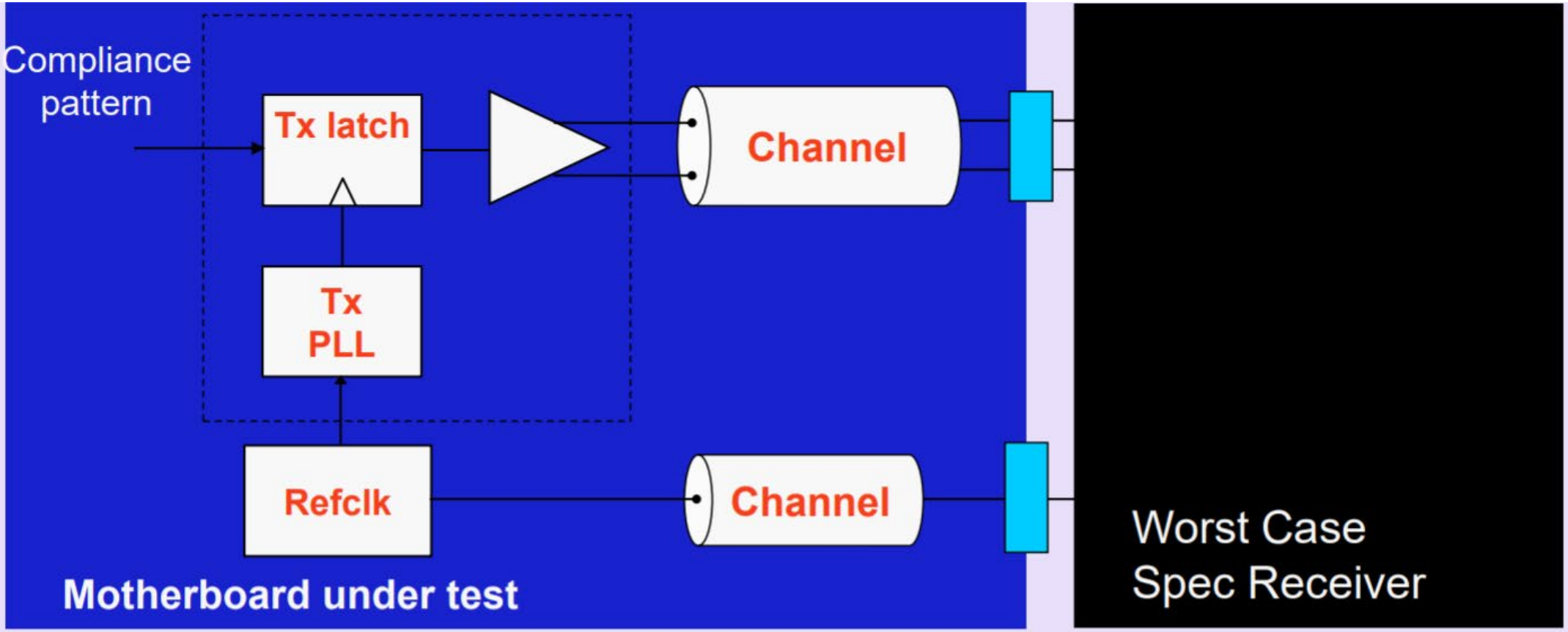
| Source | SSC | RT Scope | Jitter (fs) | Jitter minus scope noise (fs) |
|---|---|---|---|---|
| Si52204 | OFF | MSO64 | 126.03 | 106.26 |
| Si52204 | ON | MSO64 | 115.82 | 79.21 |
| Si52204 | OFF | DPS77004SX | 141.65 | 102.48 |
| Si52204 | ON | DPS77004SX | 140.34 | 66.88 |

Measurement Details

1. Channel was 50 Ohm terminated into the RT scope channels
2. MSO64 captures where with a sample rate of 25 GS/s & BW of 6 GHz
3. DPS77004SX captures where with a sample rate of 200 GS/s and BW of 5 GHz
4. 160K edges where captured for all results
5. SSC spurs from the fundamental & harmonics where removed up to 2 MHz

# Evolving Refclk Measurements

# PCIe 2.0 Dual Port Model for MB Tx




- How Does System Look With A Worst Case Spec Receiver?
  - ✓ Assume Common Clock Receiver
  - ✓ Assume worst case legal receiver PLL and add-in card delay

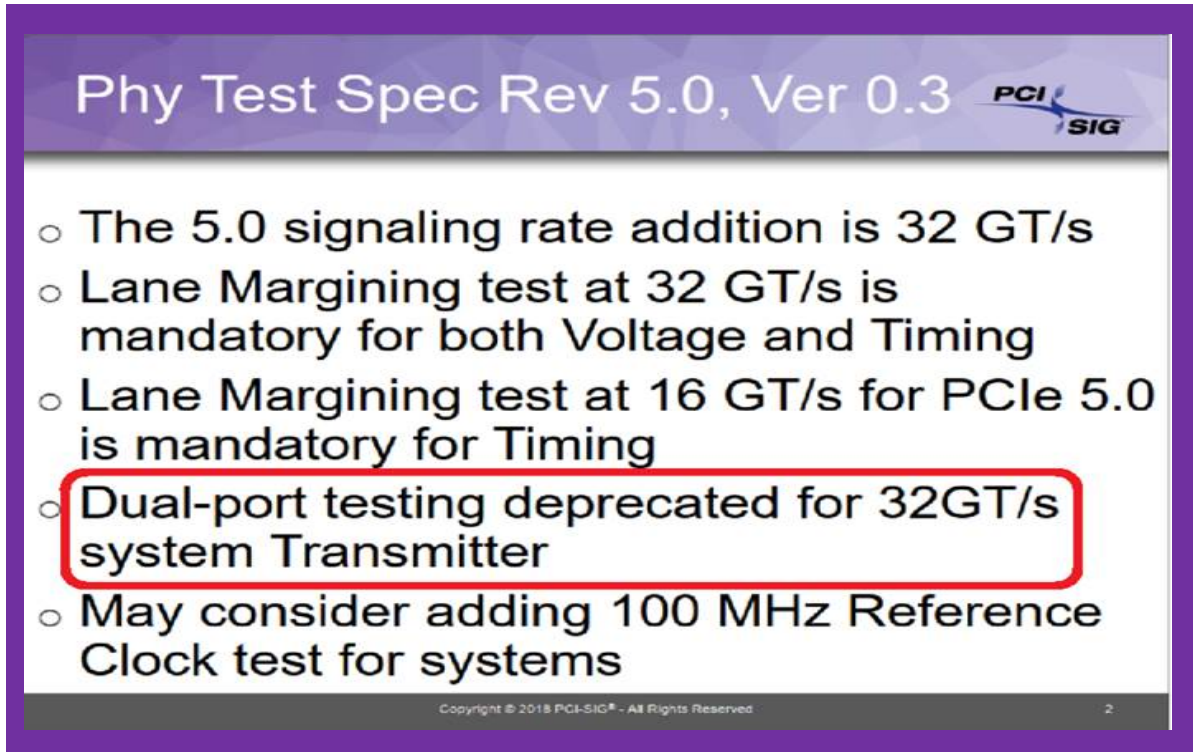
# PCIe 2.0 Dual Port Algorithm Overview

- Capture clock and data simultaneously
- Apply min/max bandwidth and peaking PLL filters to reference clock – producing several different filtered clock records
- Use each filtered clock record to compute phase jitter array for data using several different phase alignments to represent the min/max shift in phase that could occur on an add-in card
- The total jitter is the largest number obtained across all PLL bandwidths and phase alignments

# Dual Port Comparison – PCIe 2.0 & PCIe 5.0

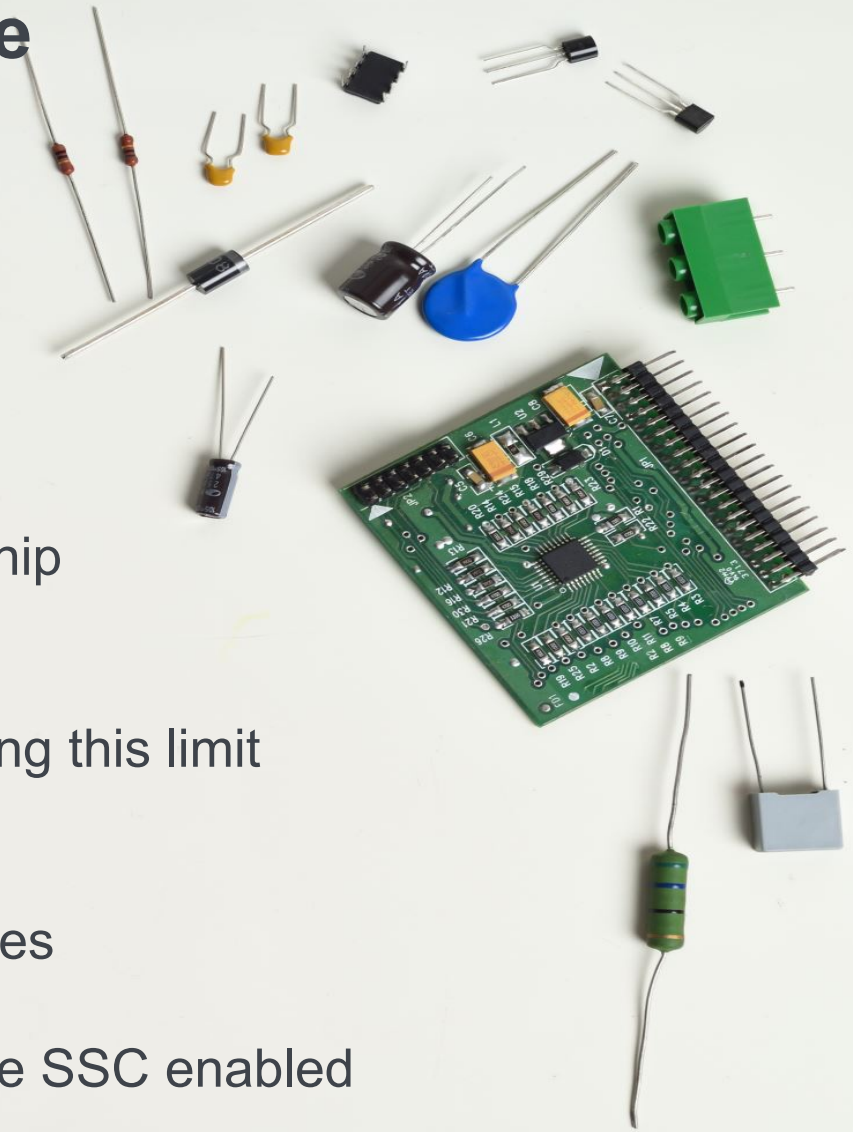
- PCIe 2.0
  - Common Clock model CDR has little rejection at 33 KHz and up to 2 MHz.
  - Reference Clock jitter limit large (3.1 ps RMS for 5.0 Gt/s PCIe).
  - Significant ability to trade off data and clock jitter at platform level
  - Significant savings from conservative assumptions of standalone clock test (min/max pll bandwidths and worst case phase mismatch)
  - Application of reference clock to compute data jitter straightforward (no reference equalizer)
- PCIe 5.0
  - Common Clock model CDR same as SRIS CDR and has lot of rejection at 33 KHz and up to 2 MHz
  - Reference Clock jitter limit very small (.15 ps RMS). No ability to trade off at platform level
  - Many high speed receiver designs do not use reference clock
  - Application of clock to compute data jitter is not straightforward. (reference receiver with CTLE and DFE and specific time domain CDR definition)
  - High speed oscilloscope channels are expensive

# Dual Port Testing Removed at 32 GT/s




- CEM workgroup voted in March 2020 to remove the Dual Port Requirement for 32 GT/s System Tx Signal Quality
- Workgroup decided to explore a 5.0 System refclk high freq jitter measurement
- Systems at 32 GT/s will be tested with the same CDR & reference Rx EQ algorithms as 32 GT/s Add-in Cards
- !!! Only 2 scope channels needed !!!

# PCI Express 5.0 System Refclk Compliance



- PCI Express 5.0 PHY Test Spec under development
- Planning System 32 GT/s Refclk high frequency jitter compliance test
- Pass/fail limit trending toward 200fs (between the 150fs chip limit and 250fs system simulation value)
- Experimentation performed with 4.0 motherboards showing this limit can be passed with refclks rated for the lower data rate
- Will scope noise removal be allowed – trending towards yes
- RT Scope (not PNA) will be used since Systems may have SSC enabled

# Tektronix Refclk Limit Experiment

Silicon Labs RefClock
(Si52204 Eval)

PCIe Gen5 Base
Rx Calibration Fixtures (Rev 1)

Tektronix RT Scope
(DPS77004SX)

| | |
|---|---|
| Reference Inputs | 1 |
| Phase Jitter (ps) | 0.4 |
| Output Frequency Max (MHz) | 100 |
| Jitter Attenuator | No |
| Package Type | QFN32 |

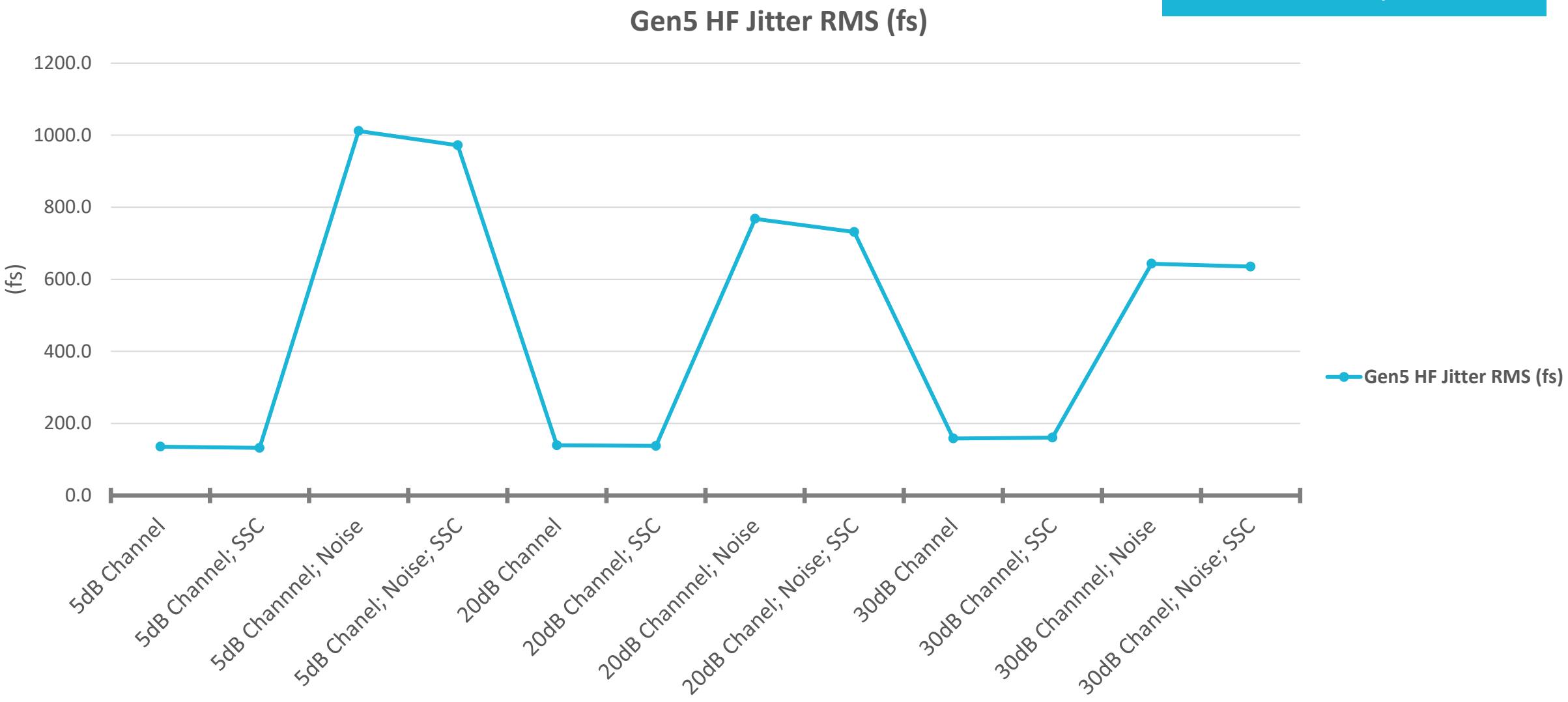
DMI

# Setup Details

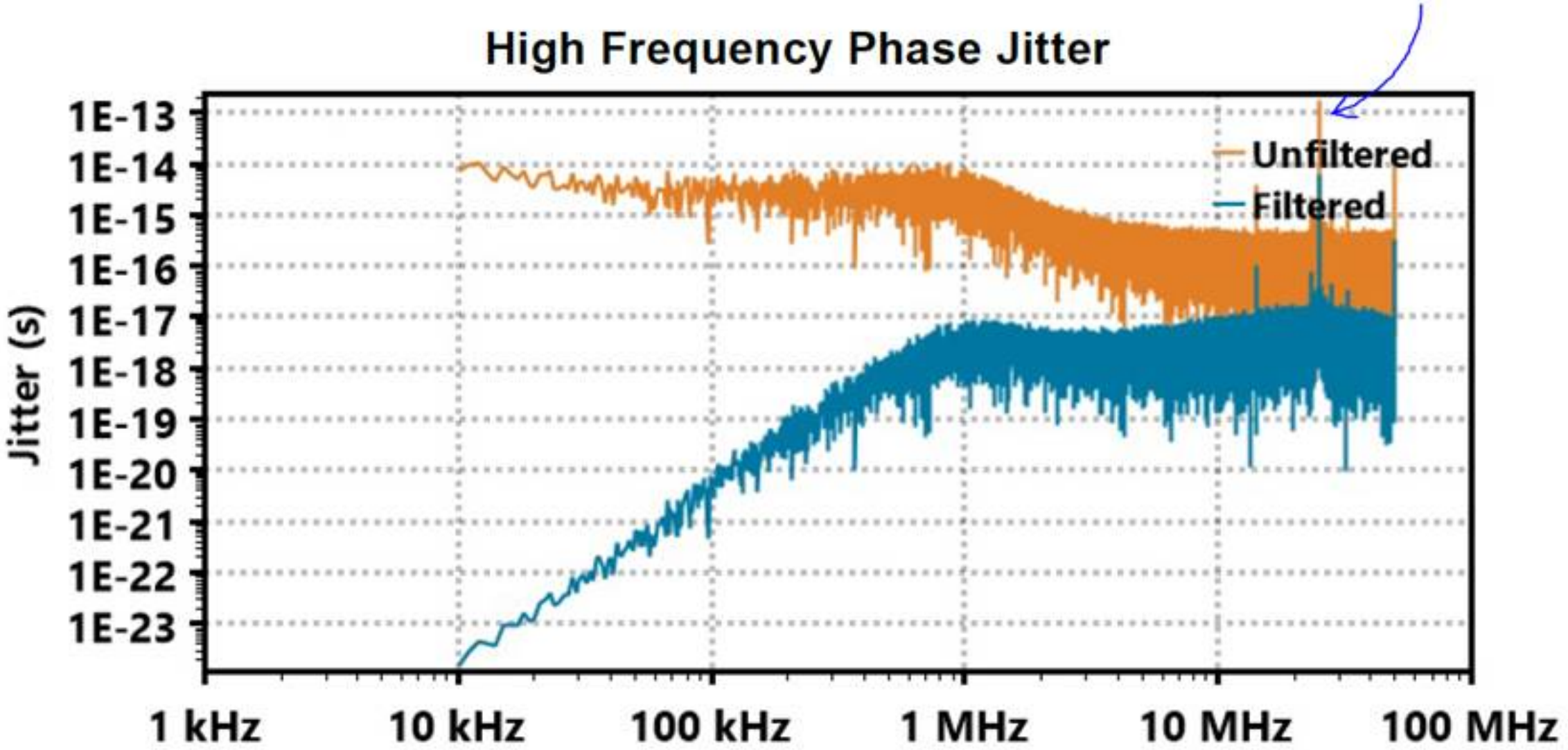
- **Source: Silicon Labs ref clock**
  - SI52204-8IX-EVB
  - Jitter RMS Spec of 110fs
  - SSC: On (30KHz with 5000ppm) & Off
- **Channels (Gen5 Base Rx Rev1 Fixtures)**
  - EVB cabled directly to scope
  - ~18 Meg6 microstrip trace & surface mount CEM connector
  - ~30 Meg6 microstrip trace & surface mount CEM connector
- **Cross Talk Addition**
  - Use 32 GT/s Rx Stressed Eye DMI Method
  - 10mV P2P 2.125 GHz sine wave coupled at output of EVB
  - Captured with and without DMI signal
- **RT Scope**
  - Tektronix DPS77004SX
  - Sample Rate: 50GS/s
  - Bandwidth: 8GHz
  - Record Length: 160K edges
- **Post Processing**
  - Silicon Labs “PCIe Clock Jitter Tool”

# Results

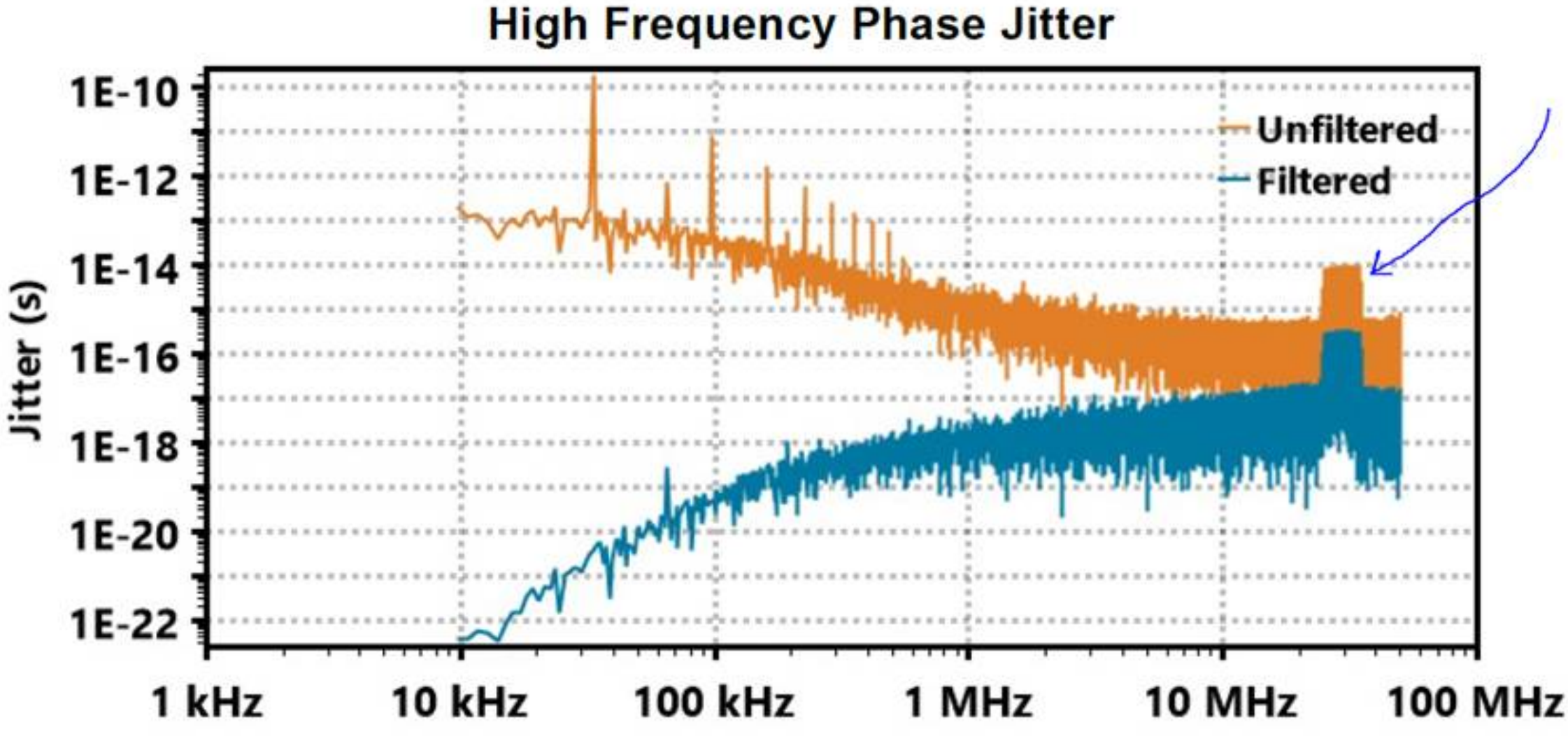
All Measurements include DUT and scope noise



# Deterministic Spur at 25 MHz (no SSC)



# Deterministic Spur around 25 MHz (SSC)



# Observations

- THE HF RMS JITTER WAS 135 FS FOR OUR BASELINE MEASUREMENT USING THE 5 DB CHANNEL WITH NO SSC AND NO NOISE ADDED. THIS IS CLOSE TO THE 150 FS GEN5 BASE SPEC LIMIT
- WHEN THE CHANNEL AND NOISE WAS FIXED A SLIGHT JITTER REDUCTION WAS OBSERVED WITH SSC ENABLED COMPARED TO SSC DISABLED. THIS IS EXPECTED DUE TO THE CHARACTERISTICS OF THE PART
- SLIGHT DECREASE OF HF RMS JITTER WITH CHANNEL LOSS INCREASE OBSERVED WHEN NOISE **WAS** INJECTED (DUE TO ATTENUATION OF 2.125 GHZ INJECTED NOISE HAVING SLIGHTLY MORE AFFECT (LOWER JITTER) THAN THE REDUCED EDGE RATE (INCREASING JITTER)
- SLIGHT INCREASE OF HF RMS JITTER WITH CHANNEL LOSS INCREASE OBSERVED WHEN NOISE **WASN'T** INJECTED (DUE TO THE SMALL REDUCTION OF HIGHER ORDER SQUIRE WAVE EDGE HARMONICS SLOWING THE EDGE RATE AND INCREASING SENSITIVITY TO SCOPE VERTICAL NOISE)
- INJECTED 2.125 GHZ NOISE (10MV PEAK-PEAK) CAUSED 25 MHZ SPUR WHERE THE JITTER TRANSFER FUNCTION IS RELATIVELY FLAT (~ 12DB DOWN) RESULTING IN HF RMS PLUS DETERMINISTIC JITTER VALUES WITHIN THE GEN5 BASE SPECIFICATION PTP SIMULATION VALUES FOR 1E-12 BER. SIMULATED JITTER PTP = 3.5PS = 250FS "RJ" RMS * 14 VS. MEASURED JITTER PTP = 2.9PS = 160FS RJ RMS * 14 + (635FS – 160FS) DJ RMS * SQRT(2)

# Tektronix Refclk Solutions

# Tektronix – PCI Express 5.0 Refclk Solution

- Fully Automated solution – TekExpress
- !!! Released Q4 2020 !!!
- Targeted Support
  - High Frequency Jitter Measurements (Gen1 to Gen5)
    - Scope Noise Removal (expected Q1 2021)
  - Refclk DC Specifications and AC Requirements
  - Data Rate Independent Refclk Parameters
- Real Time Scopes
  - DPS77004SX
  - DPS75004SX
  - MSO64

# Questions