

Tektronix

Anritsu
envision:ensure

PCI Express® Gen 5: Solving 32 GT/s Receiver Compliance and Validation Challenges

3/2/2021

Agenda

1

**PCI Express
Specification
Update**

2

**Challenges and
latest Rx
Guidelines**

3

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Tektronix PCIe
Solutions**

4

Questions

Note: PCI Express, PCIe, and PCI-SIG are registered trademarks and/or service marks of PCI-SIG.

PCI Express Specification Update

PCIe® 4.0 to 6.0 Base Specification Changes

	PCIe 4.0	PCIe 5.0	PCIe 6.0 (TBD)
Data Rate	16 GT/s	32 GT/s	64 GT/s (PAM4)
Add-in Card Loss	8dB @ 8Ghz	9.5dB @ 16GHz	TBD
Rx Test (Channel Loss)	- (27 to 30) dB @ 8GHz	- (34 to 37) dB @ 16GHz	- (30 to 33) dB @ 16GHz
Reference CTLE	2 Poles; 1 Zero; DC Gain Range (-6 to -12) dB	4 Poles; 2 Zero; DC Gain Range (-5 to -15) dB	6 Poles; 3 Zero; DC Gain Range (-5 to -15) dB
Reference DFE	2-Taps	3-Taps	16-Taps
Eye Width (Rx Test)	18.75 ps	9.375 ps	3.125 ps (top eye)
Eye Height (Rx Test)	15 mV	15 mV	6 mV (top eye)
Lane Margining	Required timing only	Required timing/voltage	Required timing/voltage
Refclk Jitter Limits	≤ 500 fs	≤ 150 fs	≤ 100 fs

PCIe 6.0 Specification Snapshot

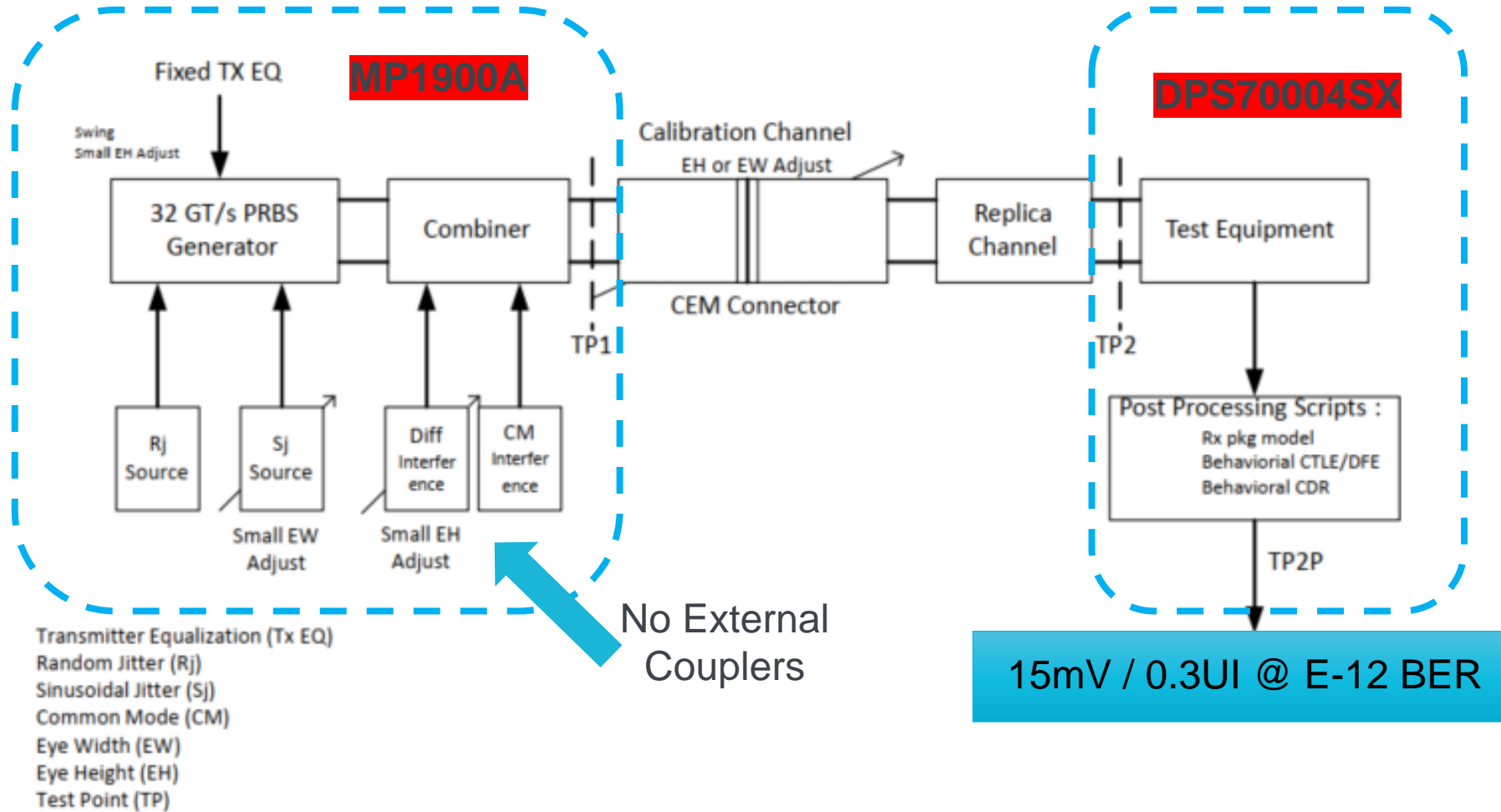
- **PCIe 6.0 Base Specification – Rev 0.7 workgroup approved**
 - Describes chip-level behavior on all levels of the stack
- **PCIe 6.0 CEM Specification – Rev 0.3 workgroup approved**
 - Card electro-mechanical (CEM) defines system and Add-in Card level
- **PCIe 6.0 PHY Test Specification – Rev 0.3 workgroup approved**
 - Describes electrical compliance tests for Tx, Rx LEQ, & PLL Bandwidth

PCIe 5.0 Specification Snapshot

- **PCIe 5.0 Base Specification – Rev 1.0 Released (Q2 2019)**
 - Describes chip-level behavior on all levels of the stack
- **PCIe 5.0 CEM Specification – Rev 1.0 workgroup approved**
 - Card electro-mechanical (CEM) defines system and Add-in Card level
- **PCIe 5.0 PHY Test Specification – Rev 0.5 workgroup approved**
 - Describes electrical compliance tests for Tx, Rx LEQ, & PLL Bandwidth
- **PCIe 4.0 – All Specifications at Rev 1.0**
 - Integrators List testing began August 2019

Challenges and Latest Rx Guidelines

32 GT/s Rx Stressed Eye Calibration



Calibration Nuances at 32 GT/s

The screenshot shows a test configuration interface with the following sections:

- BER Settings:** BER 1 E-12, Error Limit 1
- Test Length:** Duration 125 s, Confidence 90.842 % at 4E+12 Bits
- Stress Configuration:** Three tabs: Calibrated (selected), Customized, Un-Calibrated. Parameters include CMI (150 mV), RJ (0.5 ps (RMS)), DMI (27.5 mV), SJ (3.625 ps), and Amplitude (800 mV (Diff)).
- BER Measurement Pattern:** Modified Compliance

TP1 to TP3 Cable

- Cable used from BERT to Scope for Amp/Tx EQ/Rj/Sj calibration
- 16 GT/s – cable counted in Rx channel range of 27dB to 30dB
- 32 GT/s – cable excluded in Rx channel range of 34dB to 37dB

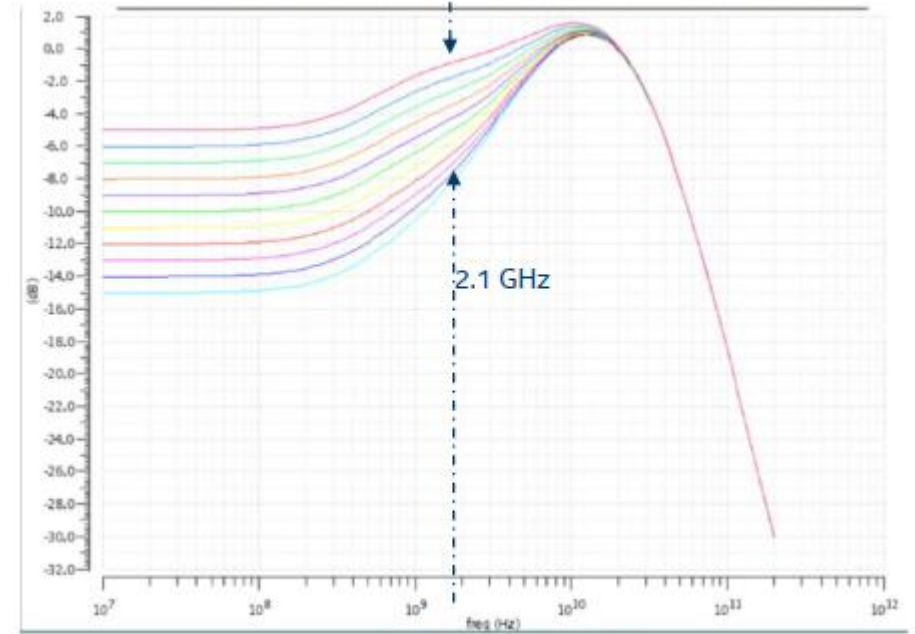
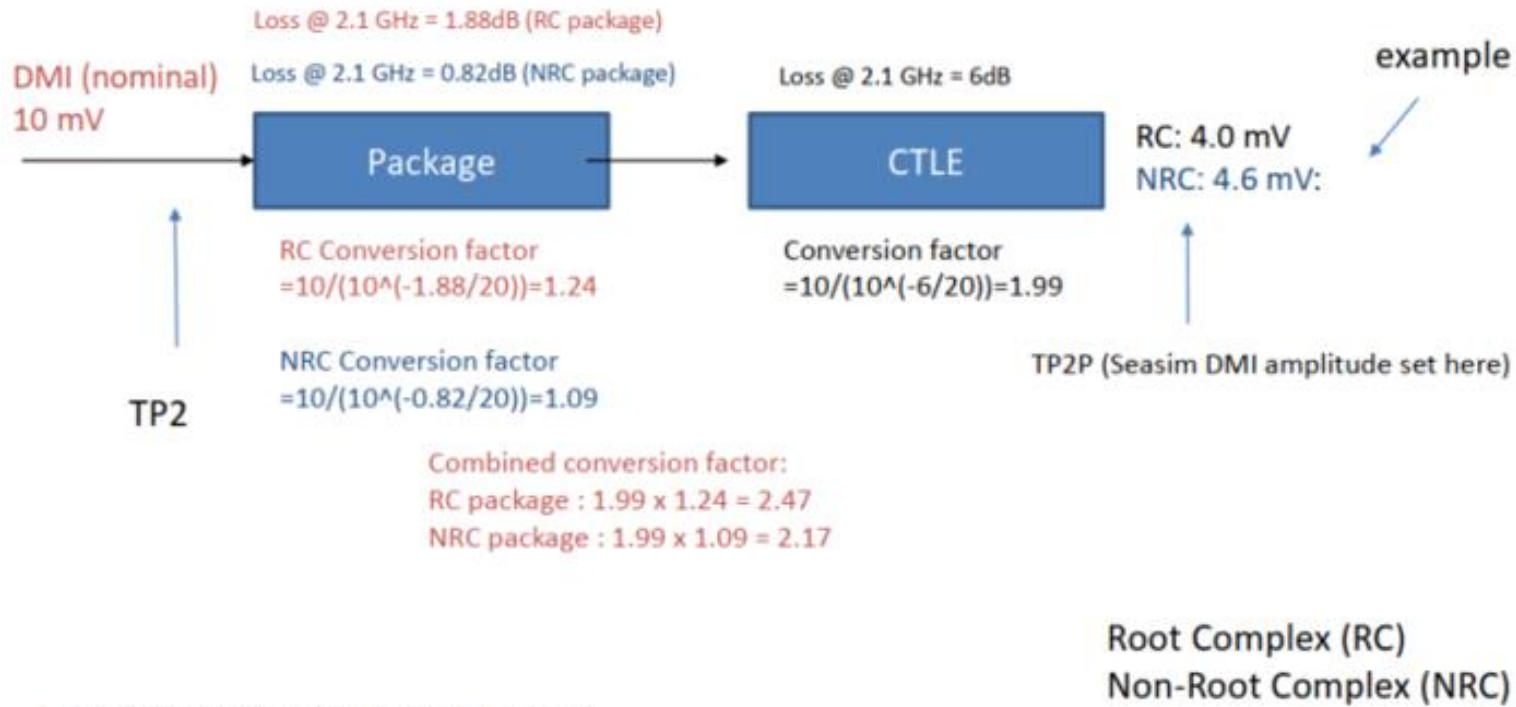
SigTest & Seasim

- Seasim - stress & noise in simulation
- SigTest (closed loop) – stress & noise intrinsic to waveform
- Seasim – requires characterizing BERT pulse width jitter

Tie Breakers

- Multiple solutions for stressed eye
- 1st – pick solution with highest channel loss
- 2nd – pick solution with EH closest to 15.0 mV
- If no solutions exist amplitude can be swept from 720mV to 800mV

Differential Mode Test Point Conversion



(Nominal DMI value based on PCIe 5.0 Rev 0.7 spec)

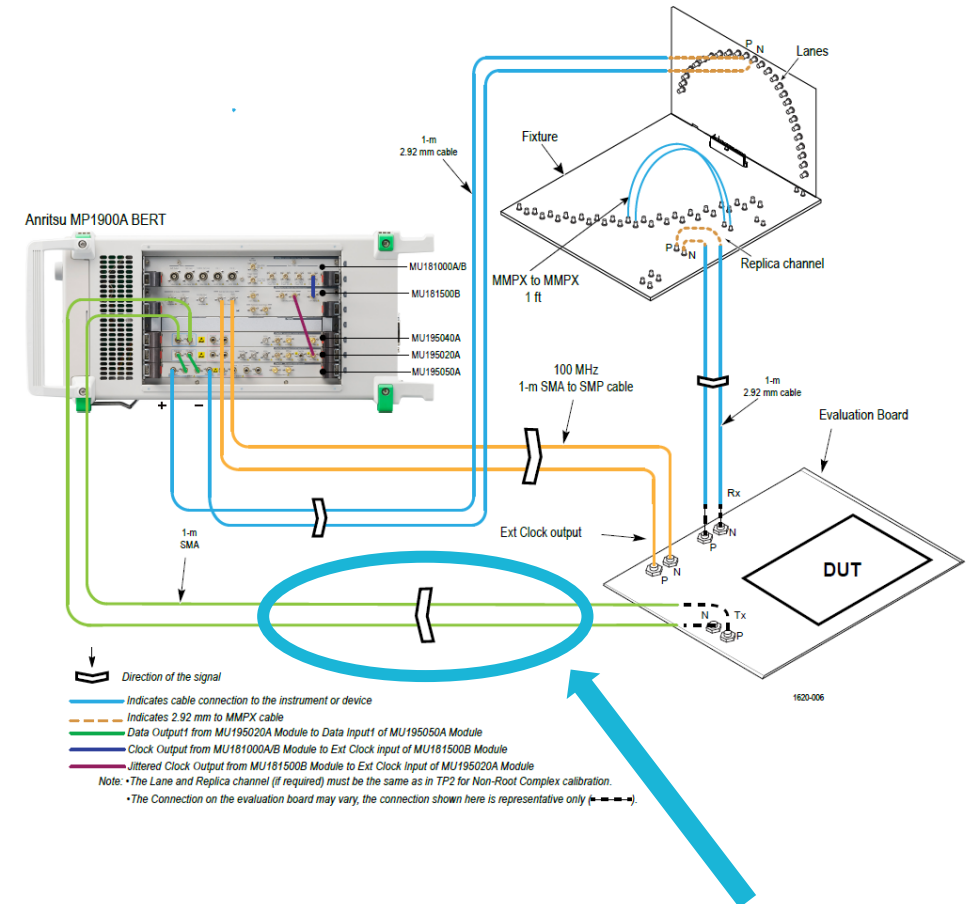
CTLE Curve	-15	-14	-13	-12	-11	-10	-9	-8	-7	-6	-5
Loss @ 2.1 GHz	-7.1656	-6.74485	-6.26725	-5.73227	-5.14069	-4.49494	-3.79846	-3.05574	-2.27145	-1.45083	-0.59882
CTLE conversion Factor	2.281813	2.173915	2.057607	1.934699	1.807318	1.677826	1.548542	1.421631	1.29889	1.181793	1.071374
RC Package Conversion Factor	1.24	1.24	1.24	1.24	1.24	1.24	1.24	1.24	1.24	1.24	1.24
NRC Package Conversion Factor	1.09	1.09	1.09	1.09	1.09	1.09	1.09	1.09	1.09	1.09	1.09
DMSI Conversion Factor RC package	2.829448	2.695654	2.551433	2.399027	2.241074	2.080505	1.920192	1.762823	1.610624	1.465424	1.328503
DMSI Conversion Factor NRC package	2.487176	2.369567	2.242792	2.108822	1.969976	1.828831	1.687911	1.549578	1.415791	1.288155	1.167797

NEW



32 GT/s Back Channel Equalization

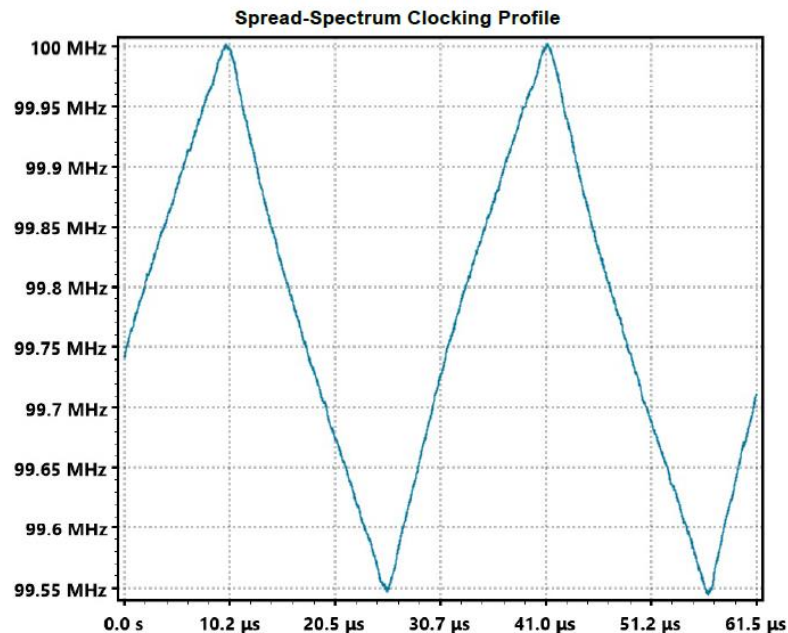
- Rx calibration calls for 34 to 37 dB @ 16GHz
- 5.0 Add-in Card budget = 9.5dB
- 5.0 Systems
 - 27.5dB including mated CEM connector
 - Fixtures/Cables could add another 4dB
- Add-in Card Rx LEQ – Error Detector EQ sufficient
- System Rx LEQ – Some require external EQ expected
 - Active Redriver should be considered
 - Expected across the industry
- Redrivers
 - Non Linear devices allowed
 - Avoid introducing bit errors in back channel only
 - Performs similar to CTLE with additional gain stages
- Experimentation expected at early FYI workshops



Backchannel (location for redriver)

Receiver Testing with SSC at 32 GT/s

Spread Spectrum Clocking (SSC) is utilized to spread the radiated electromagnetic energy across a wider frequency band and minimize the potential interference with other electronic devices.



PCI Express 5.0 SSC Parameters

SSC Frequency Range	30 to 33 KHz
SSC Deviation	-0.5 to 0.0 % UI
SSC Deviation (SRIS)	-0.3 to 0.0 % UI
SSC Slew Rate	1250 ppm / us

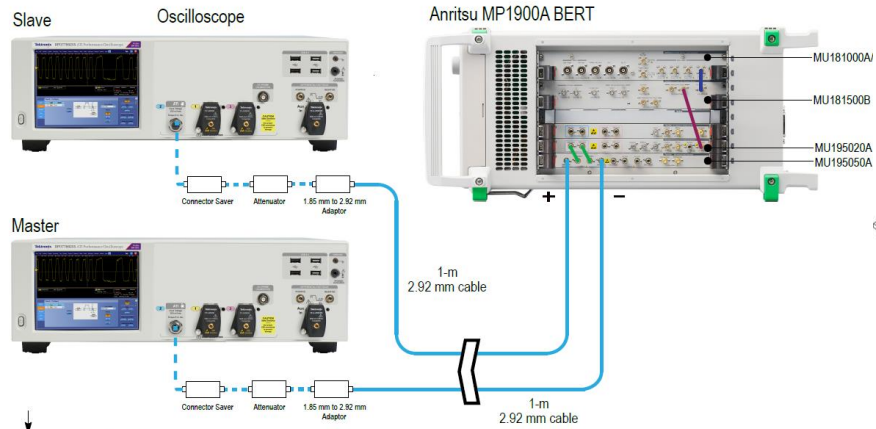
- Base Rx performs JTOL including a SSC tone
- Add-in Cards historically have not tested with SSC
- Systems testing at 16 GT/s – CTS did not define
 - In practice many were tested with SSC enabled
- Expect more clarity in 32 GT/s CTS
- **Anritsu/Tek solution supports testing with/without SSC!!!**

Anritsu & Tektronix PCIe Solutions

Tektronix Solution Configuration

TEST SYSTEM VIEW GEN5 CEM CALIBRATION

TP1 Calibration

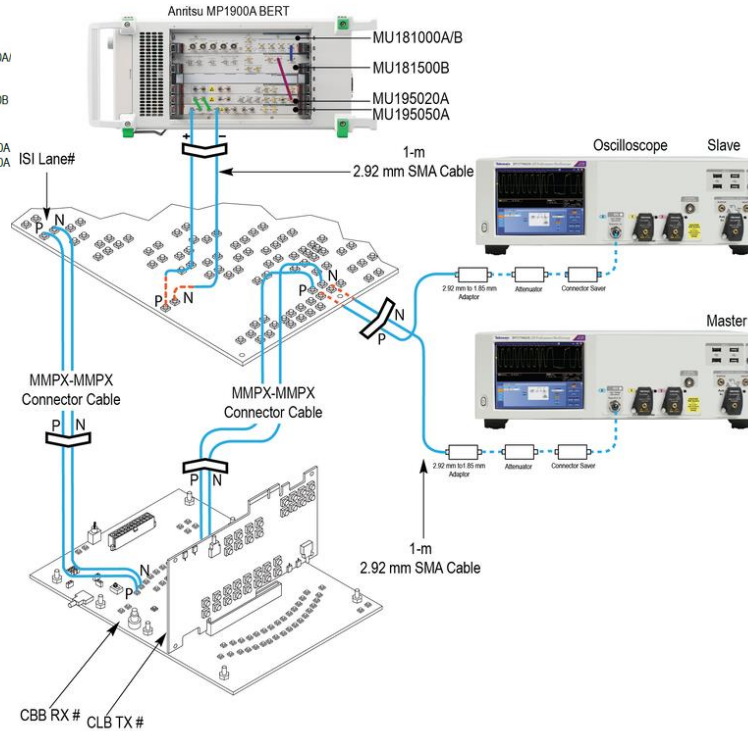


- Direction of the signal
 - Indicates direct connection to the instrument or device
 - Indicates cable connection to the instrument or device
 - Data Output1 from MU195020A Module to Data Input1 of MU195050A Module
 - Clock Output from MU181000A/B Module to Ext Clock input of MU181500B Module
 - Jittered Clock Output from MU181500B Module to Ext Clock Input of MU195020A Module
- Minimum 6dB Attenuation is required



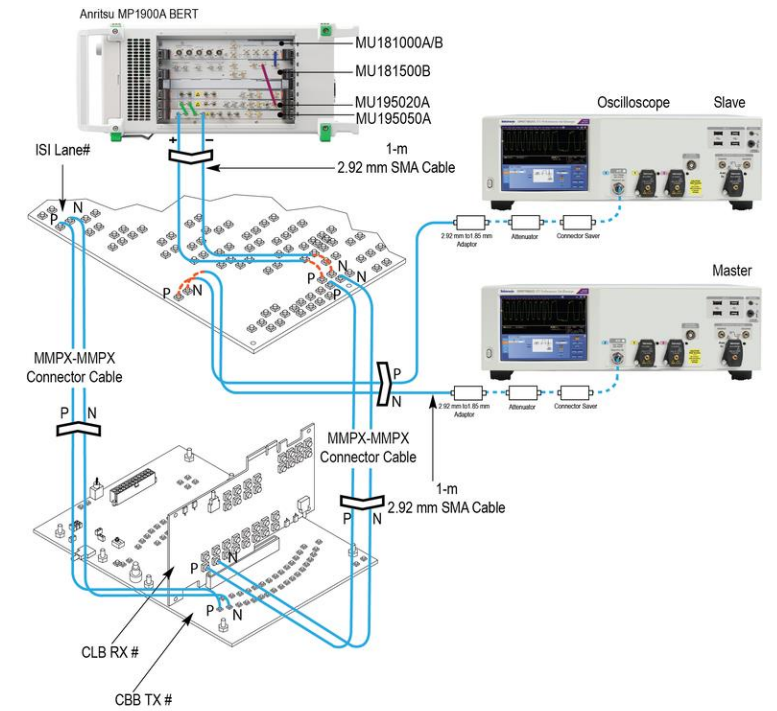
Tektronix Receiver Solution

TP2 AIC Calibration



- SMA-MMPX Connector
 - Direction of Signal
 - Indicates direct connection to the instrument or device
 - Data Output1 from MU195020A Module to Data Input1 of MU195050A Module
 - Clock Output from MU181000A/B Module to Ext Clock input of MU181500B Module
 - Jittered Clock Output from MU181500B Module to Ext Clock Input of MU195020A Module
- Note: • Use 36 dB nominal channel loss for calibration based on Lane selection (if required)
 • Physical channel loss without package model for System and AIC to be 27 dB and 32 dB respectively
 • Minimum 6 dB attenuation is required at the oscilloscope input

TP2 SYS Calibration



- SMA-MMPX Connector
 - Direction of Signal
 - Indicates direct connection to the instrument or device
 - Data Output1 from MU195020A Module to Data Input1 of MU195050A Module
 - Clock Output from MU181000A/B Module to Ext Clock input of MU181500B Module
 - Jittered Clock Output from MU181500B Module to Ext Clock Input of MU195020A Module
- Note: • Use 36 dB nominal channel loss for calibration based on Lane selection (if required)
 • Physical channel loss without package model for System and AIC to be 27 dB and 32 dB respectively
 • Minimum 6 dB attenuation is required at the oscilloscope input

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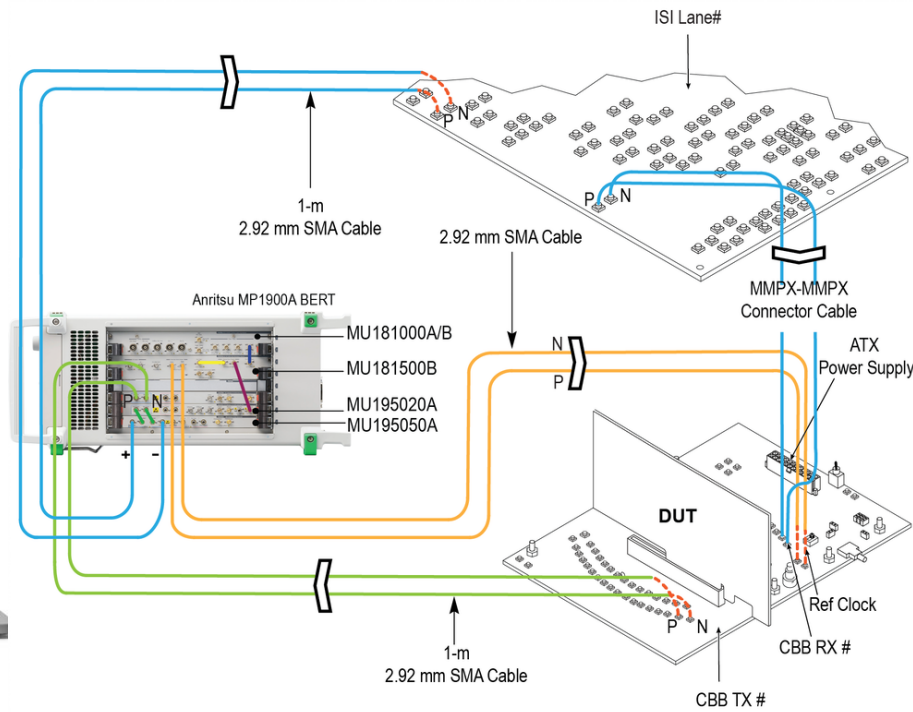
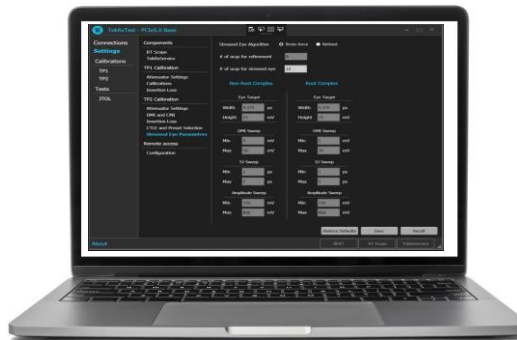
Tektronix Solution Configuration

TEST SYSTEM VIEW GEN5 CEM TEST

RX LEQ AIC Tests

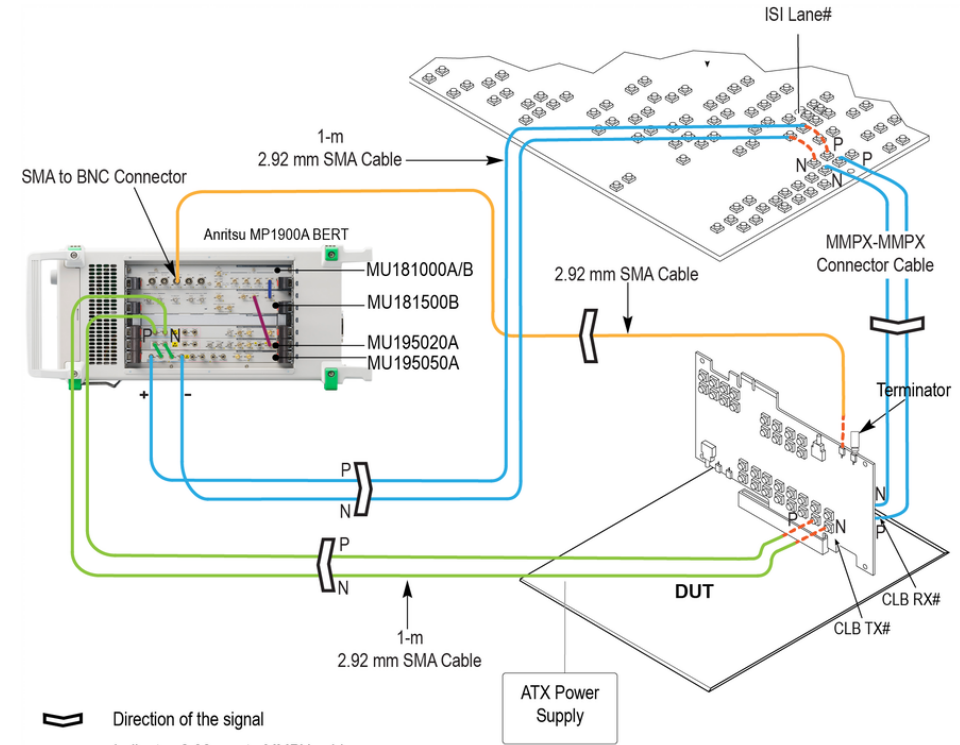
RX LEQ SYS Tests

Tektronix Receiver Solution



- Direction of the signal
- Indicates 2.92 mm to MMPX cable
- Data Output1 from MU195020A Module to Data Input1 of MU195050A Module
- Clock Output from MU181000A/B Module to Ext Clock input of MU181500B Module
- Jittered Clock Output from MU181500B Module to Ext Clock Input of MU195020A Module
- Jitter Clock Output to Aux Input

1620-006

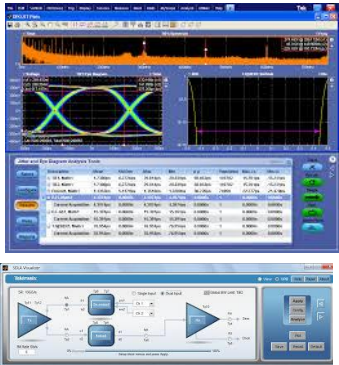


- Direction of the signal
- Indicates 2.92 mm to MMPX cable
- Data Output1 from MU195020A Module to Data Input1 of MU195050A Module
- Indicates cable connection to the instrument or device
- Clock Output from MU181000A/B Module to Ext Clock input of MU181500B Module
- Jittered Clock Output from MU181500B Module to Ext Clock Input of MU195020A Module

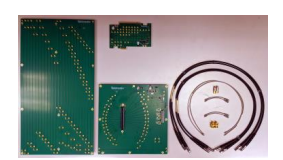
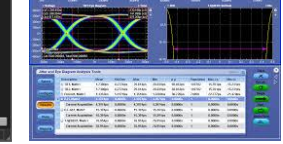
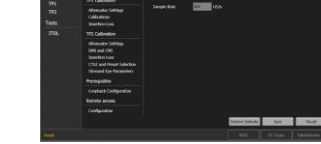
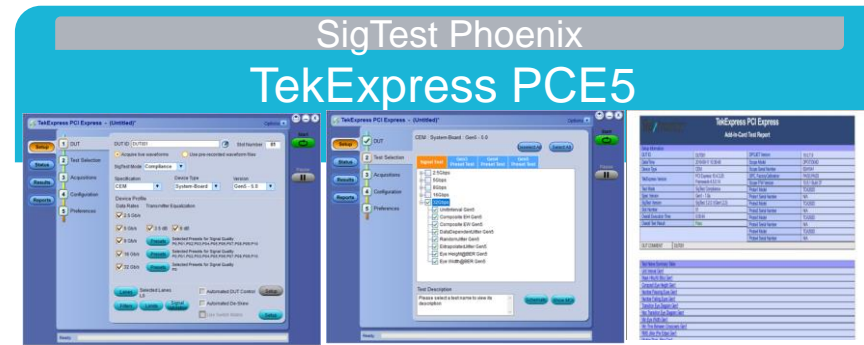
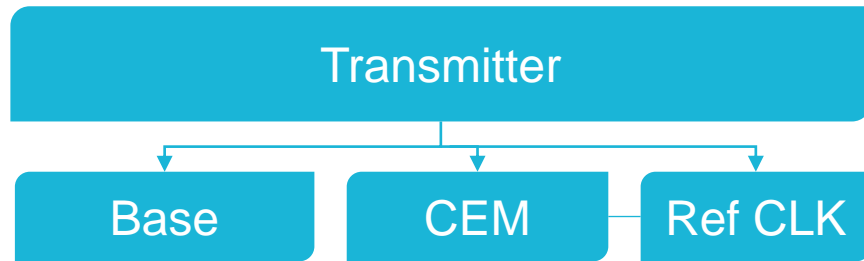
PCIe Gen5 Solution Landscape

Debug

DPOJET Plugin for Debug

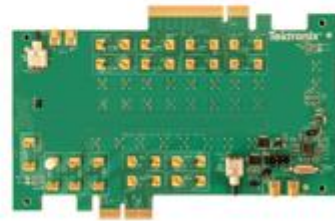
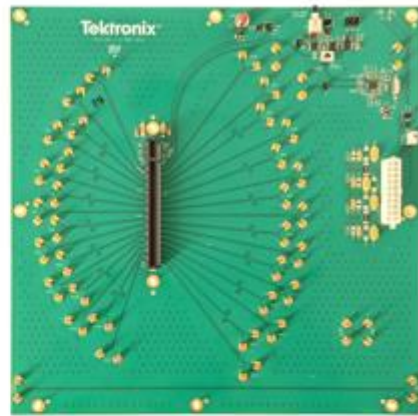


SDLA



FUTURE PROOF FOR GEN6 – Tektronix is involved in PCI-SIG pathfinding!!!

Tektronix PCIe Gen5 Pre-Compliance Fixtures



- Gen5 CEM SIG fixtures delayed
- Tektronix fixtures available today
- X1 Kit
 - CBB, CLB x1/x16 & ISI
- X16 Kit
 - CBB, CLB x1/x16 & x4/x8, ISI
- Includes MMPX adaptors & cables
- Expect similar performance to SIG fixtures
 - Stressed eye calibration
 - Rx/Tx LEQ Testing
 - Tx Signal Quality & Tx Preset
 - Add-in Card PLL BW

RX LEQ Test and Jitter Tolerance Test

RX LEQ Test Procedure

Steps of Receiver Testing

Step1: Calibration

- Channel Loss by VNA
- Eye Amplitude, Preset, SJ and RJ by BERT and RTO
- DM-I and Eye Height/Eye Width by BERT and RTO



Step2: Link Training

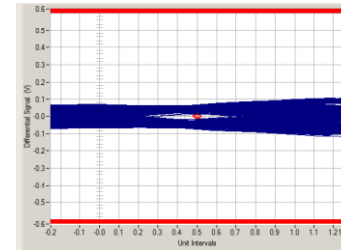
DUT needs to be looped back under the compliance stress condition

- Loopback Active Master
- Troubleshooting



Step3: Measurement

- Checking BER <math>< 1E(-12)</math> for 125 seconds (95% confidence level)
- Jitter Tolerance Testing (Optional)



	Min	Max
EH	13.5 mV	16.5 mV
EW	9.13 ps	9.62 ps

Equipment Setup | Link Training | Run Test | Graph | Report | Output

Specification: 5.0(32.0 GT/s) | Endpoint (AIC) | More results

LTSSM State: Loopback.Active.Master | Linkup Speed: 32.0 Gbps

LEQ Test: Rx LEQ | Apply

Rx LEQ: Initial TX LEQ | Tx LEQ Response

Loopback Through: Recovery

Link EQ: Preset | Saved Cursor...

Lane: 0/8

Test Pattern: MCP (Modified Compliance Pattern)

Received: Use Preset | Preset | PPG Final Preset | P5

PPG Final Cursor: Pre-Cursor: 2 | Cursor: 22 | Post-Cursor: 0

Full Swing, Low Frequency: 48 | 16

Link, Lane Number: 1 | 0

Recovery.EQ: PCIe 3 | PCIe 4 | PCIe 5

1 | Complete | Complete | Complete

2 | Complete | Complete | Complete

3 | Complete | Complete | Complete

PCIe 5.0 | CTLE Gain [dB]: PCIe5 | -3.0

EC Threshold: 1

Pass/Fail: PASS

Cycle: Single

Gating Time: 125 [s]

Switch To Manual BER Test: Error Addition

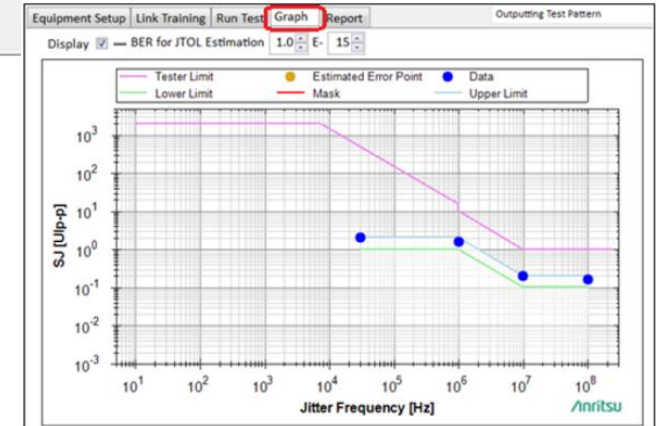
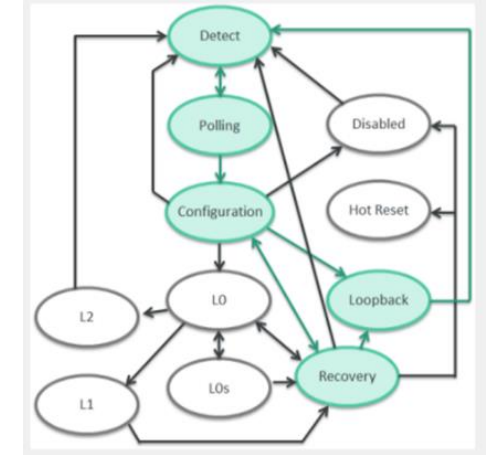
Total BER: 0.0000E-12

Total Error Count: 0

Total Bits: 4.0000E+12

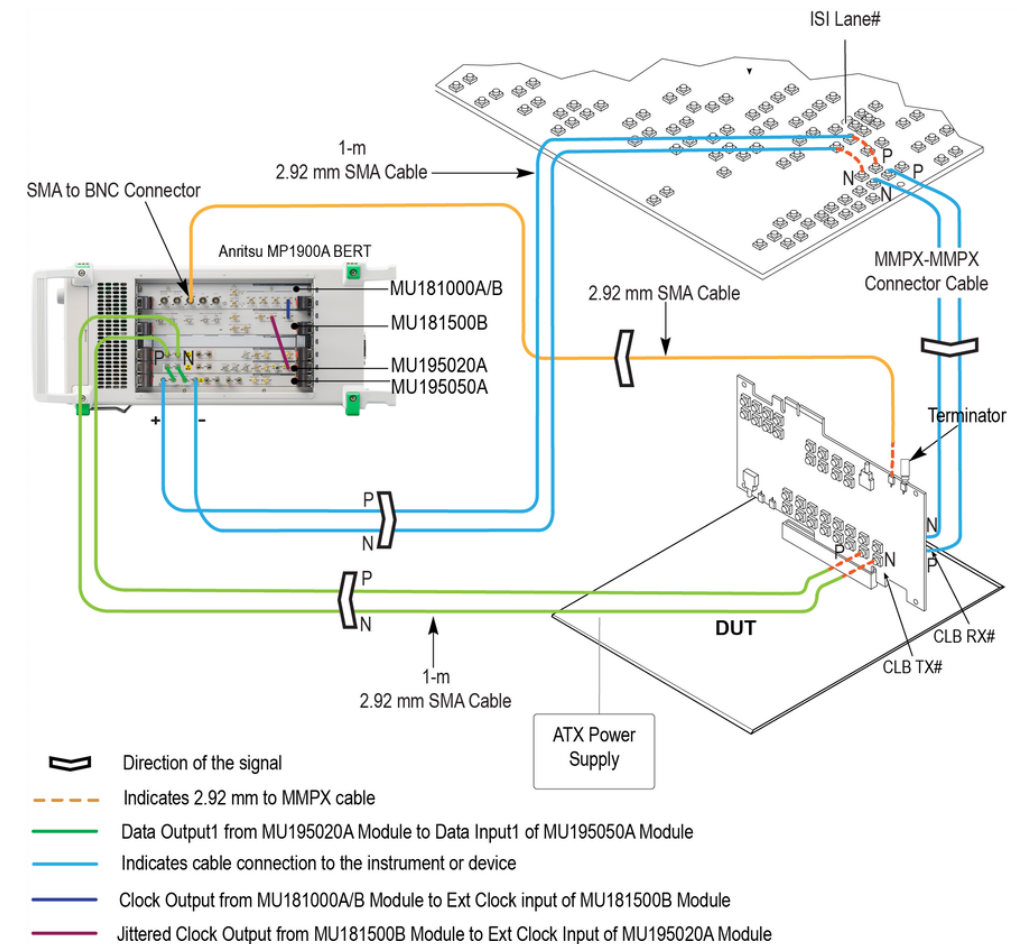
Current BER: 0.0000E-09

Sync Loss: | Clock Loss:



First and Most Critical Step for Stable and Repeatable RX Test

- Object of RX LEQ Test: Successful Link Equalization Training under the specific stressed eye condition
 - ✓ Optimize the equalizer (Preset and CTLE)
 - ✓ Go to Loopback Status (Loopback Active Master)
 - ✓ BER 1E(-12)
- **Establish the return path:**
 - ✓ Minimize loss and ISI of the return path
 - ✓ Optimize the equalization between DUT TX Preset and CTLE of the error detector
 - ✓ Error Free on the return path (DUT TX to the Error Detector) to isolate the error source
 - ✓ System may need Re-Driver when the Actual physical loss of the return path is more than 18 dB (18 to 26.5 dB)



PCI Express Gen5 RX LEQ Calibration Points

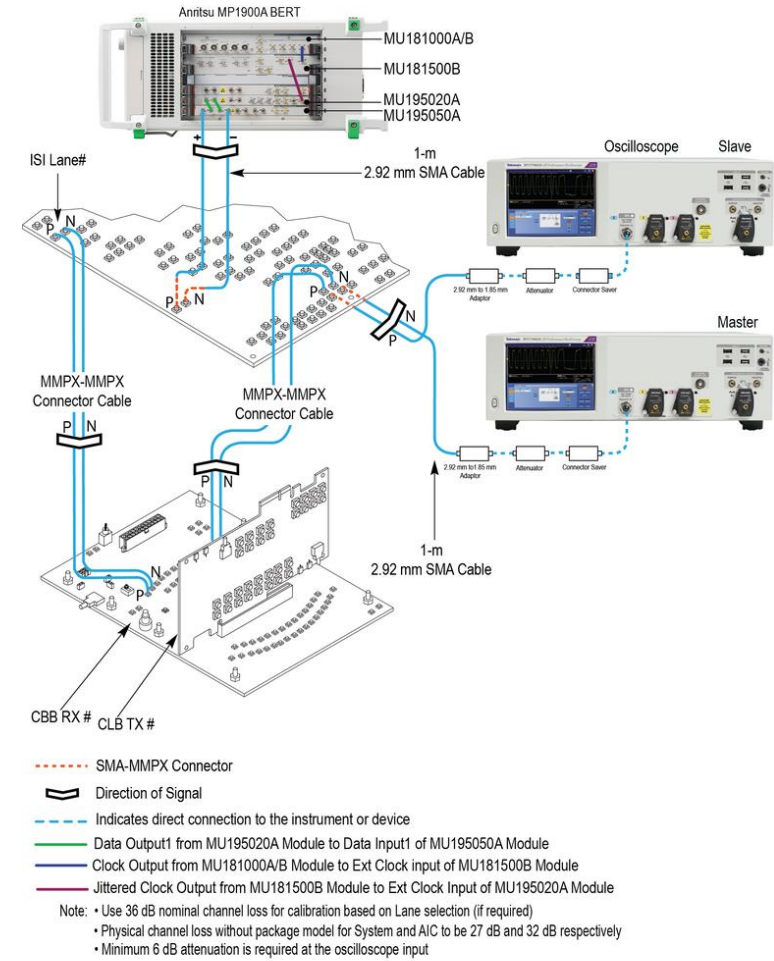
Stress Signal Calibration

Transition to Loopback Status

Stress Signal Input Test

Table 8-9 Stressed Jitter Eye Parameters

Symbol	Parameter	2.5 GT/s	5.0 GT/s	8.0 GT/s	16.0 GT/s	32.0 GT/s	Units	Details
$V_{RX-LAUNCH}$	Generator launch voltage	800 to 1200	800 to 1200	800 to 1200	720 to 800	720 to 800	mV PP	Note 1
T_{RX-UI}	Unit Interval	400	200	125	62.5	31.25	ps	
T_{RX-ST}	Eye width	≤ 0.4	≤ 0.32	≤ 0.30	≤ 0.30	≤ 0.30	UI	Note 3, 4, 8, 10
V_{RX-ST}	Eye height	≤ 175	≤ 100	≤ 25	≤ 15	≤ 15	mV PP	Note 2, 4, 8, 9
$T_{RX-ST-SJ}$	Swept Sj	N/A	75 ps (max) See Note 11	See Section 8.4.2.2.1	See Section 8.4.2.2.1	See Section 8.4.2.2.1	ps	Note 5
$T_{RX-ST-RJ}$	Random Jitter	N/A	3.4	(max) 3.0	1.0	0.5	ps RMS	Note 6, 7
$V_{RX-DIFF-INT}$	Differential noise	N/A	N/A	14	14	10	mV PP	Note 7, 12 Adjust to set EH. Frequency = 2.1 GHz .
$V_{RX-CM-INT}$	Common mode noise	150	150	150	150	150	mV PP	Note 8



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PCI Express Gen5 Link Training

Stress Signal Calibration

Transition to Loopback Status

Stress Signal Input Test

MX183000A - PCIe Link Training

File Setup Help

Operate MP1900A

Equipment Setup Link Training Run Test Graph Report

Specification DUT

5.0(32.0 GT/s) Endpoint (AIC) More results

Unlink

Matrix Scan

LEQ Test Setting Rx LEQ

Configure

BER Measurement

LTSSM Log

Loopback Method

Recovery Full EQ

Test Pattern

Compliance

MCP

Timeout

Option

Received

Use Preset Preset

PPG Final Preset P5

PPG Final Cursor

Pre-Cursor	Cursor	Post-Cursor
2	22	0

Full Swing, Low Frequency

	PCIe 3	PCIe 4	PCIe 5
Phase0 (Root)	-----	-----	-----
Phase1	Complete	Complete	Complete
Phase2	Complete	Complete	Complete
Phase3	Complete	Complete	Complete

Recovery.EQ

Recovery Full EQ

Recovery EQ

Phase0 (Root) -----

Phase1 Complete Complete Complete

Phase2 Complete Complete Complete

Phase3 Complete Complete Complete

Loopback Through: Recovery

Link EQ: Preset Saved Cursor...

Lane: 0/8

Test Pattern: MCP (Modified Compliance Pattern)

PPG Starting Preset: P9

DUT Initial Preset (Preset Hint Tx): P9

DUT Target Preset (Change Preset): P9

PCIe 5.0

CTLE Gain [dB] PCIe5 -3.0

Preset Auto

BER Measurement

EC Threshold 1

Pass/Fail PASS

Cycle Single

Gating Time 125 [s]

Switch To Manual BER Test Error Addition

Total BER 0.0000E-12

Total Error Count 0

Total Bits 4.0000E+12

Current BER 0.0000E-09

Sync Loss Clock Loss

Jitter

SJ1

Frequency 100000000 Hz

Amplitude 0.132 Ulp-p

4.12 ps p-p

SJ2

SJ2 Mode SJ2 via MU181000

Frequency 10 Hz

Amplitude 0.000 Ulp-p

0.00 ps p-p

BUJ

PRBS PRBS7

Bitrate 12.500000 Gbit/s

Amplitude 0.000 Ulp-p

0.00 ps p-p

Troubleshooting by Manual Preset/Cursor Setting

PCIe 5.0

CTLE Gain [dB]

EC Threshold

Pass/Fail

Gating Time [s]

Switch To Manual BER Test

Total BER

Total Error Count

Total Bits

Current BER

Sync Loss Clock Loss

Cursor BER Measurement

Coefficient

C-1 PS dB

C0 DE dB

C+1 Boost dB

	C+1	0/24	1/24	2/24	3/24	4/24	5/24	6/24	7/24	8/24
C-1	0.0000	0.0417	0.0833	0.1250	0.1667	0.2083	0.2500	0.2917	0.3333	
0/24	0.0000	0.0, 0.0	0.0, -0.8	0.0, -1.6	0.0, -2.5	0.0, -3.5	0.0, -4.7	0.0, -6.0	0.0, -7.6	0.0, -9.5
1/24	0.0417	0.8, 0.0	0.8, -0.8	0.9, -1.7	1.0, -2.8	1.2, -3.9	1.3, -5.3	1.6, -6.8	1.9, -8.8	
2/24	0.0833	1.6, 0.0	1.7, -0.9	1.9, -1.9	2.2, -3.1	2.5, -4.4	2.9, -6.0	3.5, -8.0		
3/24	0.1250	2.5, 0.0	2.8, -1.0	3.1, -2.2	3.5, -3.5	4.1, -5.1	4.9, -7.0			
4/24	0.1667	3.5, 0.0	3.9, -1.2	4.4, -2.5	5.1, -4.1	6.0, -6.0				
5/24	0.2083	4.7, 0.0	5.3, -1.3	6.0, -2.9	7.0, -4.9					
6/24	0.2500	6.0, 0.0	6.8, -1.6	8.0, -3.5						

SI PPG

Amplitude Vp-p

PCIe AIC Test: SSC

SI ED

Data Threshold V

XData Threshold V

Noise

CM

Band

Frequency MHz

Amplitude mVp-p

DM

Frequency GHz

Amplitude mVp-p

Auto Cursor Matrix Scan

C1/FS	C1/FS	063	163	263	363	463	563	663	763	863	963	1063	1163	1263	1363	1463	1563	1663	1763	1863	1963	2063	2163	
063	0.000	0.00	0.03	0.06	0.09	0.12	0.15	0.18	0.22	0.25	0.29	0.33	0.37	0.42	0.46	0.51	0.55	0.60	0.64	0.69	0.74	0.79	0.83	0.88
163	0.016	0.03	0.07	0.11	0.15	0.19	0.23	0.27	0.31	0.35	0.39	0.43	0.47	0.51	0.55	0.59	0.63	0.67	0.71	0.75	0.79	0.83	0.87	0.91
263	0.032	0.06	0.13	0.20	0.27	0.34	0.41	0.48	0.55	0.62	0.69	0.76	0.83	0.89	0.96	1.03	1.10	1.17	1.24	1.31	1.38	1.45	1.52	1.59
363	0.048	0.09	0.19	0.29	0.39	0.49	0.59	0.69	0.79	0.89	0.99	1.09	1.19	1.29	1.39	1.49	1.59	1.69	1.79	1.89	1.99	2.09	2.19	2.29
463	0.063	0.12	0.25	0.38	0.51	0.64	0.77	0.90	1.03	1.16	1.29	1.42	1.55	1.68	1.81	1.94	2.07	2.20	2.33	2.46	2.59	2.72	2.85	2.98
563	0.079	0.15	0.31	0.47	0.63	0.79	0.95	1.11	1.27	1.43	1.59	1.75	1.91	2.07	2.23	2.39	2.55	2.71	2.87	3.03	3.19	3.35	3.51	3.67
663	0.095	0.18	0.37	0.56	0.75	0.94	1.13	1.32	1.51	1.70	1.89	2.08	2.27	2.46	2.65	2.84	3.03	3.22	3.41	3.60	3.79	3.98	4.17	4.36
763	0.111	0.22	0.44	0.66	0.88	1.10	1.32	1.54	1.76	1.98	2.20	2.42	2.64	2.86	3.08	3.30	3.52	3.74	3.96	4.18	4.40	4.62	4.84	5.06
863	0.127	0.25	0.50	0.75	1.00	1.25	1.50	1.75	2.00	2.25	2.50	2.75	3.00	3.25	3.50	3.75	4.00	4.25	4.50	4.75	5.00	5.25	5.50	5.75
963	0.143	0.29	0.57	0.86	1.14	1.43	1.71	2.00	2.29	2.57	2.86	3.14	3.43	3.71	4.00	4.29	4.57	4.86	5.14	5.43	5.71	6.00	6.29	6.57
1063	0.159	0.33	0.66	0.99	1.32	1.65	1.98	2.31	2.64	2.97	3.30	3.63	3.96	4.29	4.62	4.95	5.28	5.61	5.94	6.27	6.60	6.93	7.26	7.59
1163	0.175	0.37	0.74	1.11	1.48	1.85	2.22	2.59	2.96	3.33	3.70	4.07	4.44	4.81	5.18	5.55	5.92	6.29	6.66	7.03	7.40	7.77	8.14	8.51
1263	0.190	0.42	0.84	1.26	1.68	2.10	2.52	2.94	3.36	3.78	4.20	4.62	5.04	5.46	5.88	6.30	6.72	7.14	7.56	7.98	8.40	8.82	9.24	9.66
1363	0.206	0.46	0.92	1.38	1.84	2.30	2.76	3.22	3.68	4.14	4.60	5.06	5.52	5.98	6.44	6.90	7.36	7.82	8.28	8.74	9.20	9.66	10.12	10.58
1463	0.222	0.51	1.02	1.53	2.04	2.55	3.06	3.57	4.08	4.59	5.10	5.61	6.12	6.63	7.14	7.65	8.16	8.67	9.18	9.69	10.20	10.71	11.22	11.73
1563	0.238	0.56	1.11	1.66	2.21	2.76	3.31	3.86	4.41	4.96	5.51	6.06	6.61	7.16	7.71	8.26	8.81	9.36	9.91	10.46	11.01	11.56	12.11	12.66
1663	0.254	0.62	1.24	1.81	2.38	2.95	3.52	4.09	4.66	5.23	5.80	6.37	6.94	7.51	8.08	8.65	9.22	9.79	10.36	10.93	11.50	12.07	12.64	13.21

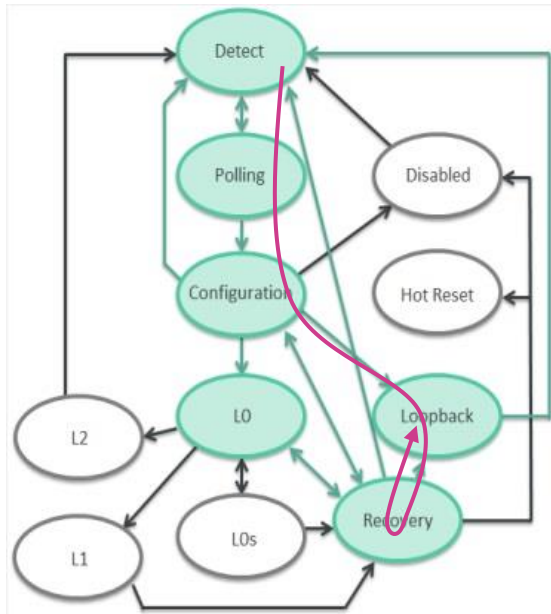
PCI Express Gen5 Link Training

Stress Signal Calibration

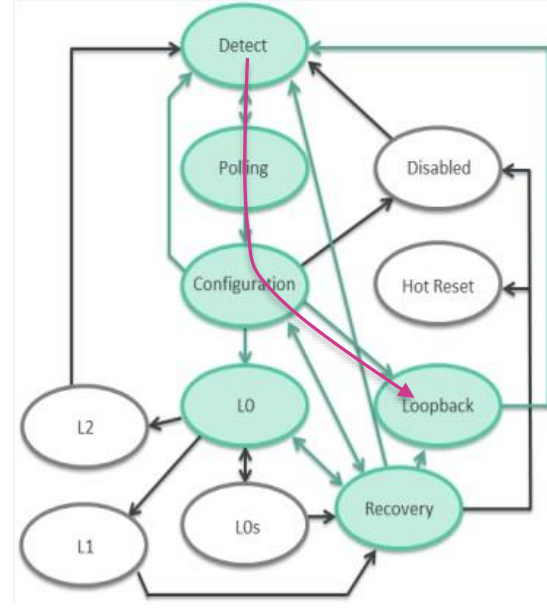
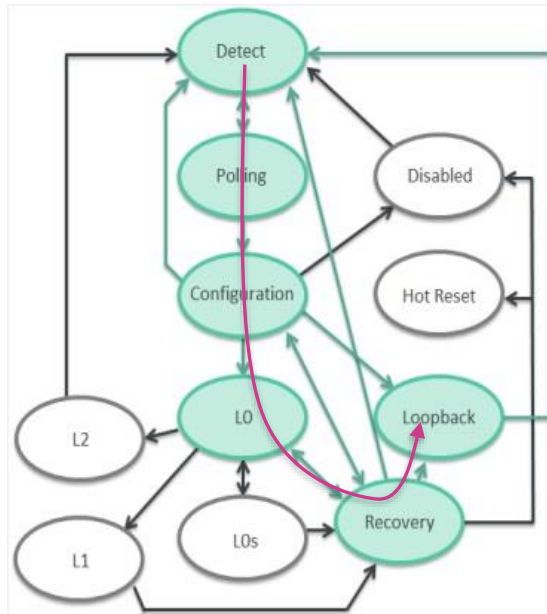
Transition to Loopback Status

Stress Signal Input Test

New for 32 GT/s



8, 16, and 32 GT/s (Legacy)



PCI Express Gen5 Link Training



LTSSM Log Viewer

LTSSM Trigger

Capture problematic event

Time [ns]	ΔTime [ns]	State	Speed[Gt/s]	Detect Preset	Error Count	Use Preset	Preset	Pre-cursor	Cursor	Post-cursor	FS	LF
440,750,376	4	RECOVERY_RCVR_LOCK	16.0	---	---	---	---	---	---	---	---	---
440,750,380	1,153,864	RECOVERY_EQUALIZATION_PHASE0	16.0	---	---	---	---	---	---	---	24	8
441,904,244	8	RECOVERY_EQUALIZATION_PHASE0	16.0	---	---	---	---	---	---	---	24	8
441,904,252	2,848	RECOVERY_EQUALIZATION_PHASE1	16.0	---	---	---	---	---	---	---	---	---
441,907,100	272	RECOVERY_EQUALIZATION_PHASE2	16.0	0 (MP1900A => DUT)	0	1 (Preset)	P6	3	21	0	---	---
441,907,372	1,999,728	RECOVERY_EQUALIZATION_PHASE2	16.0	1 (MP1900A <= DUT)	0	1 (Preset)	P6	3	21	0	---	---
443,907,100	2,864	RECOVERY_EQUALIZATION_PHASE2	16.0	0 (MP1900A => DUT)	0	1 (Preset)	P4	0	24	0	---	---
443,909,964	2,000,000	RECOVERY_EQUALIZATION_PHASE2	16.0	1 (MP1900A <= DUT)	0	1 (Preset)	P4	0	24	0	---	---
445,909,964	2,860	RECOVERY_EQUALIZATION_PHASE3	16.0	0 (MP1900A => DUT)	0	1 (Preset)	P5	2	22	0	---	---
445,912,824	4	RECOVERY_EQUALIZATION_PHASE3	16.0	1 (MP1900A <= DUT)	0	1 (Preset)	P5	2	22	0	---	---
445,912,828	1,999,980	RECOVERY_EQUALIZATION_PHASE3	16.0	0 (MP1900A => DUT)	0	1 (Preset)	P5	2	22	0	---	---
447,912,808	4	RECOVERY_EQUALIZATION_PHASE3	16.0	1 (MP1900A <= DUT)	0	1 (Preset)	P4	0	24	0	---	---
447,912,812	2,002,840	RECOVERY_EQUALIZATION_PHASE3	16.0	0 (MP1900A => DUT)	0	1 (Preset)	P4	0	24	0	---	---
449,915,652	64	RECOVERY_RCVR_LOCK	16.0	---	---	---	---	---	---	---	---	---
449,915,716	2,980	RECOVERY_RCVR_CFG_TS2	16.0	---	---	---	---	---	---	---	---	---
449,918,696	508	RECOVERY_IDLE	16.0	---	---	---	---	---	---	---	---	---
449,919,204	12	RECOVERY_LO	16.0	---	---	---	---	---	---	---	---	---
449,919,216	2,420	RECOVERY_RCVR_LOCK	16.0	---	---	---	---	---	---	---	---	---
449,921,636	6,553,832	RECOVERY_RCVR_CFG_EQT32	16.0	---	---	---	---	---	---	---	---	---
456,475,468	100,016	RECOVERY_SPEED	16.0	---	---	---	---	---	---	---	---	---
456,575,484	32	RECOVERY_SPEED	32.0	---	---	---	---	---	---	---	---	---
456,575,516	4	RECOVERY_RCVR_LOCK	32.0	---	---	---	---	---	---	---	---	---
456,575,520	1,213,648	RECOVERY_EQUALIZATION_PHASE0	32.0	---	---	---	---	---	---	---	24	8
457,789,168	8	RECOVERY_EQUALIZATION_PHASE0	32.0	---	---	---	---	---	---	---	24	8
457,789,176	1,892	RECOVERY_EQUALIZATION_PHASE1	32.0	---	---	---	---	---	---	---	---	---
457,791,068	264	RECOVERY_EQUALIZATION_PHASE2	32.0	0 (MP1900A => DUT)	0	1 (Preset)	P6	3	21	0	---	---
457,791,332	1,999,736	RECOVERY_EQUALIZATION_PHASE2	32.0	1 (MP1900A <= DUT)	0	1 (Preset)	P6	3	21	0	---	---
459,791,068	1,912	RECOVERY_EQUALIZATION_PHASE2	32.0	0 (MP1900A => DUT)	0	1 (Preset)	P4	0	24	0	---	---
459,792,980	2,000,000	RECOVERY_EQUALIZATION_PHASE2	32.0	1 (MP1900A <= DUT)	0	1 (Preset)	P4	0	24	0	---	---
461,792,980	1,912	RECOVERY_EQUALIZATION_PHASE3	32.0	0 (MP1900A => DUT)	0	1 (Preset)	P5	2	22	0	---	---
461,794,892	4	RECOVERY_EQUALIZATION_PHASE3	32.0	1 (MP1900A <= DUT)	0	1 (Preset)	P5	2	22	0	---	---
461,794,896	2,000,004	RECOVERY_EQUALIZATION_PHASE3	32.0	0 (MP1900A => DUT)	0	1 (Preset)	P5	0	24	0	---	---
463,794,900	4	RECOVERY_EQUALIZATION_PHASE3	32.0	1 (MP1900A <= DUT)	0	1 (Preset)	P4	0	24	0	---	---
463,794,904	2,001,908	RECOVERY_EQUALIZATION_PHASE3	32.0	0 (MP1900A => DUT)	0	1 (Preset)	P4	0	24	0	---	---
465,796,812	32	RECOVERY_RCVR_LOCK	32.0	---	---	---	---	---	---	---	---	---
465,796,844	1,948	RECOVERY_RCVR_CFG_TS2	32.0	---	---	---	---	---	---	---	---	---
465,798,792	524	LOOPBACK_ENTRY_MASTER_TS1	32.0	---	---	---	---	---	---	---	---	---
465,799,316	0	LOOPBACK_ACTIVE_MASTER	32.0	---	---	---	---	---	---	---	---	---

Option

State Machine SKP Link EQ PPG/ED Trigger

PPG Aux Output Trigger

Trigger LTSSM

State Loopback.Active.Master

Link Speed 16.0 G

Change Preset Send Preset value in Recovery.EQ.Phase3

Trigger - Bus

Trigger Type Bus

Bus B1

Trigger On Pattern

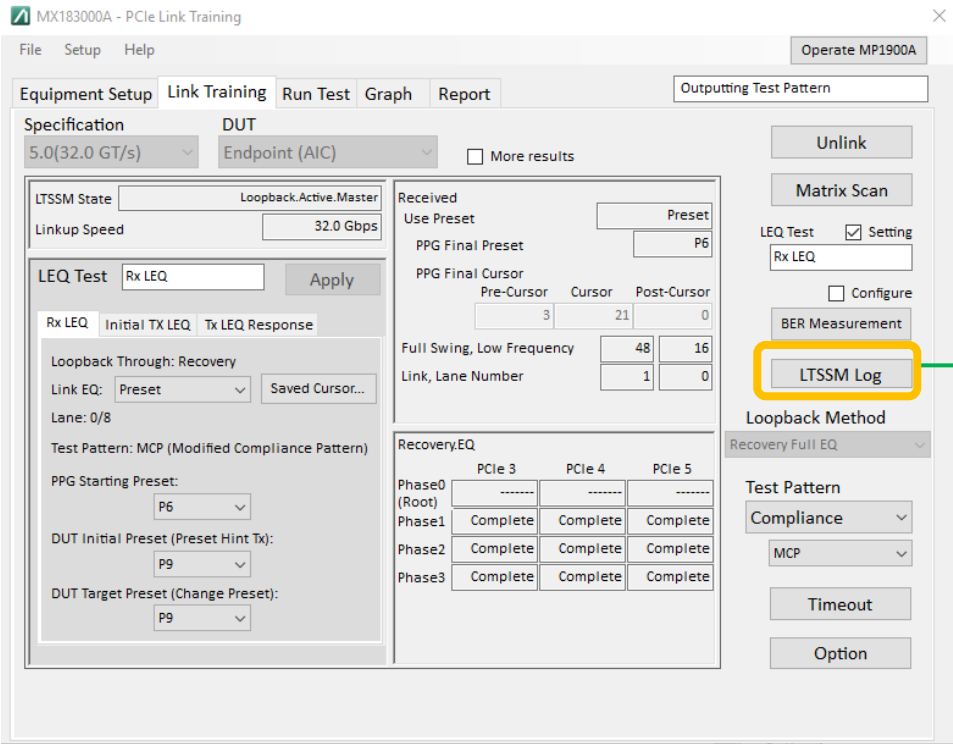
Bus Type 8b10b

Character

MSB	X	X	X	X
	X	X	X	X
	X	X	X	X
	X	X	X	X

Disparity Either

Debugging with BERT: Training Log Viewer



Time [ns]	ΔTime [ns]	State	Speed[GT/s]	Detect Preset	Error Count	Use Preset	Preset	Pre-cursor	Cursor	Post-cursor	FS	LF
440,750,376	4	RECOVERY_RCVR_LOCK	16.0	---	---	---	---	---	---	---	---	---
440,750,380	1,153,864	RECOVERY_EQUALIZATION_PHASE2	16.0	---	---	---	---	---	---	---	24	8
441,904,244	8	RECOVERY_EQUALIZATION_PHASE2	16.0	---	---	---	---	---	---	---	24	8
441,904,252	2,848	RECOVERY_EQUALIZATION_PHASE1	16.0	---	---	---	---	---	---	---	---	---
441,907,100	272	RECOVERY_EQUALIZATION_PHASE2	16.0	0 (MP1900A => DUT)	0	1 (Preset)	P6	3	21	0	---	---
441,907,372	1,999,728	RECOVERY_EQUALIZATION_PHASE2	16.0	1 (MP1900A <== DUT)	0	1 (Preset)	P6	3	21	0	---	---
443,907,100	2,864	RECOVERY_EQUALIZATION_PHASE2	16.0	0 (MP1900A => DUT)	0	1 (Preset)	P4	0	24	0	---	---
443,909,964	2,000,000	RECOVERY_EQUALIZATION_PHASE2	16.0	1 (MP1900A <== DUT)	0	1 (Preset)	P4	0	24	0	---	---
445,909,964	2,860	RECOVERY_EQUALIZATION_PHASE3	16.0	0 (MP1900A => DUT)	0	1 (Preset)	P5	2	22	0	---	---
445,912,824	4	RECOVERY_EQUALIZATION_PHASE3	16.0	1 (MP1900A <== DUT)	0	1 (Preset)	P5	2	22	0	---	---
445,912,828	1,999,980	RECOVERY_EQUALIZATION_PHASE3	16.0	0 (MP1900A => DUT)	0	1 (Preset)	P5	2	22	0	---	---
447,912,808	4	RECOVERY_EQUALIZATION_PHASE3	16.0	1 (MP1900A <== DUT)	0	1 (Preset)	P4	0	24	0	---	---
447,912,812	2,002,840	RECOVERY_EQUALIZATION_PHASE3	16.0	0 (MP1900A => DUT)	0	1 (Preset)	P4	0	24	0	---	---
449,915,652	64	RECOVERY_RCVR_LOCK	16.0	---	---	---	---	---	---	---	---	---
449,915,716	2,980	RECOVERY_RCVR_LOCK	16.0	---	---	---	---	---	---	---	---	---
449,918,696	508	RECOVERY_RCVR_LOCK	16.0	---	---	---	---	---	---	---	---	---
449,919,204	12	RECOVERY_RCVR_LOCK	16.0	---	---	---	---	---	---	---	---	---
449,919,216	2,420	RECOVERY_RCVR_LOCK	16.0	---	---	---	---	---	---	---	---	---
449,921,636	6,553,832	RECOVERY_RCVR_LOCK	16.0	---	---	---	---	---	---	---	---	---
456,475,468	100,016	RECOVERY_RCVR_LOCK	16.0	---	---	---	---	---	---	---	---	---
456,575,484	32	RECOVERY_RCVR_LOCK	16.0	---	---	---	---	---	---	---	---	---
456,575,516	4	RECOVERY_RCVR_LOCK	16.0	---	---	---	---	---	---	---	---	---
456,575,520	1,213,648	RECOVERY_RCVR_LOCK	16.0	---	---	---	---	---	---	---	---	---
457,789,168	8	RECOVERY_RCVR_LOCK	16.0	---	---	---	---	---	---	---	---	---
457,789,176	1,892	RECOVERY_RCVR_LOCK	16.0	---	---	---	---	---	---	---	---	---
457,791,068	264	RECOVERY_RCVR_LOCK	16.0	---	---	---	---	---	---	---	---	---
457,791,332	1,999,736	RECOVERY_RCVR_LOCK	16.0	---	---	---	---	---	---	---	---	---
459,791,068	1,912	RECOVERY_RCVR_LOCK	16.0	---	---	---	---	---	---	---	---	---
459,792,980	2,000,000	RECOVERY_RCVR_LOCK	16.0	---	---	---	---	---	---	---	---	---
461,792,980	1,912	RECOVERY_RCVR_LOCK	16.0	---	---	---	---	---	---	---	---	---
461,794,892	4	RECOVERY_RCVR_LOCK	16.0	---	---	---	---	---	---	---	---	---
461,794,896	2,000,004	RECOVERY_RCVR_LOCK	16.0	---	---	---	---	---	---	---	---	---
463,794,900	4	RECOVERY_RCVR_LOCK	16.0	---	---	---	---	---	---	---	---	---
463,794,904	2,001,908	RECOVERY_RCVR_LOCK	16.0	---	---	---	---	---	---	---	---	---
465,796,812	32	RECOVERY_RCVR_LOCK	16.0	---	---	---	---	---	---	---	---	---
465,796,844	1,948	RECOVERY_RCVR_LOCK	16.0	---	---	---	---	---	---	---	---	---
465,798,792	524	LOOPBACK_ACTIVE_MASTER	16.0	---	---	---	---	---	---	---	---	---
465,799,316	0	LOOPBACK_ACTIVE_MASTER	16.0	---	---	---	---	---	---	---	---	---

Time [ns]	ΔTime [...]	State	Speed[GT/s]	Detect Pre
0	0	INITIAL	16.0	
17280	17280	DETECT_QUITE	16.0	
12017280	12000000	DETECT_ACTIVE	16.0	
12017296	16	POLLING_ACTIVE_TS1	16.0	
36017296	24000000	INITIAL	16.0	
36017312	16	DETECT_QUITE	16.0	
48017312	12000000	DETECT_ACTIVE	16.0	
48017328	16	POLLING_ACTIVE_TS1	16.0	
72017328	24000000	INITIAL	16.0	
72017344	16	DETECT_QUITE	16.0	
84017344	12000000	DETECT_ACTIVE	16.0	
84017360	16	POLLING_ACTIVE_TS1	16.0	
108017360	24000000	INITIAL	16.0	

- The MP1900A Training Log Viewer function can display the actual Training State transition logs.
- The state transition path (route) and transition times can be analyzed in detail.

LTSSM Details

Training Log Viewer													
Time [ns]	Δ Time [ns]	State	Speed[GT/s]	Detect Preset	Error Count	Use Preset	Preset	Pre-cursor	Cursor	Post-cursor	FS	LF	
440,750,376	4	RECOVERY_RCVR_LOCK	16.0	---	---	---	---	---	---	---	---	---	---
440,750,380	1,153,864	RECOVERY_EQUALIZATION_PHASE0	16.0	---	---	---	---	---	---	---	24	8	
441,904,244	8	RECOVERY_EQUALIZATION_PHASE0	16.0	---	---	---	---	---	---	---	24	8	
441,904,252	2,848	RECOVERY_EQUALIZATION_PHASE1	16.0	---	---	---	---	---	---	---	---	---	
441,907,100	272	RECOVERY_EQUALIZATION_PHASE2	16.0	0 (MP1900A ==> DUT)	0	1 (Preset)	P6	3	21	0	---	---	
441,907,372	1,999,728	RECOVERY_EQUALIZATION_PHASE2	16.0	1 (MP1900A <== DUT)	0	1 (Preset)	P6	3	21	0	---	---	
443,907,100	2,864	RECOVERY_EQUALIZATION_PHASE2	16.0	0 (MP1900A ==> DUT)	0	1 (Preset)	P4	0	24	0	---	---	
443,909,964	2,000,000	RECOVERY_EQUALIZATION_PHASE2	16.0	1 (MP1900A <== DUT)	0	1 (Preset)	P4	0	24	0	---	---	
445,909,964	2,860	RECOVERY_EQUALIZATION_PHASE3	16.0	0 (MP1900A ==> DUT)	0	1 (Preset)	P5	2	22	0	---	---	
445,912,824	4	RECOVERY_EQUALIZATION_PHASE3	16.0	1 (MP1900A <== DUT)	0	1 (Preset)	P5	2	22	0	---	---	
445,912,828	1,999,980	RECOVERY_EQUALIZATION_PHASE3	16.0	0 (MP1900A ==> DUT)	0	1 (Preset)	P5	2	22	0	---	---	
447,912,808	4	RECOVERY_EQUALIZATION_PHASE3	16.0	1 (MP1900A <== DUT)	0	1 (Preset)	P4	0	24	0	---	---	
447,912,812	2,002,840	RECOVERY_EQUALIZATION_PHASE3	16.0	0 (MP1900A ==> DUT)	0	1 (Preset)	P4	0	24	0	---	---	
449,915,652	64	RECOVERY_RCVR_LOCK	16.0	---	---	---	---	---	---	---	---	---	
449,915,716	2,980	RECOVERY_RCVR_CFG_TS2	16.0	---	---	---	---	---	---	---	---	---	
449,918,696	508	RECOVERY_IDLE	16.0	---	---	---	---	---	---	---	---	---	
449,919,204	12	L0	16.0	---	---	---	---	---	---	---	---	---	
449,919,216	2,420	RECOVERY_RCVR_LOCK	16.0	---	---	---	---	---	---	---	---	---	
449,921,636	6,553,832	RECOVERY_RCVR_CFG_EQTS2	16.0	---	---	---	---	---	---	---	---	---	
456,475,468	100,016	RECOVERY_SPEED	16.0	---	---	---	---	---	---	---	---	---	
456,575,484	32	RECOVERY_SPEED	32.0	---	---	---	---	---	---	---	---	---	
456,575,516	4	RECOVERY_RCVR_LOCK	32.0	---	---	---	---	---	---	---	---	---	
456,575,520	1,213,648	RECOVERY_EQUALIZATION_PHASE0	32.0	---	---	---	---	---	---	---	24	8	
457,789,168	8	RECOVERY_EQUALIZATION_PHASE0	32.0	---	---	---	---	---	---	---	24	8	
457,789,176	1,892	RECOVERY_EQUALIZATION_PHASE1	32.0	---	---	---	---	---	---	---	---	---	
457,791,068	264	RECOVERY_EQUALIZATION_PHASE2	32.0	0 (MP1900A ==> DUT)	0	1 (Preset)	P6	3	21	0	---	---	
457,791,332	1,999,736	RECOVERY_EQUALIZATION_PHASE2	32.0	1 (MP1900A <== DUT)	0	1 (Preset)	P6	3	21	0	---	---	
459,791,068	1,912	RECOVERY_EQUALIZATION_PHASE2	32.0	0 (MP1900A ==> DUT)	0	1 (Preset)	P4	0	24	0	---	---	
459,792,980	2,000,000	RECOVERY_EQUALIZATION_PHASE2	32.0	1 (MP1900A <== DUT)	0	1 (Preset)	P4	0	24	0	---	---	
461,792,980	1,912	RECOVERY_EQUALIZATION_PHASE3	32.0	0 (MP1900A ==> DUT)	0	1 (Preset)	P5	2	22	0	---	---	
461,794,892	4	RECOVERY_EQUALIZATION_PHASE3	32.0	1 (MP1900A <== DUT)	0	1 (Preset)	P5	2	22	0	---	---	
461,794,896	2,000,004	RECOVERY_EQUALIZATION_PHASE3	32.0	0 (MP1900A ==> DUT)	0	1 (Preset)	P5	0	24	0	---	---	
463,794,900	4	RECOVERY_EQUALIZATION_PHASE3	32.0	1 (MP1900A <== DUT)	0	1 (Preset)	P4	0	24	0	---	---	
463,794,904	2,001,908	RECOVERY_EQUALIZATION_PHASE3	32.0	0 (MP1900A ==> DUT)	0	1 (Preset)	P4	0	24	0	---	---	
465,796,812	32	RECOVERY_RCVR_LOCK	32.0	---	---	---	---	---	---	---	---	---	
465,796,844	1,948	RECOVERY_RCVR_CFG_TS2	32.0	---	---	---	---	---	---	---	---	---	
465,798,792	524	LOOPBACK_ENTRY_MASTER_TS1	32.0	---	---	---	---	---	---	---	---	---	
465,799,316	0	LOOPBACK_ACTIVE_MASTER	32.0	---	---	---	---	---	---	---	---	---	

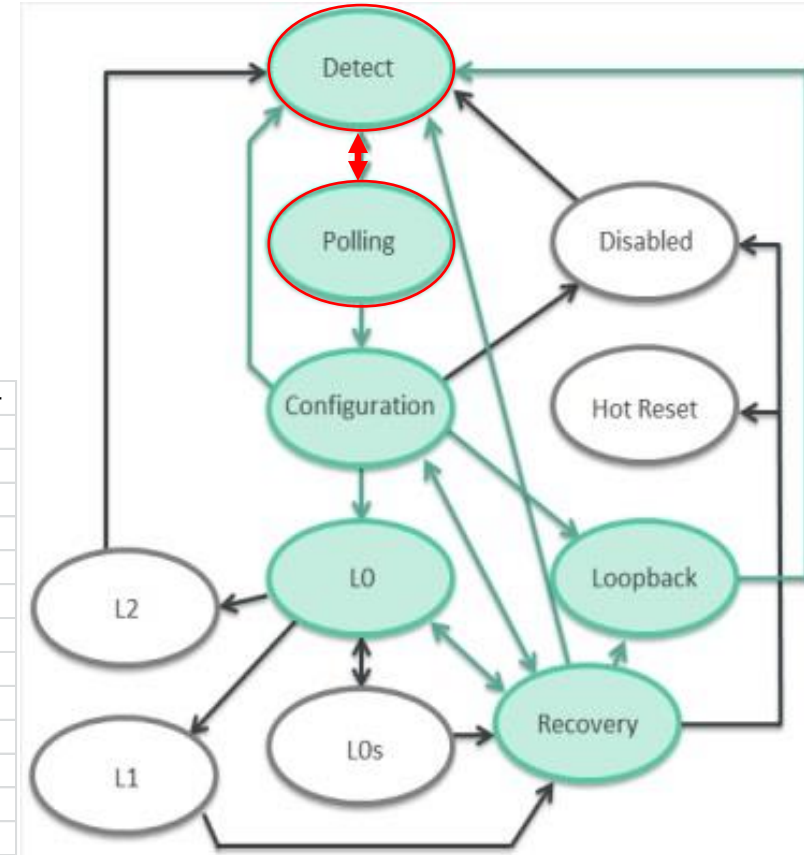


Troubleshoot: 2.5GT/s Link Failure

90% of this case, No signal or no reference clock.
Check the cable connection and polarity

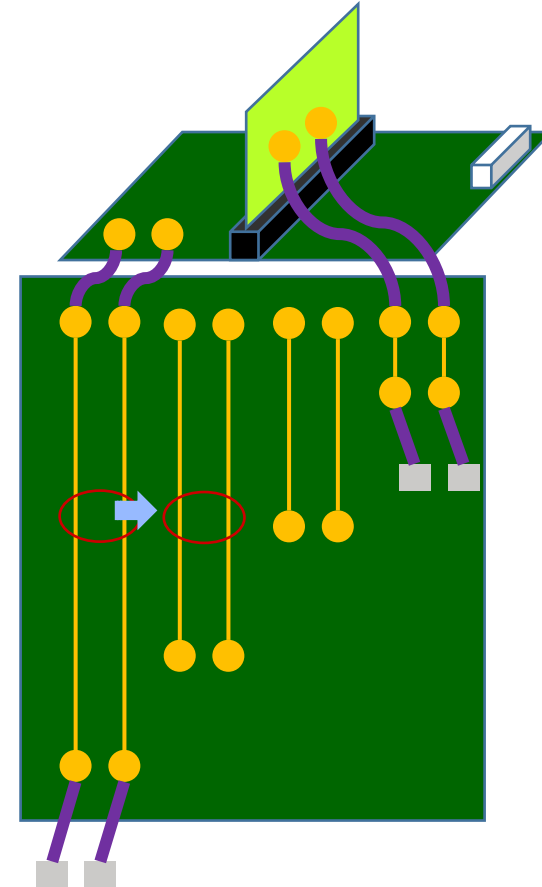
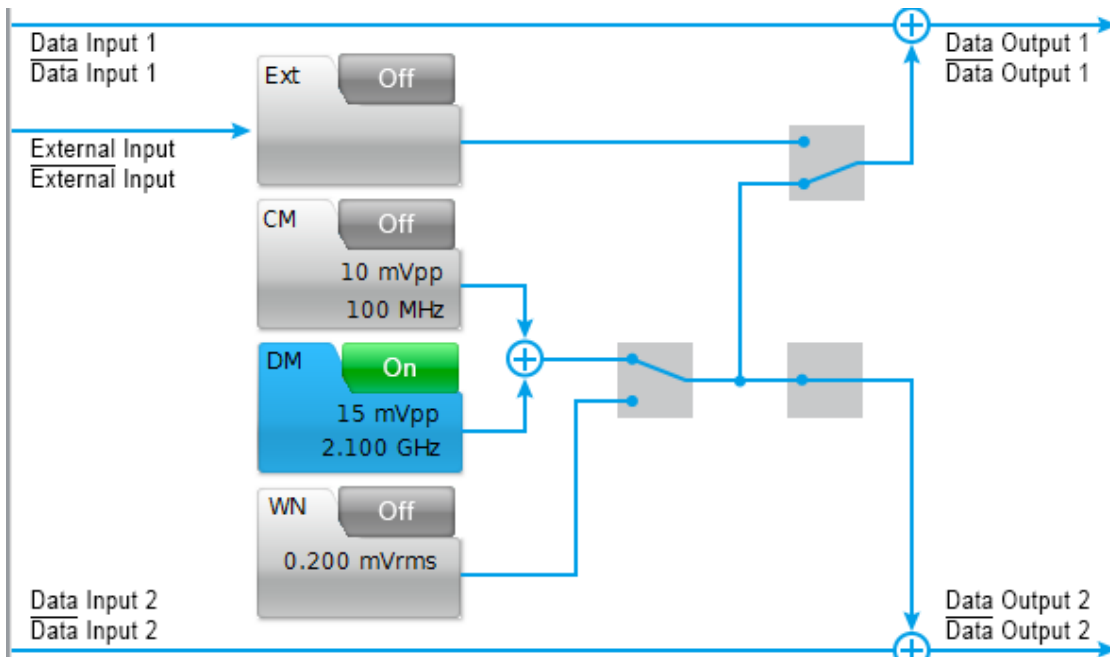
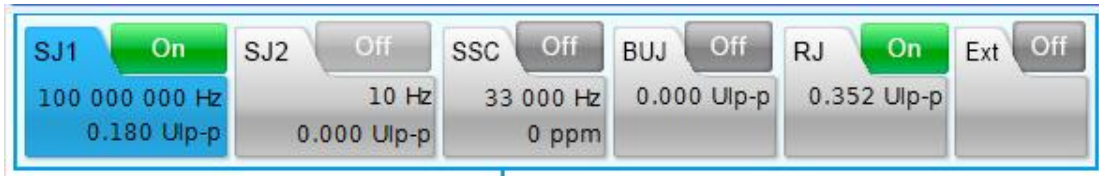
- LTSSM times-out at Polling Active and repeatedly performs the operation for returning to Detect.
- Gen1 2.5 GT/s Symbol Lock is not obtained.

Time[ns]	Delta Time[ns]	State	Speed[GT/s]	Detect Preset	Error Count	Use Preset	Preset	Pre-cursor	Cursor	Post-cursor
0	13552	INITIAL	8	----	----	----	----	----	----	----
13552	8738088	DETECT_QUIET	8	----	----	----	----	----	----	----
8751640	3261912	DETECT_QUIET	2.5	----	----	----	----	----	----	----
12013552	16	DETECT_ACTIVE	2.5	----	----	----	----	----	----	----
12013568	24000000	POLLING_ACTIVE_TS1	2.5	----	----	----	----	----	----	----
36013568	16	INITIAL	2.5	----	----	----	----	----	----	----
36013584	12000000	DETECT_QUIET	2.5	----	----	----	----	----	----	----
48013584	16	DETECT_ACTIVE	2.5	----	----	----	----	----	----	----
48013600	24000000	POLLING_ACTIVE_TS1	2.5	----	----	----	----	----	----	----
72013600	16	INITIAL	2.5	----	----	----	----	----	----	----
72013616	12000000	DETECT_QUIET	2.5	----	----	----	----	----	----	----
84013616	16	DETECT_ACTIVE	2.5	----	----	----	----	----	----	----
84013632	24000000	POLLING_ACTIVE_TS1	2.5	----	----	----	----	----	----	----
108013632	16	INITIAL	2.5	----	----	----	----	----	----	----
108013648	12000000	DETECT_QUIET	2.5	----	----	----	----	----	----	----
120013648	16	DETECT_ACTIVE	2.5	----	----	----	----	----	----	----
120013664	24000000	POLLING_ACTIVE_TS1	2.5	----	----	----	----	----	----	----

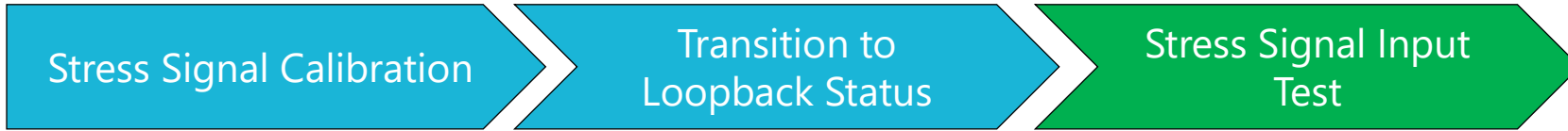


Troubleshoot : Never Become Error-Free

Reduce/Kill the stress: DMI, CMI, SJ, RJ, ISI Loss Channel
Still Error? Check the return path.



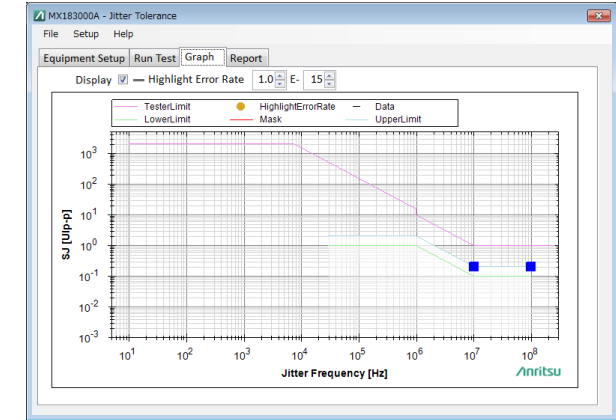
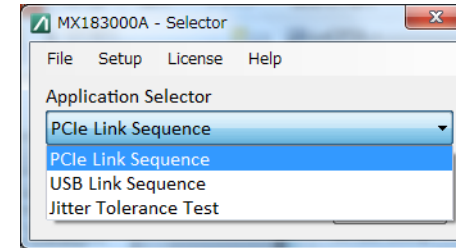
PCI Express Gen5 Rx JTOL Test



Stress Signal Input Test (Jitter Tolerance Margin Test)

Automated Jitter Control and Tolerance Measurement

- Impresses SJ and Tests PHY Device Jitter Tolerance
- Tests Device Margin using Low BER Estimation
- Outputs Measurement Results in HTML and CSV Formats



Item	MX183000A-PL001 Specifications
Direction Search	Binary, Downward Linear, Downward Log, Upward Linear, Upward Log, Binary + Linear
Detection	Error Rate, Error Count, Estimate, FEC Uncorrectable Burst Error
Error Threshold	1.0E-3 to 1.0E-14
Highlight Error Rate	9.9E-9 to 1.0E-20 (at estimate)
Report Function	Reports results in HTML and CSV formats

Jitter Tolerance Test Example

Equipment Setup | Link Training | **Run Test** | Graph | Report | Outputting Test Pattern

Check All | Measurement Completed. | Detail | Run Test

Uncheck All

No.	Jitter Freq. [Hz]	Mask [UI]	Upper Limit [UI]	Lower Limit [UI]	Meas. [UI]	Meas. Judge	Esti
<input checked="" type="checkbox"/>	100,000,000	0.100	0.200	0.100	0.160	PASS	
<input checked="" type="checkbox"/>	10,000,000	0.100	0.200	0.100	0.200	PASS	
<input checked="" type="checkbox"/>	1,000,000	1.000	2.000	1.000	1.600	PASS	
<input checked="" type="checkbox"/>	30,000	1.000	2.000	1.000	2.000	PASS	

Jitter Freq.[Hz] 10 | Add | Save | Open | Bit Rate 16.000000 Gbit/s

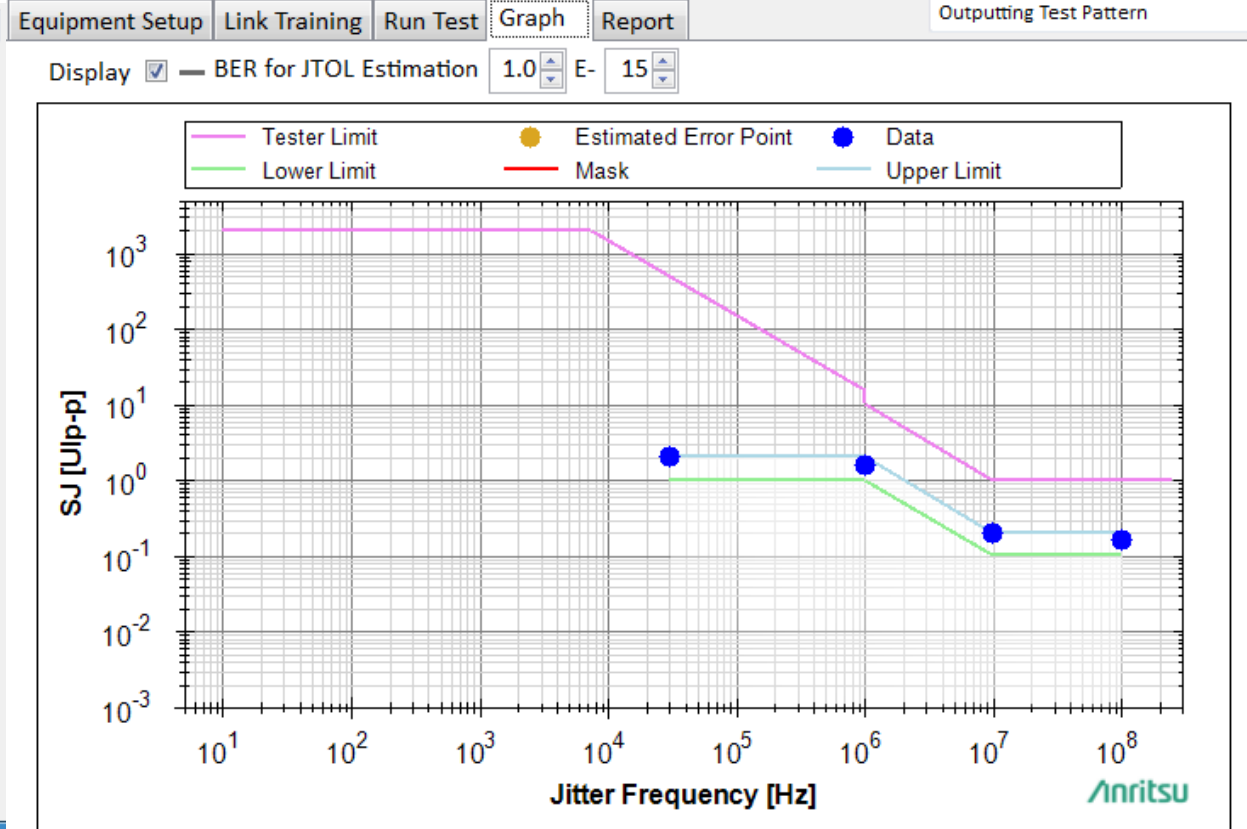
Mask [UI] 1.000 | Delete | Title PCIe_CC | Clock Selection Clock and Data Recovery

Upper Limit [UI] 2.000 | All Clear

Lower Limit [UI] 1.000

Upper Ratio 2.000 | Measurement Sequence From higher Freq. side | JTOL Settings

Lower Ratio 1.000 | Set All Limit



Anritsu/Tek Stressed Eye Calibration Demonstration Video