Tektronix

Anritsu
envision : ensure

PCI Express® Gen 5: Solving 32 GT/s Receiver Compliance and Validation Challenges

3/2/2021

Agenda

1	2	3	4
PCI Express Specification Update	Challenges and latest Rx Guidelines	Anritsu & Tektronix PCIe Solutions	Questions

PCI Express Specification Update

PCIe® 4.0 to 6.0 Base Specification Changes

	PCIe 4.0	PCIe 5.0	PCIe 6.0 (TBD)
Data Rate	16 GT/s	32 GT/s	64 GT/s (PAM4)
Add-in Card Loss	8dB @ 8Ghz	9.5dB @ 16GHz	TBD
Rx Test (Channel Loss)	- (27 to 30) dB @ 8GHz	- (34 to 37) dB @ 16GHz	- (30 to 33) dB @ 16GHz
Reference CTLE	2 Poles; 1 Zero; DC Gain Range (-6 to -12) dB	4 Poles; 2 Zero; DC Gain Range (-5 to -15) dB	6 Poles; 3 Zero; DC Gain Range (-5 to -15) dB
Reference DFE	2-Taps	3-Taps	16-Taps
Eye Width (Rx Test)	18.75 ps	9.375 ps	3.125 ps (top eye)
Eye Height (Rx Test)	15 mV	15 mV	6 mV (top eye)
Lane Margining	Required timing only	Required timing/voltage	Required timing/voltage
Refclk Jitter Limits	<= 500 fs	<= 150 fs	<=100 fs

PCIe 6.0 Specification Snapshot

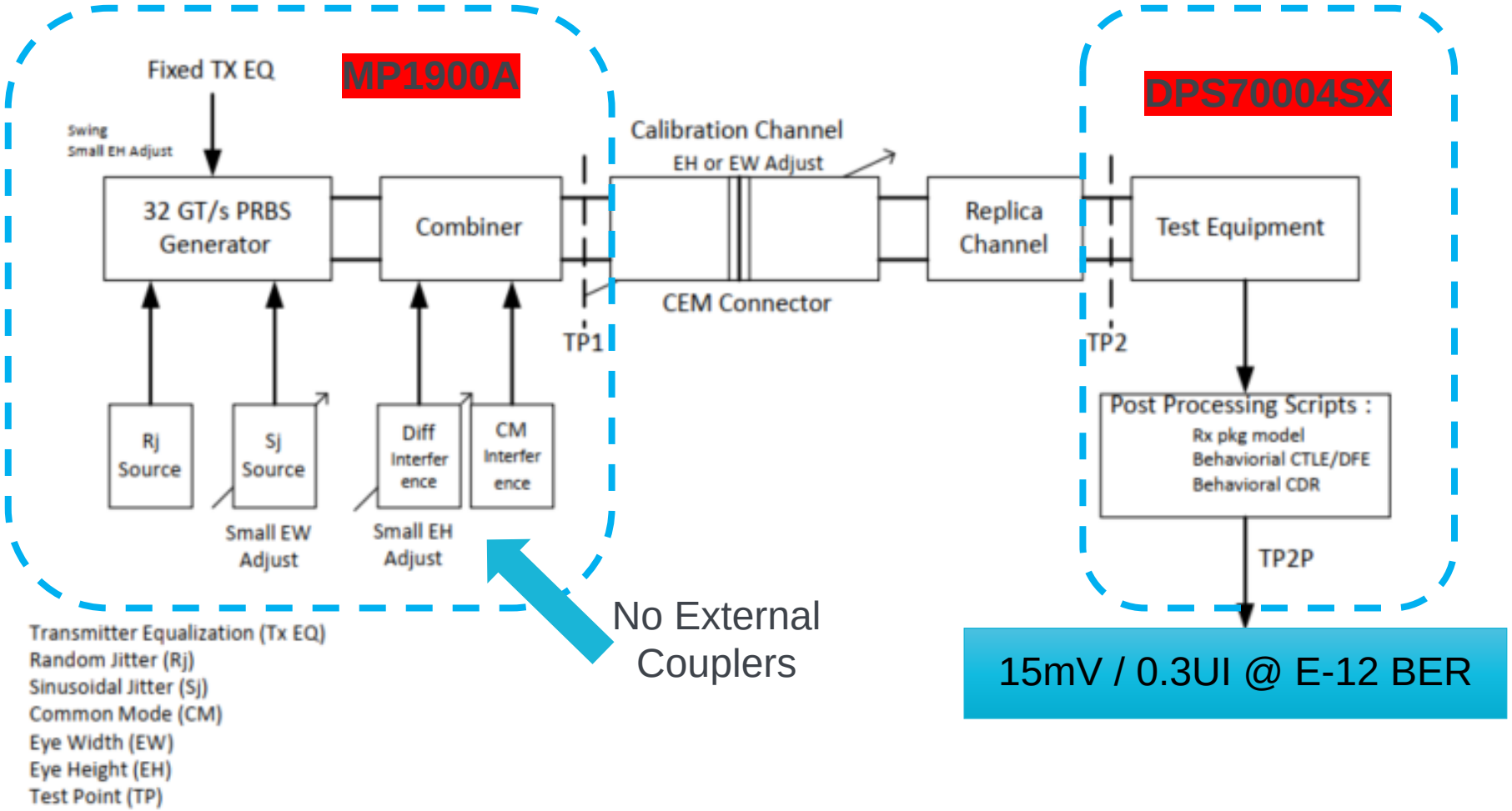
- **PCIe 6.0 Base Specification – Rev 0.7 workgroup approved**
  - Describes chip-level behavior on all levels of the stack
- **PCIe 6.0 CEM Specification – Rev 0.3 workgroup approved**
  - Card electro-mechanical (CEM) defines system and Add-in Card level
- **PCIe 6.0 PHY Test Specification – Rev 0.3 workgroup approved**
  - Describes electrical compliance tests for Tx, Rx LEQ, & PLL Bandwidth

PCIe 5.0 Specification Snapshot

- **PCIe 5.0 Base Specification – Rev 1.0 Released (Q2 2019)**
  - Describes chip-level behavior on all levels of the stack
- **PCIe 5.0 CEM Specification – Rev 1.0 workgroup approved**
  - Card electro-mechanical (CEM) defines system and Add-in Card level
- **PCIe 5.0 PHY Test Specification – Rev 0.5 workgroup approved**
  - Describes electrical compliance tests for Tx, Rx LEQ, & PLL Bandwidth
- **PCIe 4.0 – All Specifications at Rev 1.0**
  - Integrators List testing began August 2019

Challenges and Latest Rx Guidelines

32 GT/s Rx Stressed Eye Calibration



Calibration Nuances at 32 GT/s

TP1 to TP3 Cable

- Cable used from BERT to Scope for Amp/Tx EQ/Rj/Sj calibration
- 16 GT/s – cable counted in Rx channel range of 27dB to 30dB
- 32 GT/s – cable excluded in Rx channel range of 34dB to 37dB

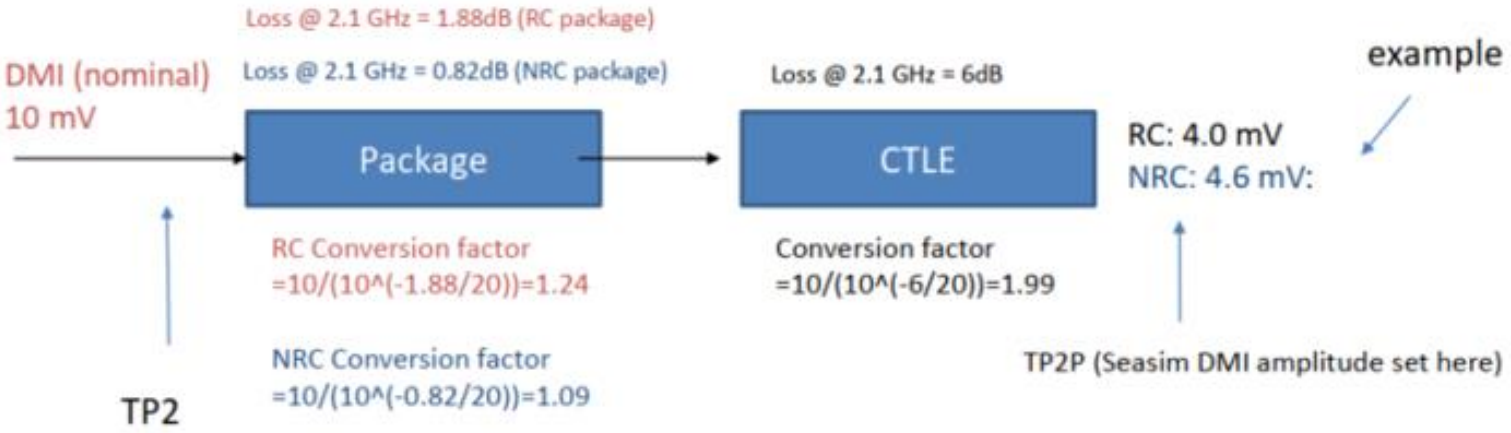
SigTest & Seasim

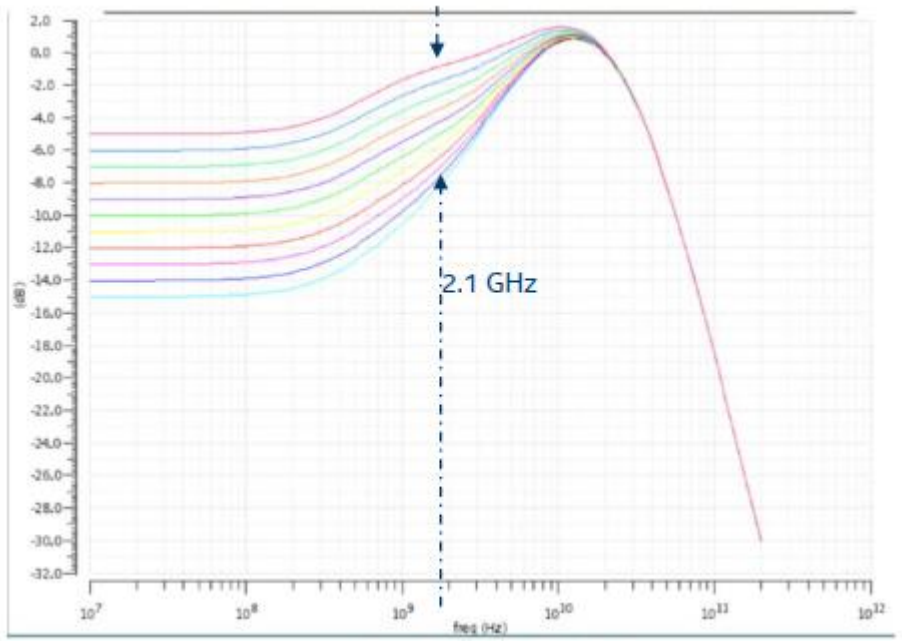
- Seasim - stress & noise in simulation
- SigTest (closed loop) – stress & noise intrinsic to waveform
- Seasim – requires characterizing BERT pulse width jitter

Tie Breakers

- Multiple solutions for stressed eye
- 1st – pick solution with highest channel loss
- 2nd – pick solution with EH closest to 15.0 mV
- If no solutions exist amplitude can be swept from 720mV to 800mV

Differential Mode Test Point Conversion





Root Complex (RC)
Non-Root Complex (NRC)

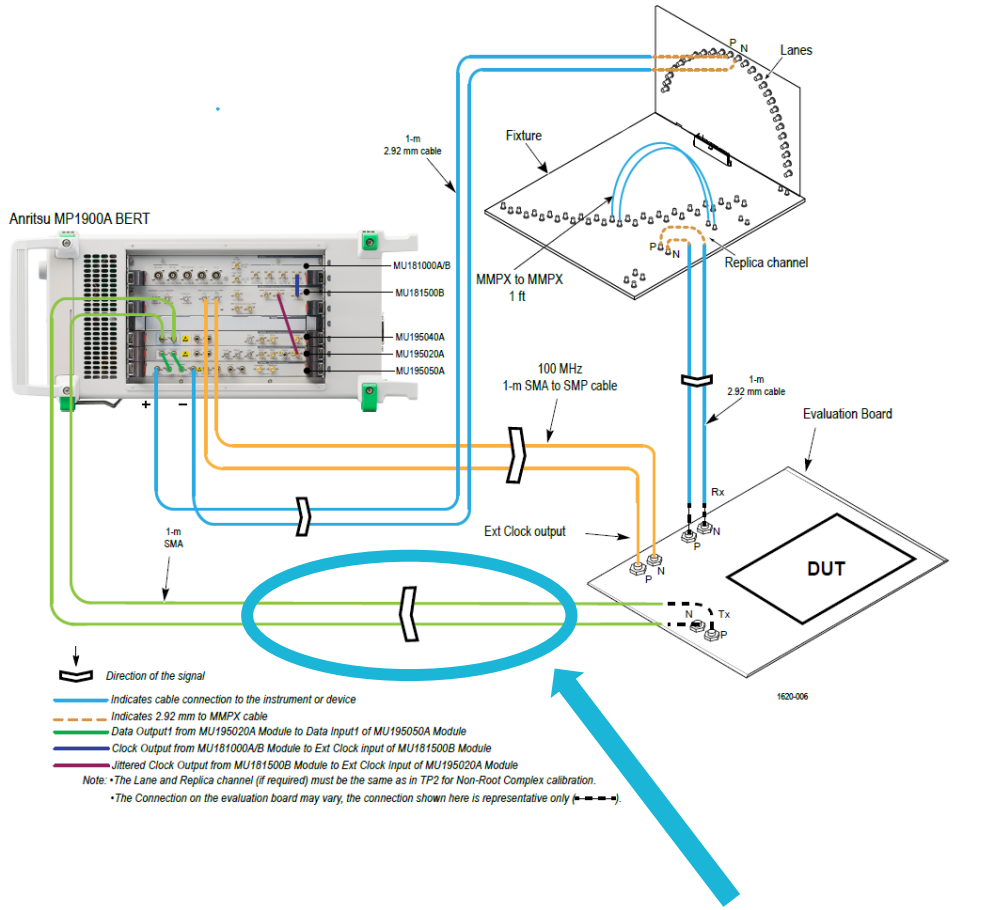
(Nominal DMI value based on PCIe 5.0 Rev 0.7 spec)

CTLE Curve	-15	-14	-13	-12	-11	-10	-9	-8	-7	-6	-5
Loss @ 2.1 GHz	-7.1656	-6.74485	-6.26725	-5.73227	-5.14069	-4.49494	-3.79846	-3.05574	-2.27145	-1.45083	-0.59882
CTLE conversion Factor	2.281813	2.173915	2.057607	1.934699	1.807318	1.677826	1.548542	1.421631	1.29889	1.181793	1.071374
RC Package Conversion Factor	1.24	1.24	1.24	1.24	1.24	1.24	1.24	1.24	1.24	1.24	1.24
NRC Pacakge Conversion Factor	1.09	1.09	1.09	1.09	1.09	1.09	1.09	1.09	1.09	1.09	1.09
DMSI Conversion Factor RC package	2.829448	2.695654	2.551433	2.399027	2.241074	2.080505	1.920192	1.762823	1.610624	1.465424	1.328503
DMSI Conversion Factor NRC package	2.487176	2.369567	2.242792	2.108822	1.969976	1.828831	1.687911	1.549578	1.415791	1.288155	1.167797

NEW

32 GT/s Back Channel Equalization

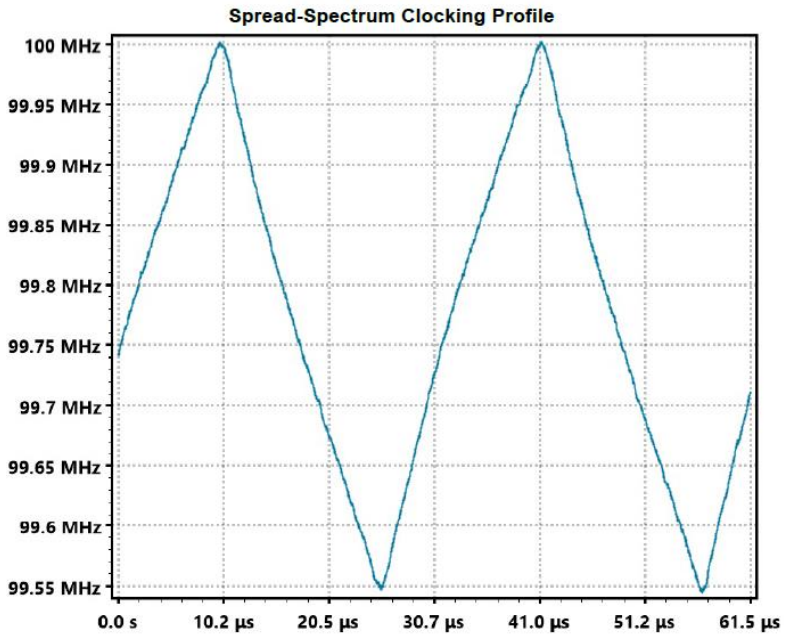
- Rx calibration calls for 34 to 37 dB @ 16GHz
- 5.0 Add-in Card budget = 9.5dB
- 5.0 Systems
  - 27.5dB including mated CEM connector
  - Fixtures/Cables could add another 4dB
- Add-in Card Rx LEQ – Error Detector EQ sufficient
- System Rx LEQ – Some require external EQ expected
  - Active Redriver should be considered
  - Expected across the industry
- Redrivers
  - Non Linear devices allowed
  - Avoid introducing bit errors in back channel only
  - Performs similar to CTLE with additional gain stages
- Experimentation expected at early FYI workshops



Backchannel (location for redriver)

Receiver Testing with SSC at 32 GT/s

Spread Spectrum Clocking (SSC) is utilized to spread the radiated electromagnetic energy across a wider frequency band and minimize the potential interference with other electronic devices.



PCI Express 5.0 SSC Parameters	
SSC Frequency Range	30 to 33 KHz
SSC Deviation	-0.5 to 0.0 % UI
SSC Deviation (SRIS)	-0.3 to 0.0 % UI
SSC Slew Rate	1250 ppm / us

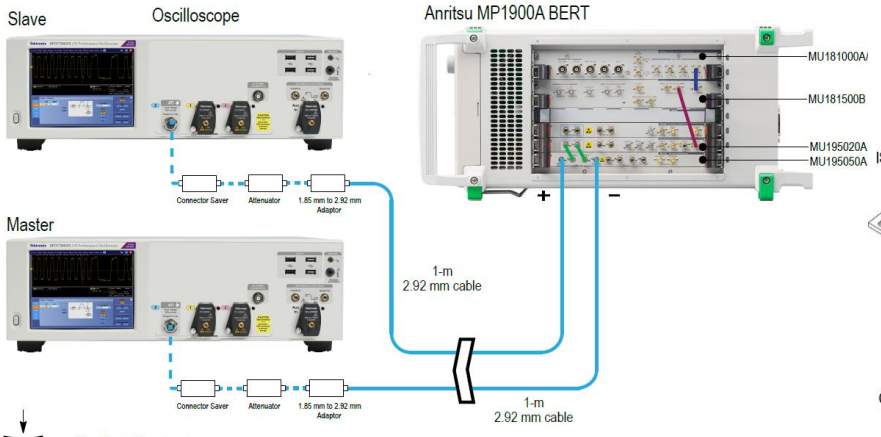
- Base Rx performs JTOL including a SSC tone
- Add-in Cards historically have not tested with SSC
- Systems testing at 16 GT/s – CTS did not define
  - In practice many were tested with SSC enabled
- Expect more clarity in 32 GT/s CTS
- Anritsu/Tek solution supports testing with/without SSC!!!

Anritsu & Tektronix PCIe Solutions

Tektronix Solution Configuration

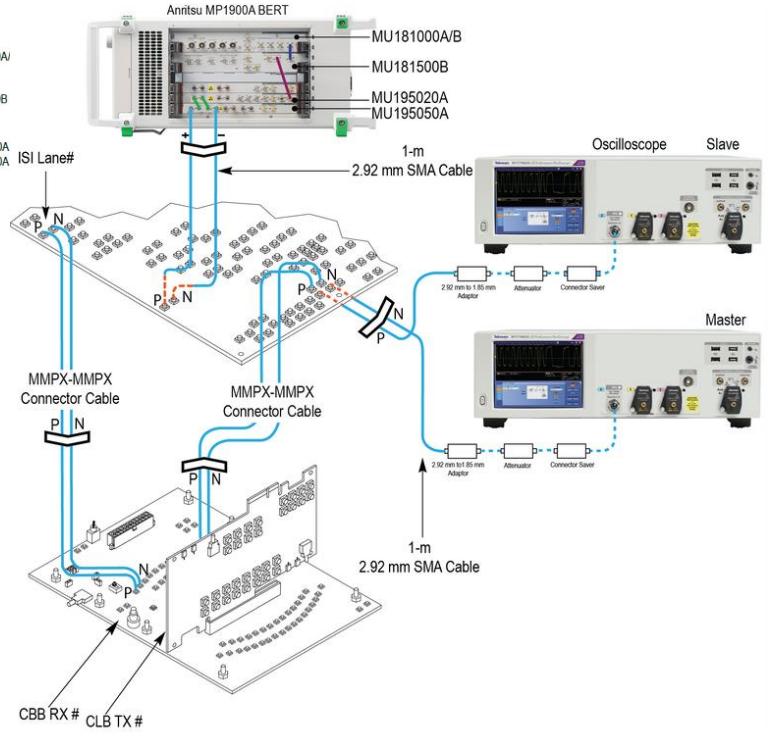
TEST SYSTEM VIEW GEN5 CEM CALIBRATION

TP1 Calibration

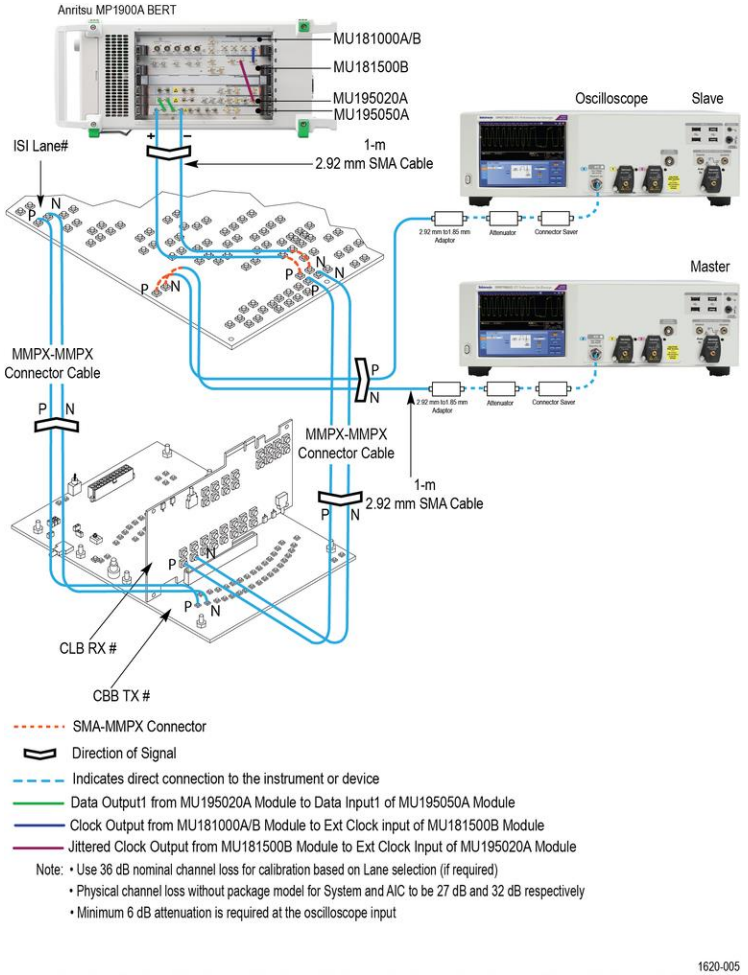


Tektronix Receiver Solution

TP2 AIC Calibration



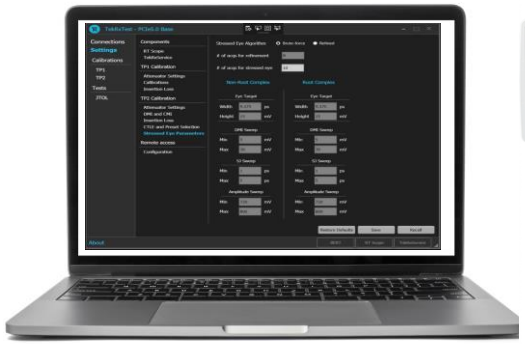
TP2 SYS Calibration



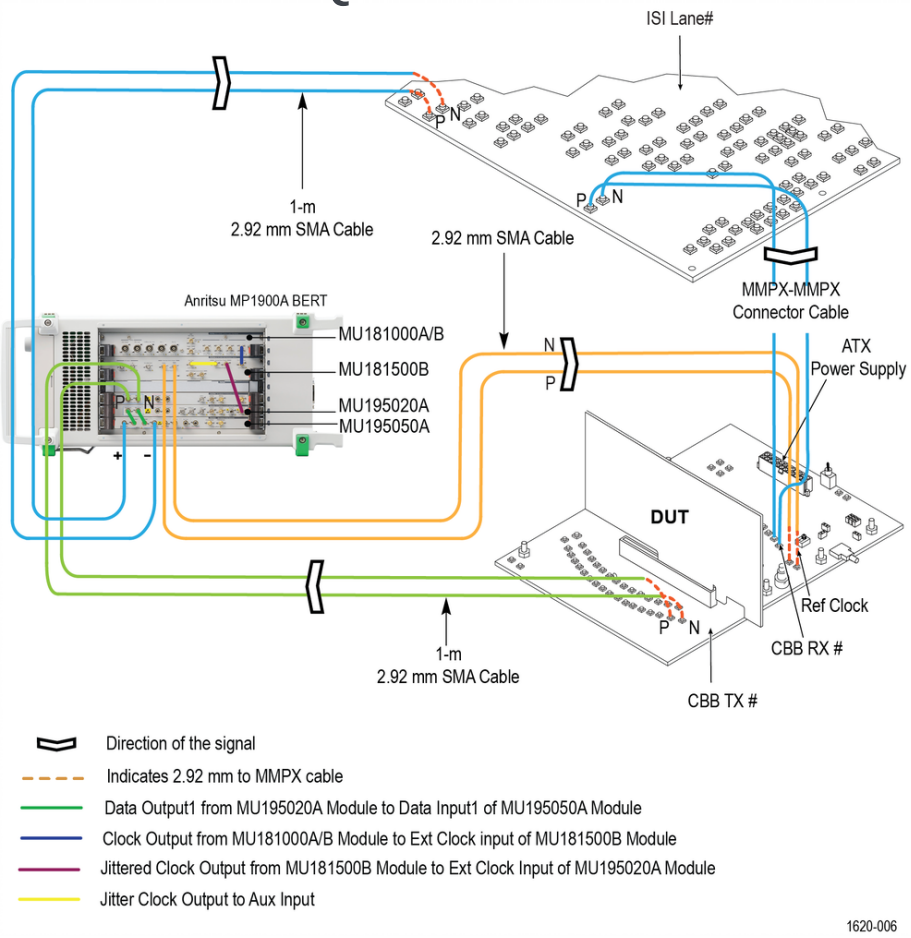
Tektronix Solution Configuration

TEST SYSTEM VIEW GEN5 CEM TEST

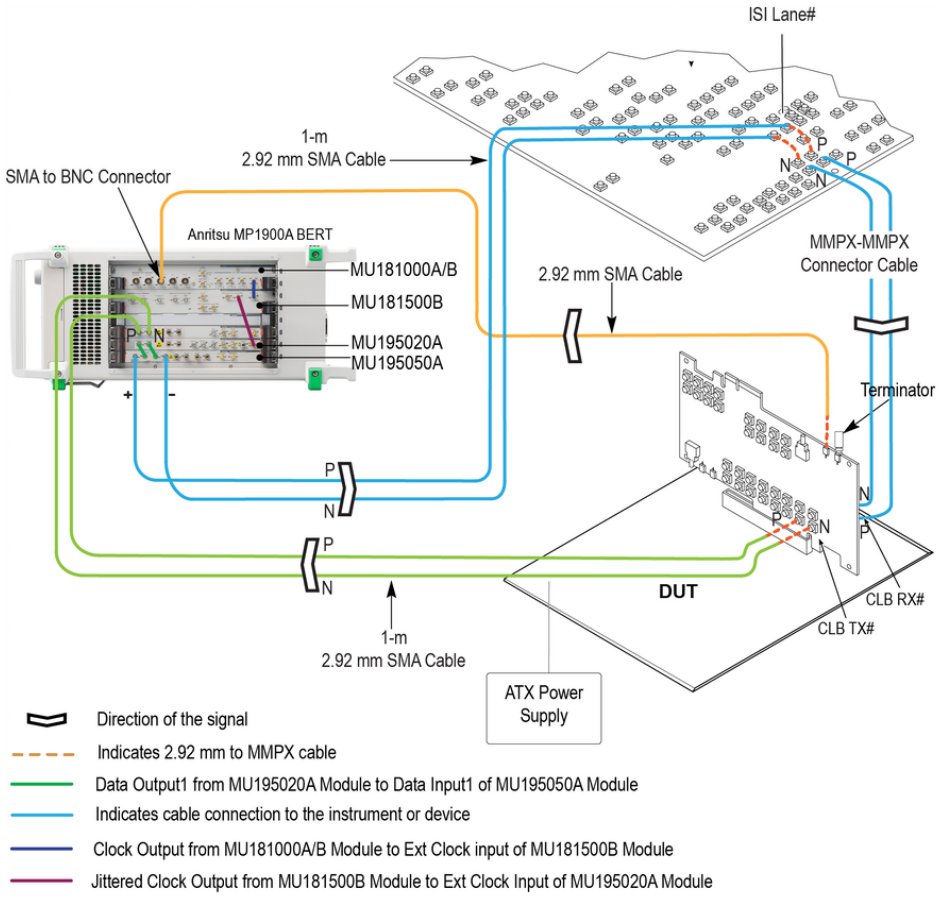
Tektronix
Receiver Solution



RX LEQ AIC Tests



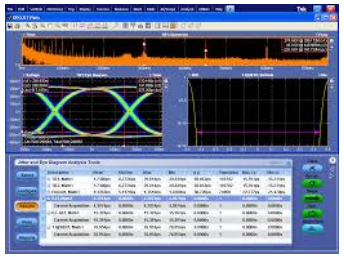
RX LEQ SYS Tests



PCIe Gen5 Solution Landscape

Debug

DPOJET Plugin for Debug



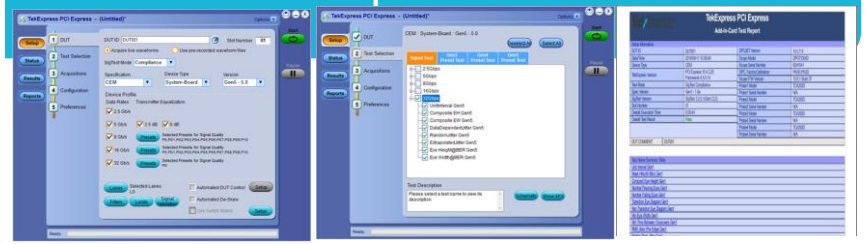
SDLA

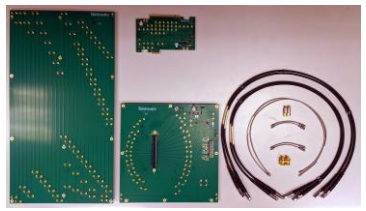
Transmitter

- Base
- CEM
- Ref CLK

SigTest Phoenix

TekExpress PCE5



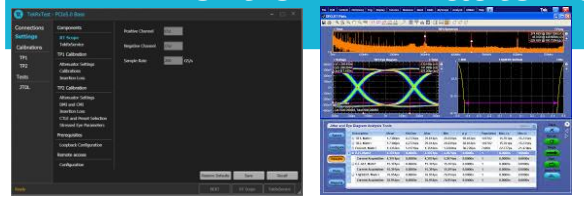


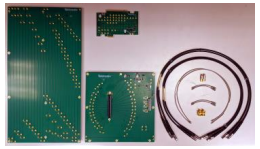
Receiver

BASE	CEM
TP1-TP2	TP1-TP2
JTOL	JTOL
	Rx/Tx LEQ

SigTest

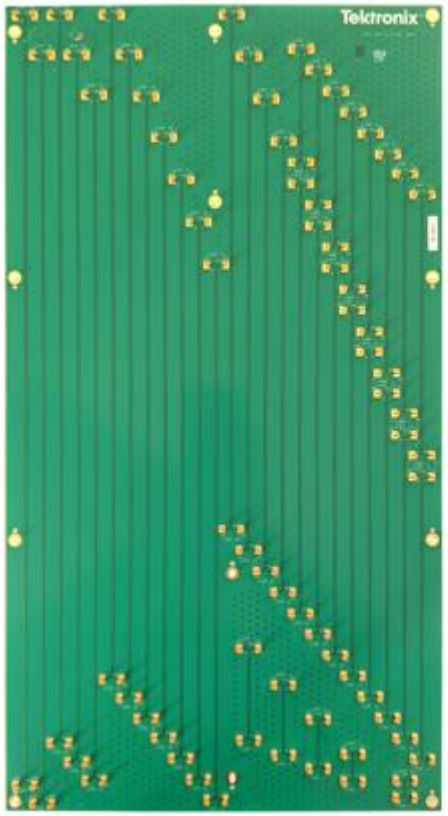
Tektronix Rx automation

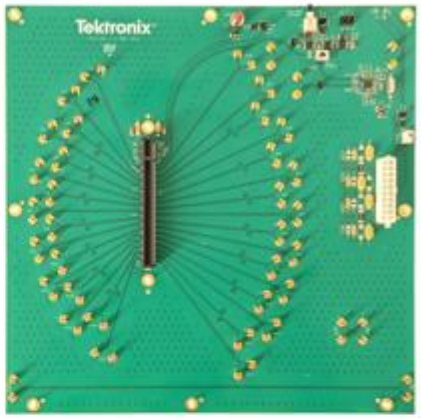


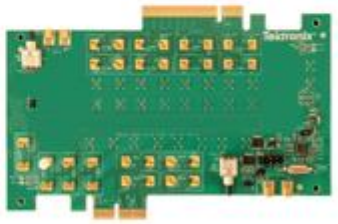


FUTURE PROOF FOR GEN6 – Tektronix is involved in PCI-SIG pathfinding!!!

Tektronix PCIe Gen5 Pre-Compliance Fixtures







- Gen5 CEM SIG fixtures delayed
- Tektronix fixtures available today
- X1 Kit
  - CBB, CLB x1/x16 & ISI
- X16 Kit
  - CBB, CLB x1/x16 & x4/x8, ISI
- Includes MMPX adaptors & cables
- Expect similar performance to SIG fixtures
  - Stressed eye calibration
  - Rx/Tx LEQ Testing
  - Tx Signal Quality & Tx Preset
  - Add-in Card PLL BW

RX LEQ Test and Jitter Tolerance Test

RX LEQ Test Procedure

Steps of Receiver Testing

Step1: Calibration

- Channel Loss by VNA
- Eye Amplitude, Preset, SJ and RJ by BERT and RTO
- DM-I and Eye Height/Eye Width by BERT and RTO

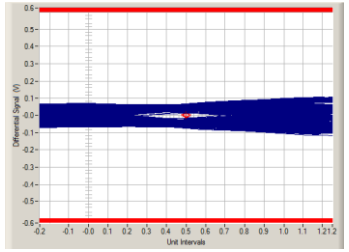
Step2: Link Training

DUT needs to be looped back under the compliance stress condition

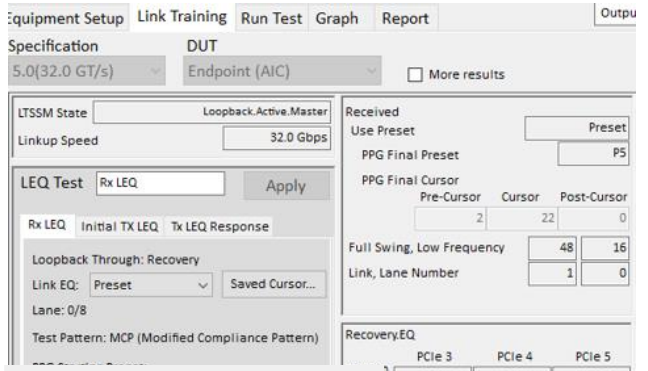
- Loopback Active Master
- Troubleshooting

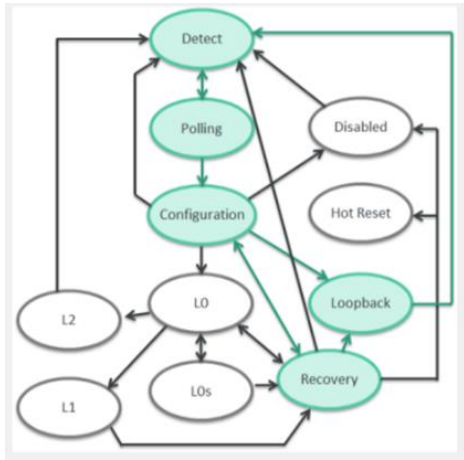
Step3: Measurement

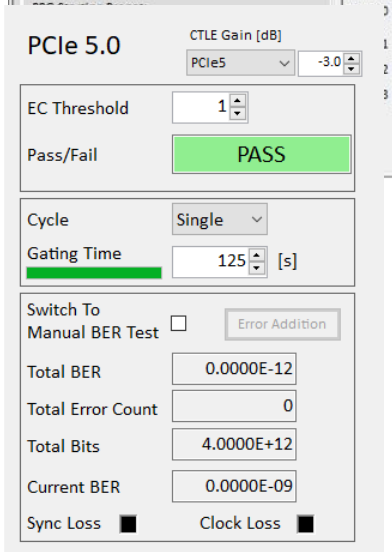
- Checking BER <1E(-12) for 125 seconds (95% confidence level)
- Jitter Tolerance Testing (Optional)

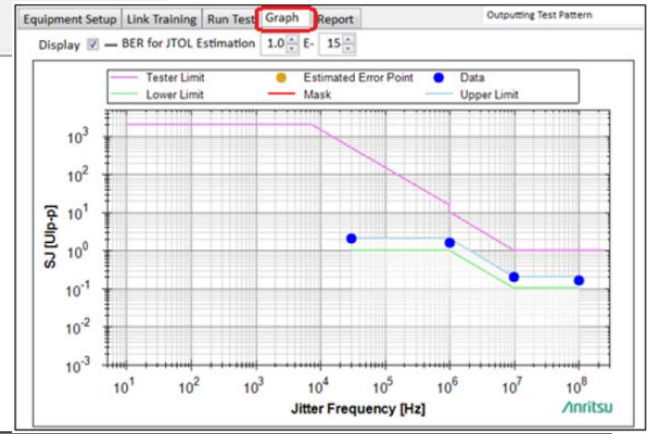


	Min	Max
EH	13.5 mV	16.5 mV
EW	9.13 ps	9.62 ps



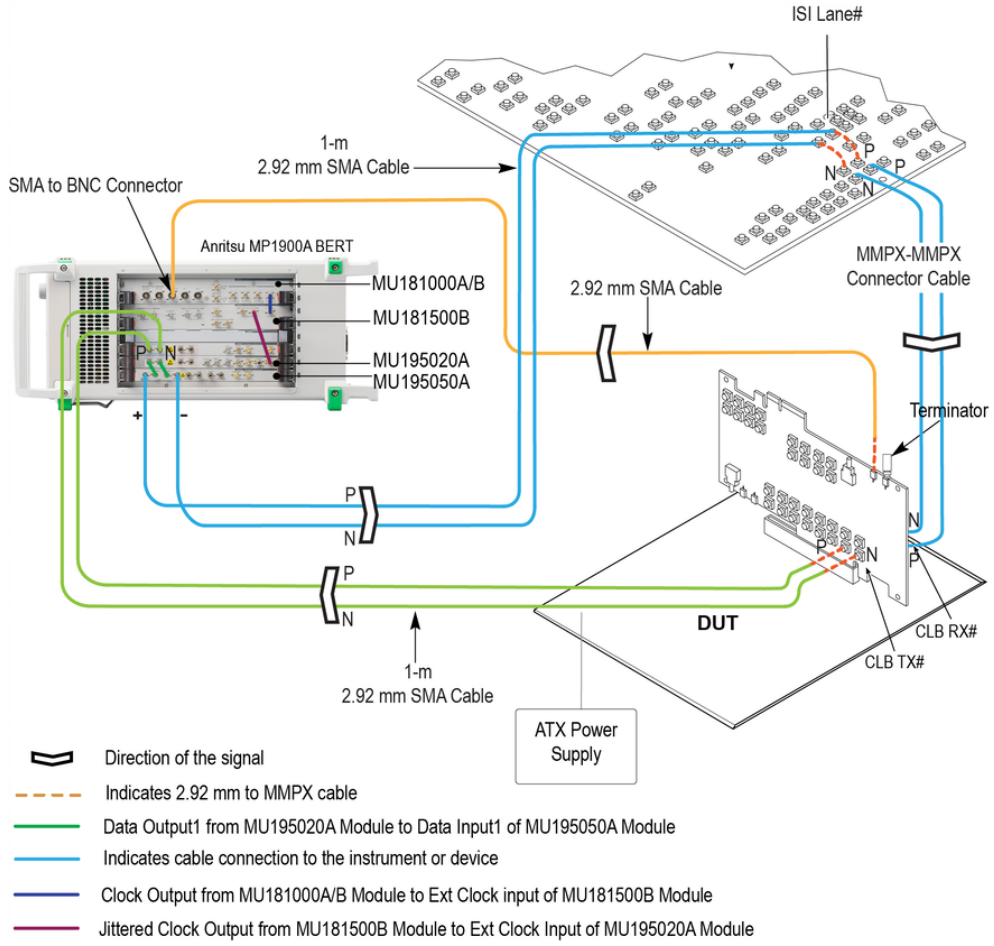






First and Most Critical Step for Stable and Repeatable RX Test

- Object of RX LEQ Test: Successful Link Equalization Training under the specific stressed eye condition
  - ✓ Optimize the equalizer (Preset and CTLE)
  - ✓ Go to Loopback Status (Loopback Active Master)
  - ✓ BER 1E(-12)
- **Establish the return path:**
  - ✓ Minimize loss and ISI of the return path
  - ✓ Optimize the equalization between DUT TX Preset and CTLE of the error detector
  - ✓ Error Free on the return path (DUT TX to the Error Detector) to isolate the error source
  - ✓ System may need Re-Driver when the Actual physical loss of the return path is more than 18 dB (18 to 26.5 dB)

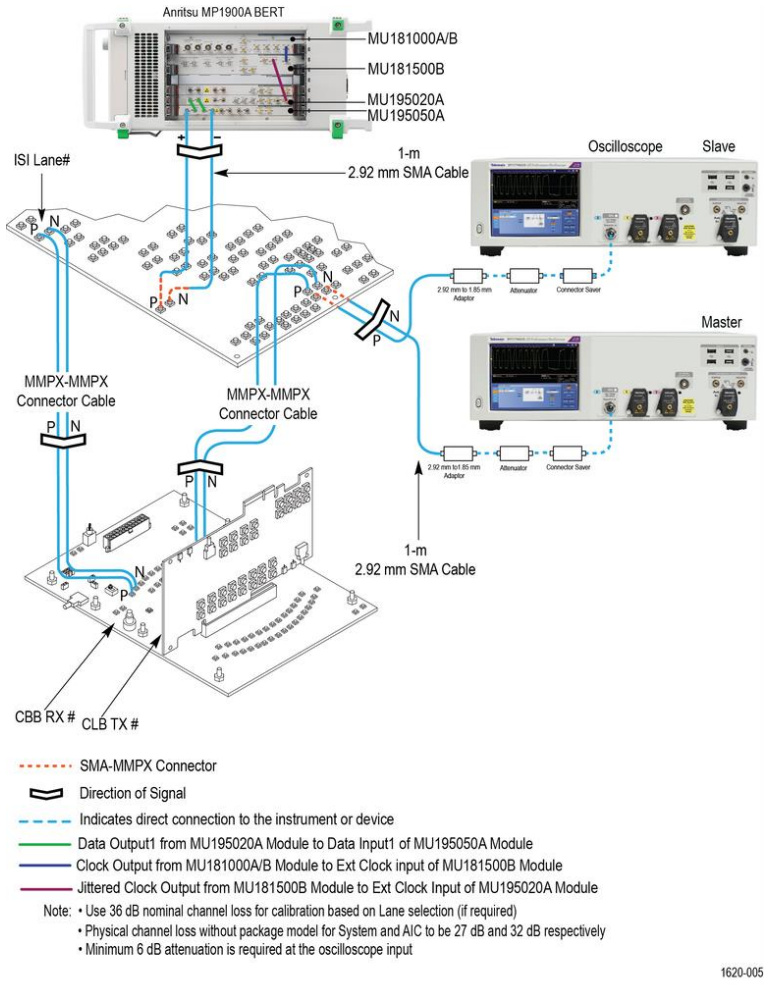


PCI Express Gen5 RX LEQ Calibration Points

Stress Signal Calibration → Transition to Loopback Status → Stress Signal Input Test

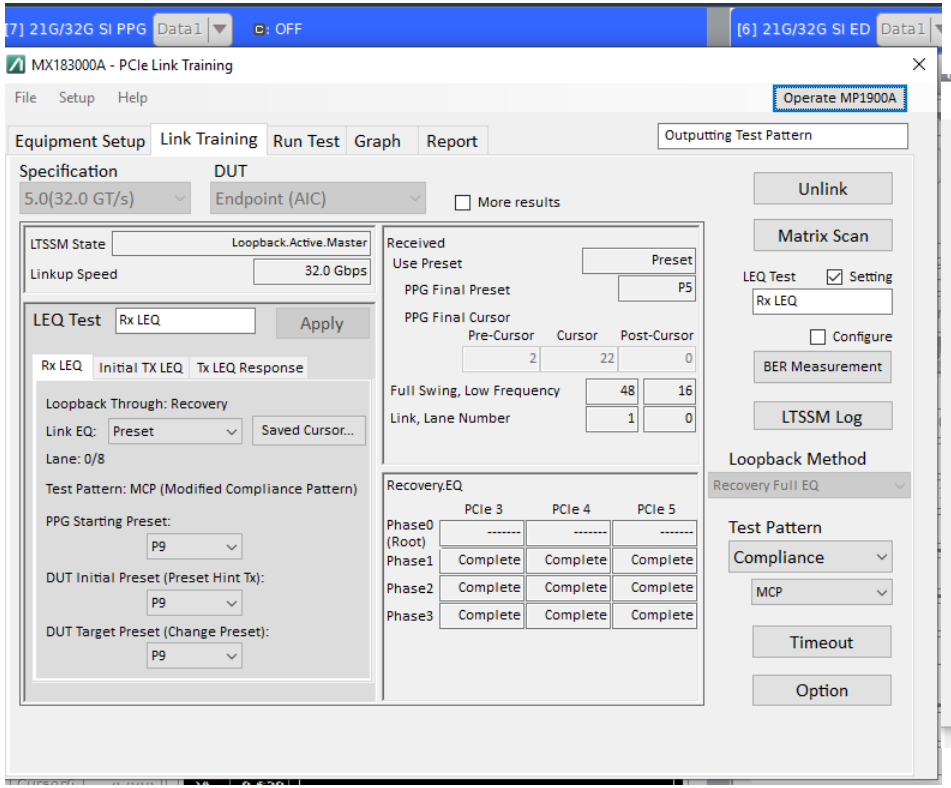
Table 8-9 Stressed Jitter Eye Parameters

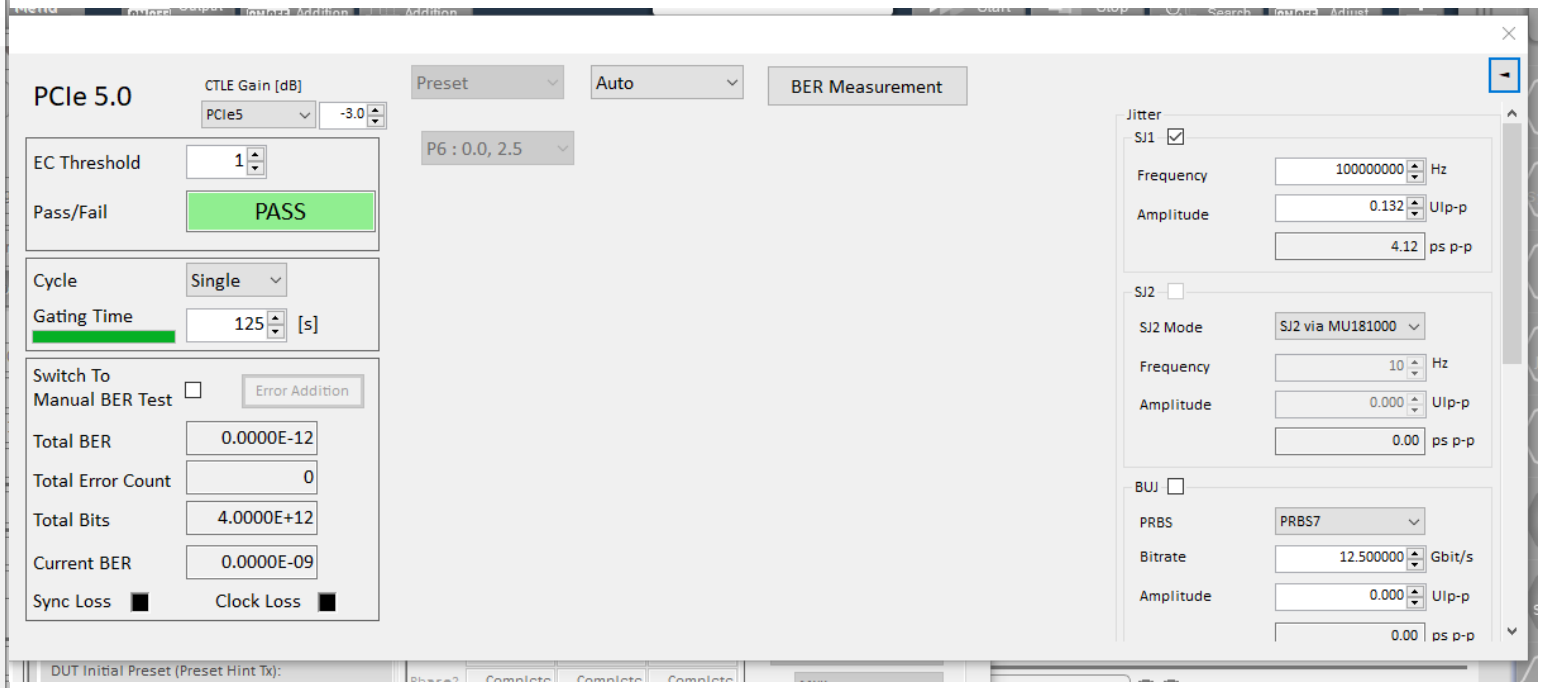
Symbol	Parameter	2.5 GT/s	5.0 GT/s	8.0 GT/s	16.0 GT/s	32.0 GT/s	Units	Details
$V_{RX-LAUNCH}$	Generator launch voltage	800 to 1200	800 to 1200	800 to 1200	720 to 800	720 to 800	mV PP	Note 1
T_{RX-UI}	Unit Interval	400	200	125	62.5	31.25	ps	
T_{RX-ST}	Eye width	≤ 0.4	≤ 0.32	≤ 0.30	≤ 0.30	≤ 0.30	UI	Note 3, 4, 8, 10
V_{RX-ST}	Eye height	≤ 175	≤ 100	≤ 25	≤ 15	≤ 15	mV PP	Note 2, 4, 8, 9
$T_{RX-ST-SJ}$	Swept Sj	N/A	75 ps (max) See Note 11	See Section 8.4.2.2.1	See Section 8.4.2.2.1	See Section 8.4.2.2.1	ps	Note 5
$T_{RX-ST-RJ}$	Random Jitter	N/A	3.4	(max) 3.0	1.0	0.5	ps RMS	Note 6, 7
$V_{RX-DIFF-INT}$	Differential noise	N/A	N/A	14	14	10	mV PP	Note 7, 12 Adjust to set EH. Frequency = 2.1 GHz .
$V_{RX-CM-INT}$	Common mode noise	150	150	150	150	150	mV PP	Note 8



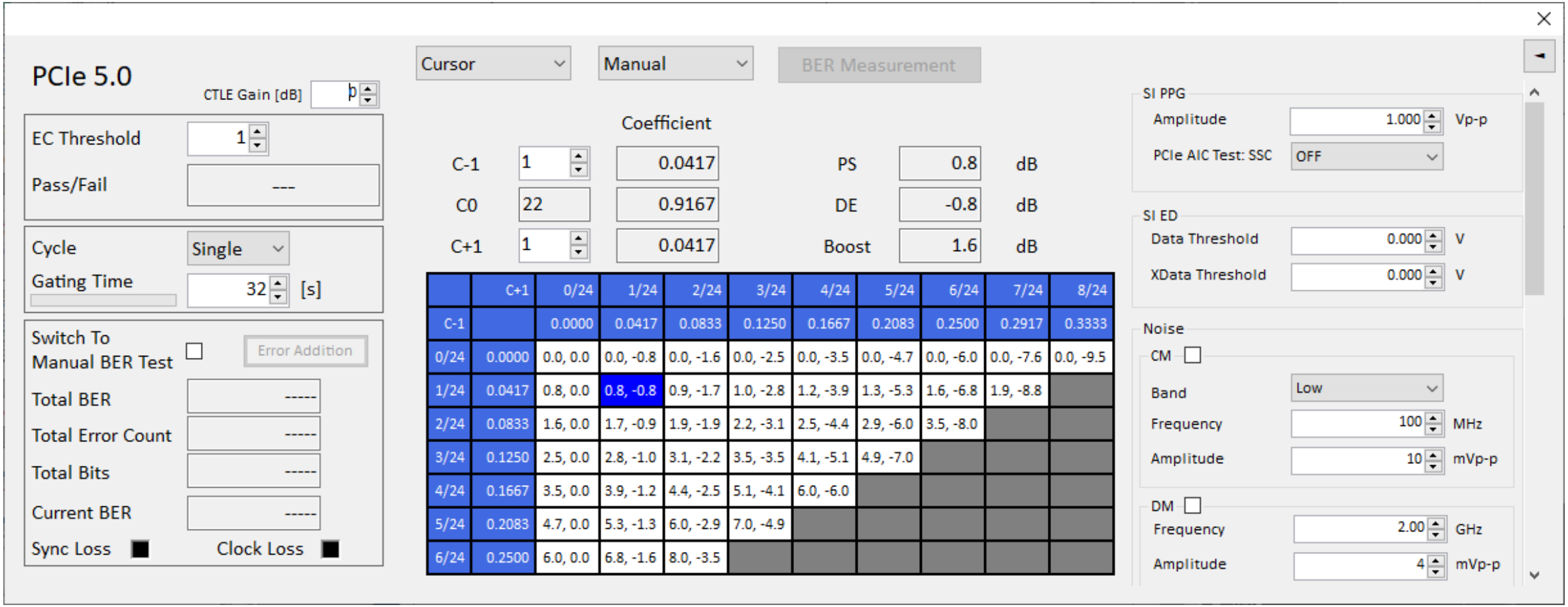
PCI Express Gen5 Link Training

Stress Signal Calibration → Transition to Loopback Status → Stress Signal Input Test



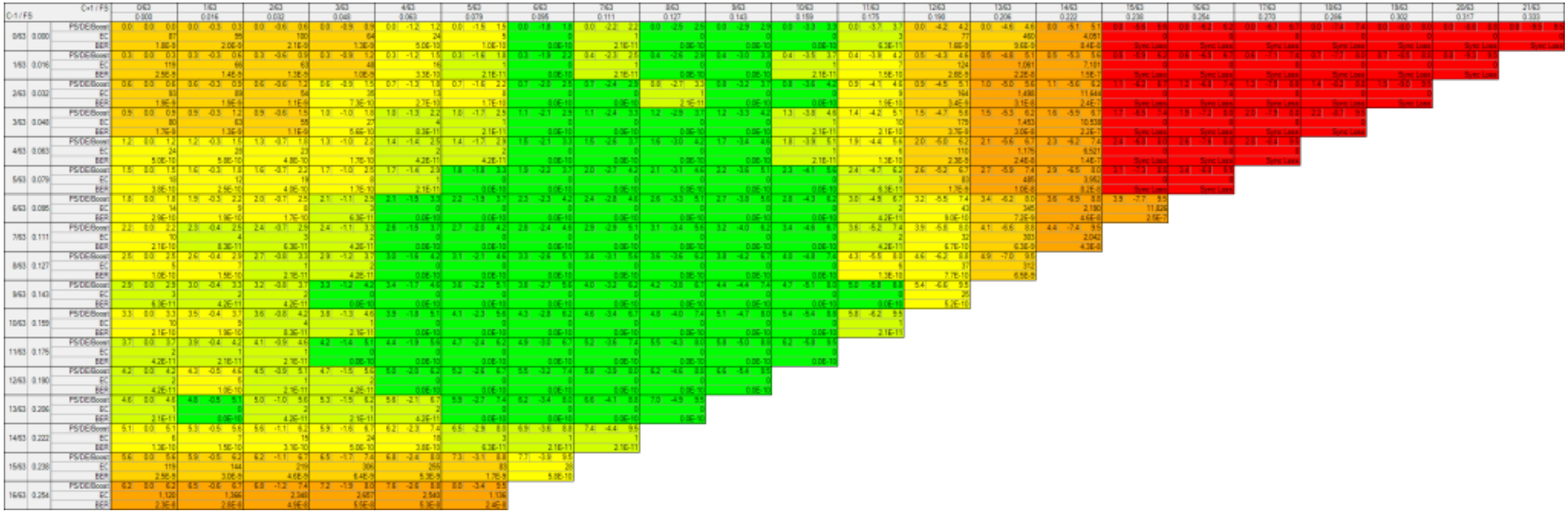


Troubleshooting by Manual Preset/Cursor Setting



	C+1	0/24	1/24	2/24	3/24	4/24	5/24	6/24	7/24	8/24
C-1		0.0000	0.0417	0.0833	0.1250	0.1667	0.2083	0.2500	0.2917	0.3333
0/24	0.0000	0.0, 0.0	0.0, -0.8	0.0, -1.6	0.0, -2.5	0.0, -3.5	0.0, -4.7	0.0, -6.0	0.0, -7.6	0.0, -9.5
1/24	0.0417	0.8, 0.0	0.8, -0.8	0.9, -1.7	1.0, -2.8	1.2, -3.9	1.3, -5.3	1.6, -6.8	1.9, -8.8	
2/24	0.0833	1.6, 0.0	1.7, -0.9	1.9, -1.9	2.2, -3.1	2.5, -4.4	2.9, -6.0	3.5, -8.0		
3/24	0.1250	2.5, 0.0	2.8, -1.0	3.1, -2.2	3.5, -3.5	4.1, -5.1	4.9, -7.0			
4/24	0.1667	3.5, 0.0	3.9, -1.2	4.4, -2.5	5.1, -4.1	6.0, -6.0				
5/24	0.2083	4.7, 0.0	5.3, -1.3	6.0, -2.9	7.0, -4.9					
6/24	0.2500	6.0, 0.0	6.8, -1.6	8.0, -3.5						

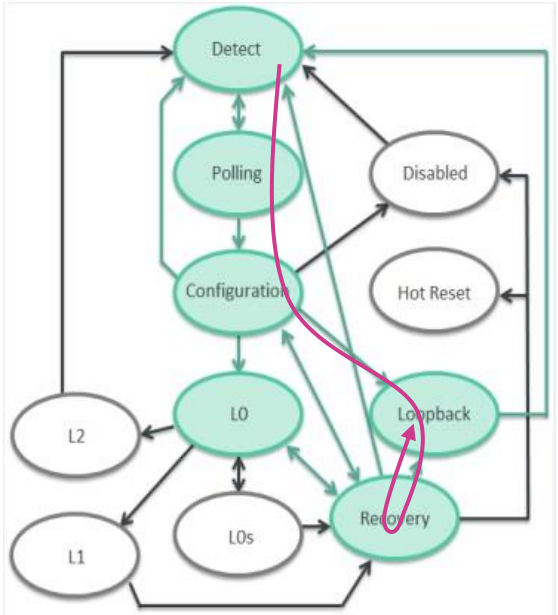
Auto Cursor Matrix Scan



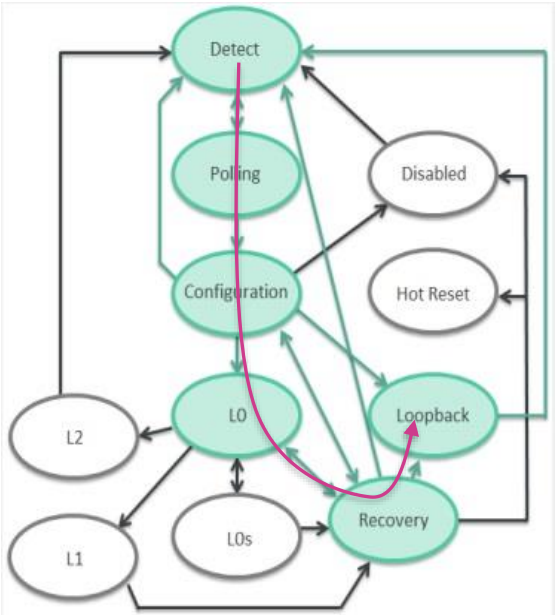
PCI Express Gen5 Link Training

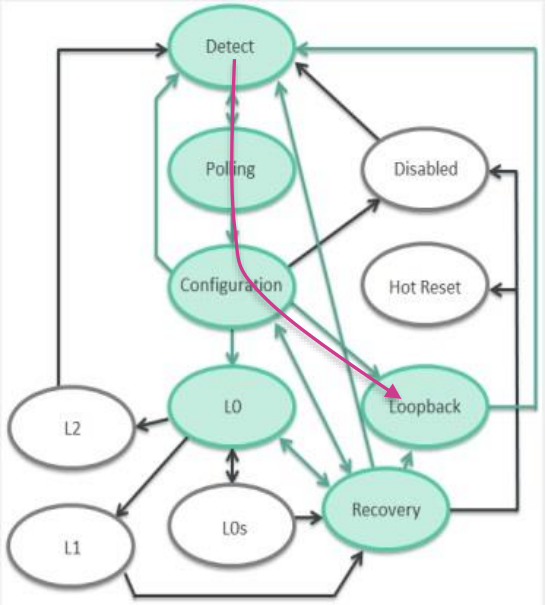
Stress Signal Calibration → Transition to Loopback Status → Stress Signal Input Test

New for 32 GT/s



8, 16, and 32 GT/s (Legacy)





PCI Express Gen5 Link Training

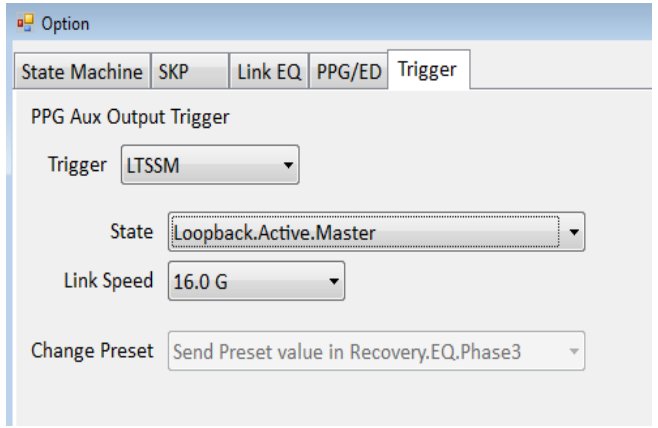
Stress Signal Calibration → Transition to Loopback Status → Stress Signal Input Test

LTSSM Log Viewer

Training Log Viewer

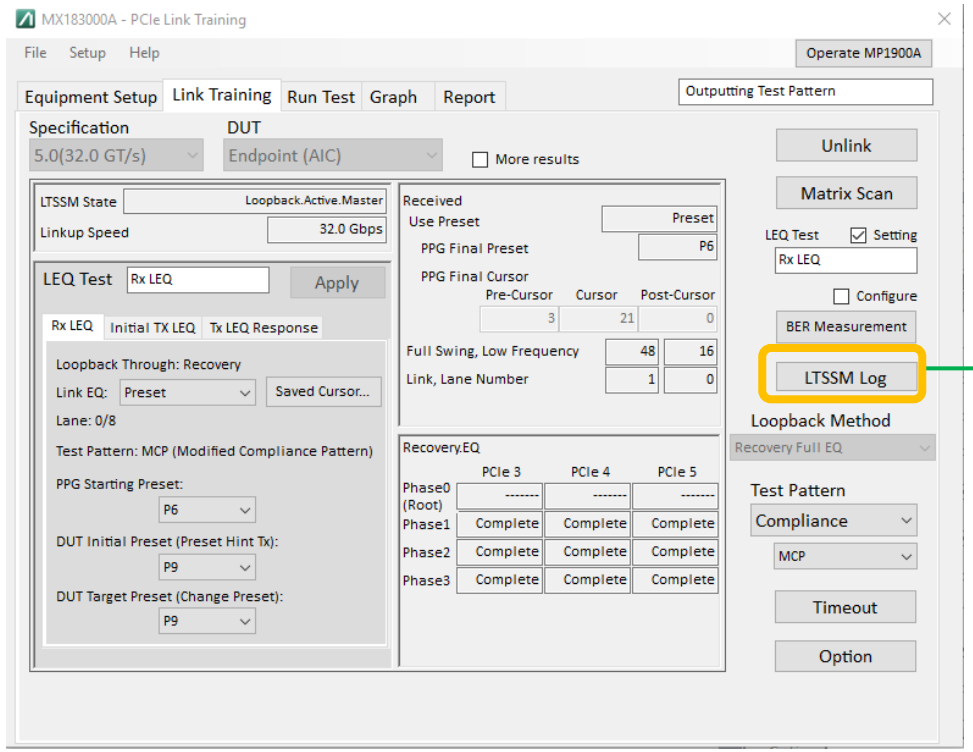
Time [ns]	Δ Time [ns]	State	Speed[GT/s]	Detect Preset	Error Count	Use Preset	Preset	Pre-cursor	Cursor	Post-cursor	FS	LF
440,750,376	4	RECOVERY_RCVR_LOCK	16.0	---	---	---	---	---	---	---	---	---
440,750,380	1,153,864	RECOVERY_EQUALIZATION_PHASE0	16.0	---	---	---	---	---	---	---	24	8
441,904,244	8	RECOVERY_EQUALIZATION_PHASE0	16.0	---	---	---	---	---	---	---	24	8
441,904,252	2,848	RECOVERY_EQUALIZATION_PHASE1	16.0	---	---	---	---	---	---	---	---	---
441,907,100	272	RECOVERY_EQUALIZATION_PHASE2	16.0	0 (MP1900A => DUT)	0	1 (Preset)	P6	3	21	0	---	---
441,907,372	1,999,728	RECOVERY_EQUALIZATION_PHASE2	16.0	1 (MP1900A <= DUT)	0	1 (Preset)	P6	3	21	0	---	---
443,907,100	2,864	RECOVERY_EQUALIZATION_PHASE2	16.0	0 (MP1900A => DUT)	0	1 (Preset)	P4	0	24	0	---	---
443,909,964	2,000,000	RECOVERY_EQUALIZATION_PHASE2	16.0	1 (MP1900A <= DUT)	0	1 (Preset)	P4	0	24	0	---	---
445,909,964	2,860	RECOVERY_EQUALIZATION_PHASE3	16.0	0 (MP1900A => DUT)	0	1 (Preset)	P5	2	22	0	---	---
445,912,824	4	RECOVERY_EQUALIZATION_PHASE3	16.0	1 (MP1900A <= DUT)	0	1 (Preset)	P5	2	22	0	---	---
445,912,828	1,999,980	RECOVERY_EQUALIZATION_PHASE3	16.0	0 (MP1900A => DUT)	0	1 (Preset)	P5	2	22	0	---	---
447,912,808	4	RECOVERY_EQUALIZATION_PHASE3	16.0	1 (MP1900A <= DUT)	0	1 (Preset)	P4	0	24	0	---	---
447,912,812	2,002,840	RECOVERY_EQUALIZATION_PHASE3	16.0	0 (MP1900A => DUT)	0	1 (Preset)	P4	0	24	0	---	---
449,915,652	64	RECOVERY_RCVR_LOCK	16.0	---	---	---	---	---	---	---	---	---
449,915,716	2,980	RECOVERY_RCVR_CFG_TS2	16.0	---	---	---	---	---	---	---	---	---
449,918,696	508	RECOVERY_IDLE	16.0	---	---	---	---	---	---	---	---	---
449,919,204	12	L0	16.0	---	---	---	---	---	---	---	---	---
449,919,216	2,420	RECOVERY_RCVR_LOCK	16.0	---	---	---	---	---	---	---	---	---
449,921,636	6,553,832	RECOVERY_RCVR_CFG_EQTS2	16.0	---	---	---	---	---	---	---	---	---
456,475,468	100,016	RECOVERY_SPEED	16.0	---	---	---	---	---	---	---	---	---
456,575,484	32	RECOVERY_SPEED	32.0	---	---	---	---	---	---	---	---	---
456,575,516	4	RECOVERY_RCVR_LOCK	32.0	---	---	---	---	---	---	---	---	---
456,575,520	1,213,648	RECOVERY_EQUALIZATION_PHASE0	32.0	---	---	---	---	---	---	---	24	8
457,789,168	8	RECOVERY_EQUALIZATION_PHASE0	32.0	---	---	---	---	---	---	---	24	8
457,789,176	1,892	RECOVERY_EQUALIZATION_PHASE1	32.0	---	---	---	---	---	---	---	---	---
457,791,068	264	RECOVERY_EQUALIZATION_PHASE2	32.0	0 (MP1900A => DUT)	0	1 (Preset)	P6	3	21	0	---	---
457,791,332	1,999,736	RECOVERY_EQUALIZATION_PHASE2	32.0	1 (MP1900A <= DUT)	0	1 (Preset)	P6	3	21	0	---	---
459,791,068	1,912	RECOVERY_EQUALIZATION_PHASE2	32.0	0 (MP1900A => DUT)	0	1 (Preset)	P4	0	24	0	---	---
459,792,980	2,000,000	RECOVERY_EQUALIZATION_PHASE2	32.0	1 (MP1900A <= DUT)	0	1 (Preset)	P4	0	24	0	---	---
461,792,980	1,912	RECOVERY_EQUALIZATION_PHASE3	32.0	0 (MP1900A => DUT)	0	1 (Preset)	P5	2	22	0	---	---
461,794,892	4	RECOVERY_EQUALIZATION_PHASE3	32.0	1 (MP1900A <= DUT)	0	1 (Preset)	P5	2	22	0	---	---
461,794,896	2,000,004	RECOVERY_EQUALIZATION_PHASE3	32.0	0 (MP1900A => DUT)	0	1 (Preset)	P5	0	24	0	---	---
463,794,900	4	RECOVERY_EQUALIZATION_PHASE3	32.0	1 (MP1900A <= DUT)	0	1 (Preset)	P4	0	24	0	---	---
463,794,904	2,001,908	RECOVERY_EQUALIZATION_PHASE3	32.0	0 (MP1900A => DUT)	0	1 (Preset)	P4	0	24	0	---	---
465,796,812	32	RECOVERY_RCVR_LOCK	32.0	---	---	---	---	---	---	---	---	---
465,796,844	1,948	RECOVERY_RCVR_CFG_TS2	32.0	---	---	---	---	---	---	---	---	---
465,798,792	524	LOOPBACK_ENTRY_MASTER_TS1	32.0	---	---	---	---	---	---	---	---	---
465,799,316	0	LOOPBACK_ACTIVE_MASTER	32.0	---	---	---	---	---	---	---	---	---

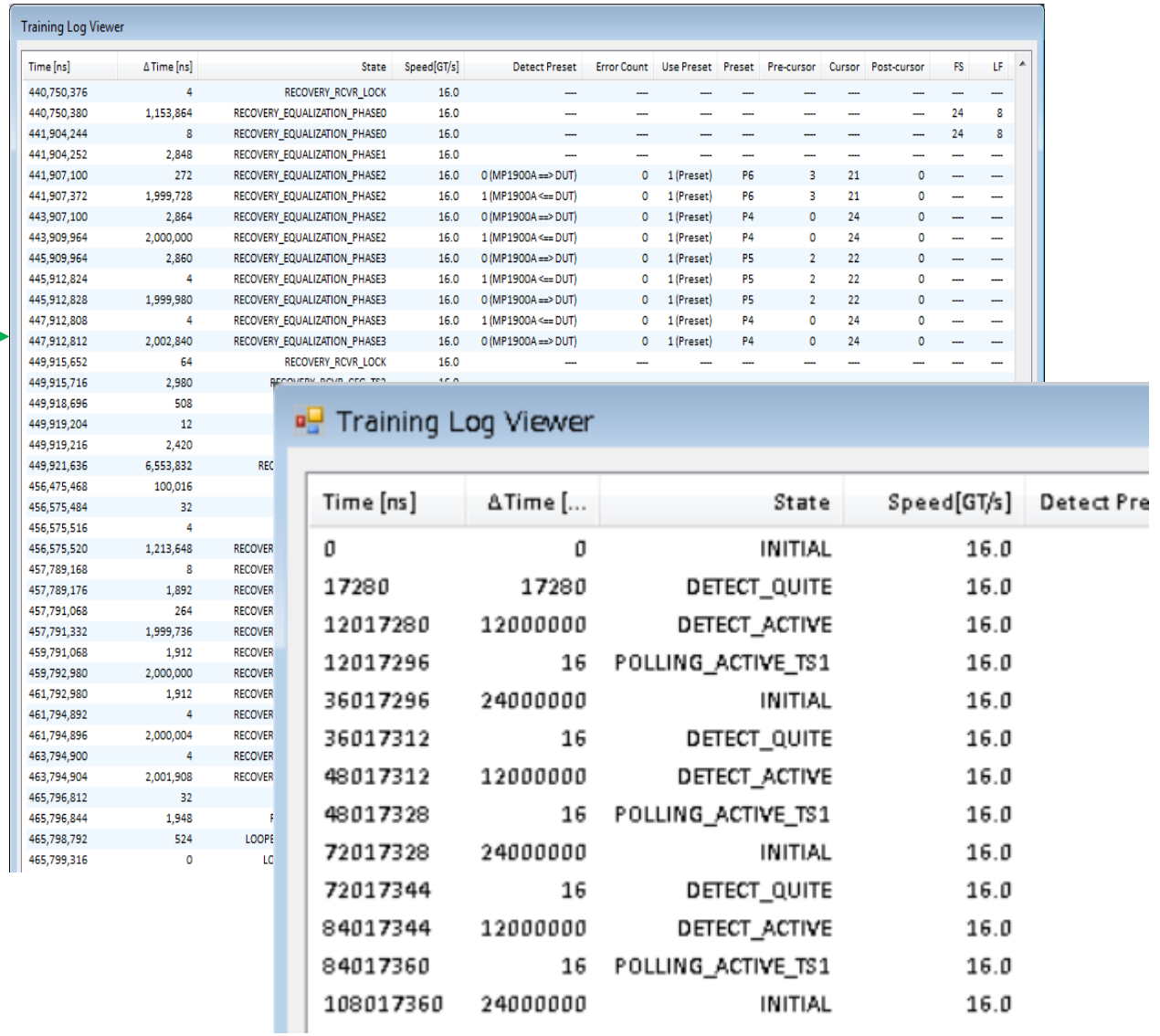
LTSSM Trigger



Capture problematic event

Debugging with BERT: Training Log Viewer





- The MP1900A Training Log Viewer function can display the actual Training State transition logs.
- The state transition path (route) and transition times can be analyzed in detail.

LTSSM Details

Training Log Viewer

Time [ns]	ΔTime [ns]	State	Speed[GT/s]	Detect Preset	Error Count	Use Preset	Preset	Pre-cursor	Cursor	Post-cursor	FS	LF
440,750,376	4	RECOVERY_RCVR_LOCK	16.0	---	---	---	---	---	---	---	---	---
440,750,380	1,153,864	RECOVERY_EQUALIZATION_PHASE0	16.0	---	---	---	---	---	---	---	24	8
441,904,244	8	RECOVERY_EQUALIZATION_PHASE0	16.0	---	---	---	---	---	---	---	24	8
441,904,252	2,848	RECOVERY_EQUALIZATION_PHASE1	16.0	---	---	---	---	---	---	---	---	---
441,907,100	272	RECOVERY_EQUALIZATION_PHASE2	16.0	0 (MP1900A ==> DUT)	0	1 (Preset)	P6	3	21	0	---	---
441,907,372	1,999,728	RECOVERY_EQUALIZATION_PHASE2	16.0	1 (MP1900A <== DUT)	0	1 (Preset)	P6	3	21	0	---	---
443,907,100	2,864	RECOVERY_EQUALIZATION_PHASE2	16.0	0 (MP1900A ==> DUT)	0	1 (Preset)	P4	0	24	0	---	---
443,909,964	2,000,000	RECOVERY_EQUALIZATION_PHASE2	16.0	1 (MP1900A <== DUT)	0	1 (Preset)	P4	0	24	0	---	---
445,909,964	2,860	RECOVERY_EQUALIZATION_PHASE3	16.0	0 (MP1900A ==> DUT)	0	1 (Preset)	P5	2	22	0	---	---
445,912,824	4	RECOVERY_EQUALIZATION_PHASE3	16.0	1 (MP1900A <== DUT)	0	1 (Preset)	P5	2	22	0	---	---
445,912,828	1,999,980	RECOVERY_EQUALIZATION_PHASE3	16.0	0 (MP1900A ==> DUT)	0	1 (Preset)	P5	2	22	0	---	---
447,912,808	4	RECOVERY_EQUALIZATION_PHASE3	16.0	1 (MP1900A <== DUT)	0	1 (Preset)	P4	0	24	0	---	---
447,912,812	2,002,840	RECOVERY_EQUALIZATION_PHASE3	16.0	0 (MP1900A ==> DUT)	0	1 (Preset)	P4	0	24	0	---	---
449,915,652	64	RECOVERY_RCVR_LOCK	16.0	---	---	---	---	---	---	---	---	---
449,915,716	2,980	RECOVERY_RCVR_CFG_TS2	16.0	---	---	---	---	---	---	---	---	---
449,918,696	508	RECOVERY_IDLE	16.0	---	---	---	---	---	---	---	---	---
449,919,204	12	L0	16.0	---	---	---	---	---	---	---	---	---
449,919,216	2,420	RECOVERY_RCVR_LOCK	16.0	---	---	---	---	---	---	---	---	---
449,921,636	6,553,832	RECOVERY_RCVR_CFG_EQTS2	16.0	---	---	---	---	---	---	---	---	---
456,475,468	100,016	RECOVERY_SPEED	16.0	---	---	---	---	---	---	---	---	---
456,575,484	32	RECOVERY_SPEED	32.0	---	---	---	---	---	---	---	---	---
456,575,516	4	RECOVERY_RCVR_LOCK	32.0	---	---	---	---	---	---	---	---	---
456,575,520	1,213,648	RECOVERY_EQUALIZATION_PHASE0	32.0	---	---	---	---	---	---	---	24	8
457,789,168	8	RECOVERY_EQUALIZATION_PHASE0	32.0	---	---	---	---	---	---	---	24	8
457,789,176	1,892	RECOVERY_EQUALIZATION_PHASE1	32.0	---	---	---	---	---	---	---	---	---
457,791,068	264	RECOVERY_EQUALIZATION_PHASE2	32.0	0 (MP1900A ==> DUT)	0	1 (Preset)	P6	3	21	0	---	---
457,791,332	1,999,736	RECOVERY_EQUALIZATION_PHASE2	32.0	1 (MP1900A <== DUT)	0	1 (Preset)	P6	3	21	0	---	---
459,791,068	1,912	RECOVERY_EQUALIZATION_PHASE2	32.0	0 (MP1900A ==> DUT)	0	1 (Preset)	P4	0	24	0	---	---
459,792,980	2,000,000	RECOVERY_EQUALIZATION_PHASE2	32.0	1 (MP1900A <== DUT)	0	1 (Preset)	P4	0	24	0	---	---
461,792,980	1,912	RECOVERY_EQUALIZATION_PHASE3	32.0	0 (MP1900A ==> DUT)	0	1 (Preset)	P5	2	22	0	---	---
461,794,892	4	RECOVERY_EQUALIZATION_PHASE3	32.0	1 (MP1900A <== DUT)	0	1 (Preset)	P5	2	22	0	---	---
461,794,896	2,000,004	RECOVERY_EQUALIZATION_PHASE3	32.0	0 (MP1900A ==> DUT)	0	1 (Preset)	P5	0	24	0	---	---
463,794,900	4	RECOVERY_EQUALIZATION_PHASE3	32.0	1 (MP1900A <== DUT)	0	1 (Preset)	P4	0	24	0	---	---
463,794,904	2,001,908	RECOVERY_EQUALIZATION_PHASE3	32.0	0 (MP1900A ==> DUT)	0	1 (Preset)	P4	0	24	0	---	---
465,796,812	32	RECOVERY_RCVR_LOCK	32.0	---	---	---	---	---	---	---	---	---
465,796,844	1,948	RECOVERY_RCVR_CFG_TS2	32.0	---	---	---	---	---	---	---	---	---
465,798,792	524	LOOPBACK_ENTRY_MASTER_TS1	32.0	---	---	---	---	---	---	---	---	---
465,799,316	0	LOOPBACK_ACTIVE_MASTER	32.0	---	---	---	---	---	---	---	---	---

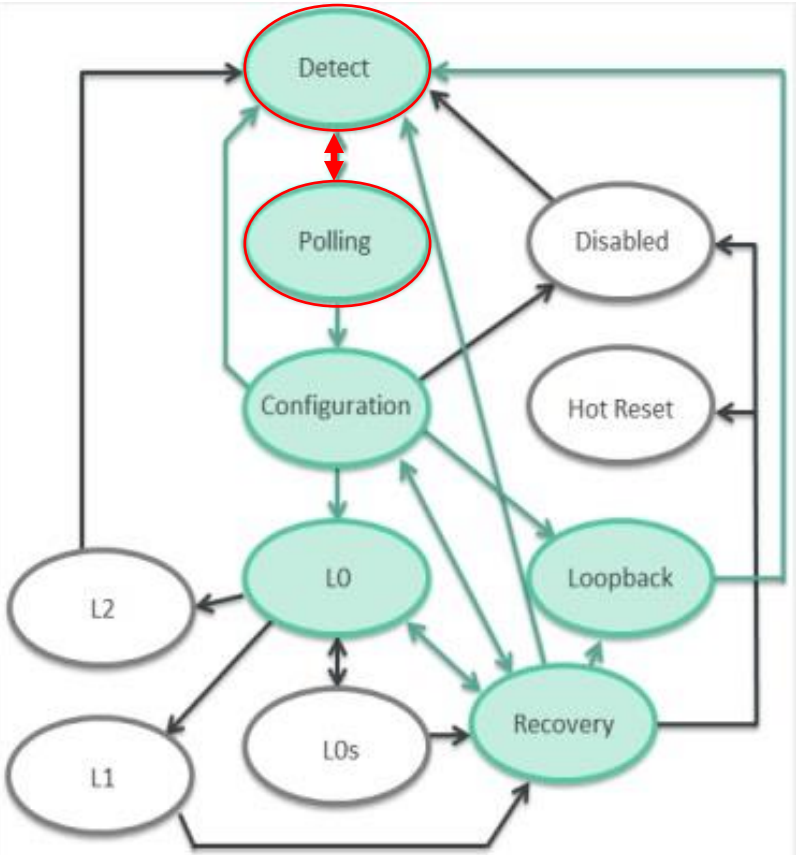
Troubleshoot: 2.5GT/s Link Failure

90% of this case, No signal or no reference clock.
Check the cable connection and polarity

- LTSSM times-out at Polling Active and repeatedly performs the operation for returning to Detect.

- Gen1 2.5 GT/s Symbol Lock is not obtained.

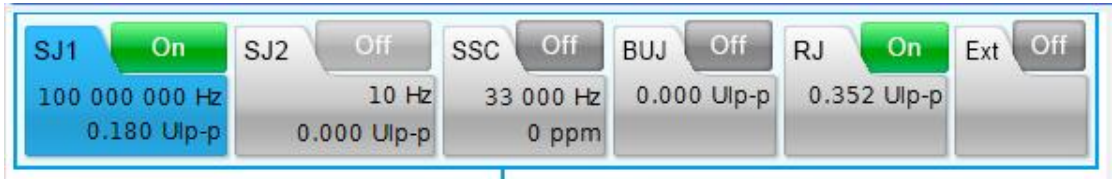
Time[ns]	Delta Time[ns]	State	Speed[GT/s]	Detect Preset	Error Count	Use Preset	Preset	Pre-cursor	Cursor	Post-cursor
0	13552	INITIAL	8	----	----	----	----	----	----	----
13552	8738088	DETECT_QUIET	8	----	----	----	----	----	----	----
8751640	3261912	DETECT_QUIET	2.5	----	----	----	----	----	----	----
12013552	16	DETECT_ACTIVE	2.5	----	----	----	----	----	----	----
12013568	24000000	POLLING_ACTIVE_TS1	2.5	----	----	----	----	----	----	----
36013568	16	INITIAL	2.5	----	----	----	----	----	----	----
36013584	12000000	DETECT_QUIET	2.5	----	----	----	----	----	----	----
48013584	16	DETECT_ACTIVE	2.5	----	----	----	----	----	----	----
48013600	24000000	POLLING_ACTIVE_TS1	2.5	----	----	----	----	----	----	----
72013600	16	INITIAL	2.5	----	----	----	----	----	----	----
72013616	12000000	DETECT_QUIET	2.5	----	----	----	----	----	----	----
84013616	16	DETECT_ACTIVE	2.5	----	----	----	----	----	----	----
84013632	24000000	POLLING_ACTIVE_TS1	2.5	----	----	----	----	----	----	----
108013632	16	INITIAL	2.5	----	----	----	----	----	----	----
108013648	12000000	DETECT_QUIET	2.5	----	----	----	----	----	----	----
120013648	16	DETECT_ACTIVE	2.5	----	----	----	----	----	----	----
120013664	24000000	POLLING_ACTIVE_TS1	2.5	----	----	----	----	----	----	----

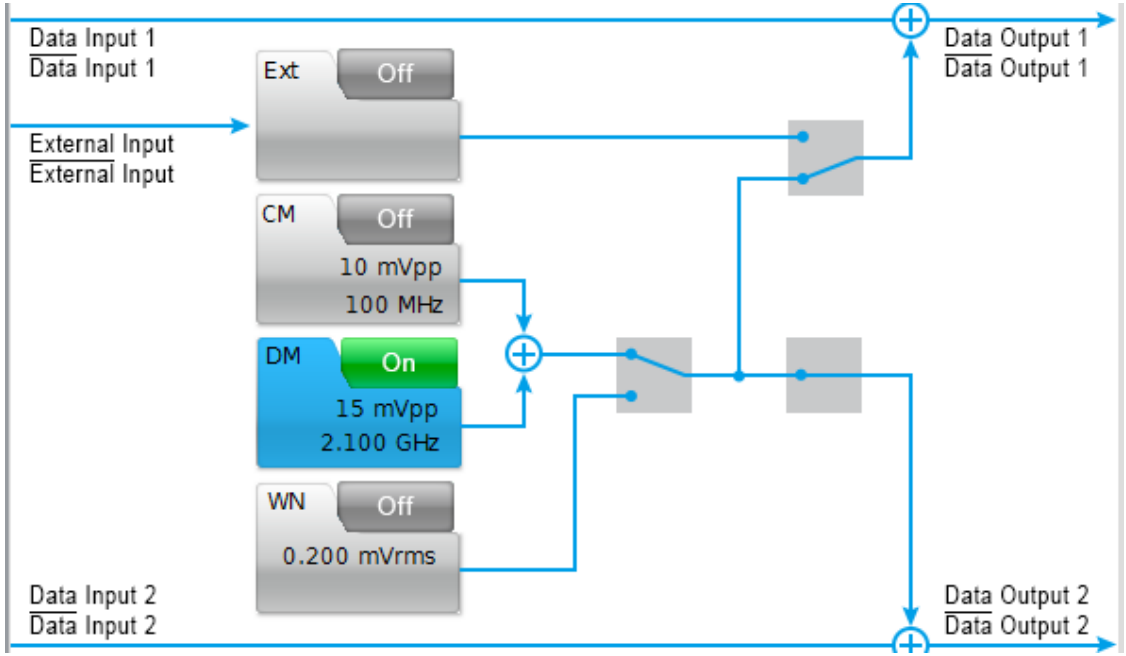


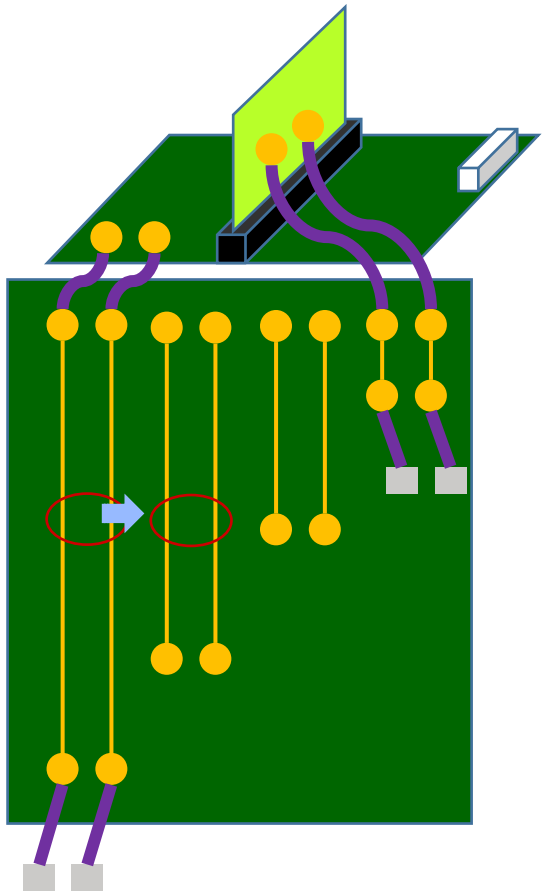
Troubleshoot : Never Become Error-Free

Reduce/Kill the stress: DMI, CMI, SJ, RJ, ISI Loss Channel

Still Error? Check the return path.



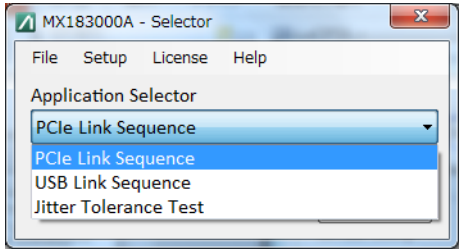


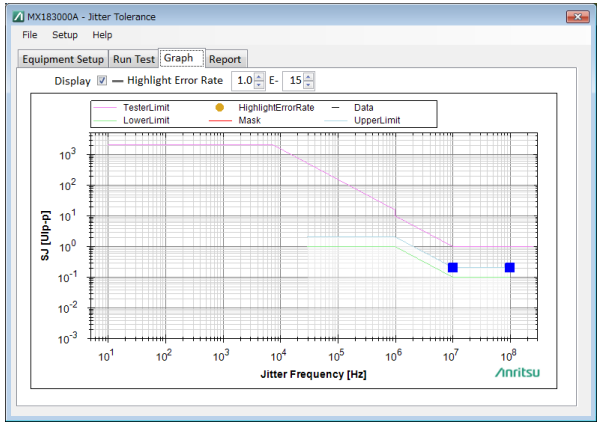


PCI Express Gen5 Rx JTOL Test

Stress Signal Calibration → Transition to Loopback Status → Stress Signal Input Test

Stress Signal Input Test (Jitter Tolerance Margin Test)



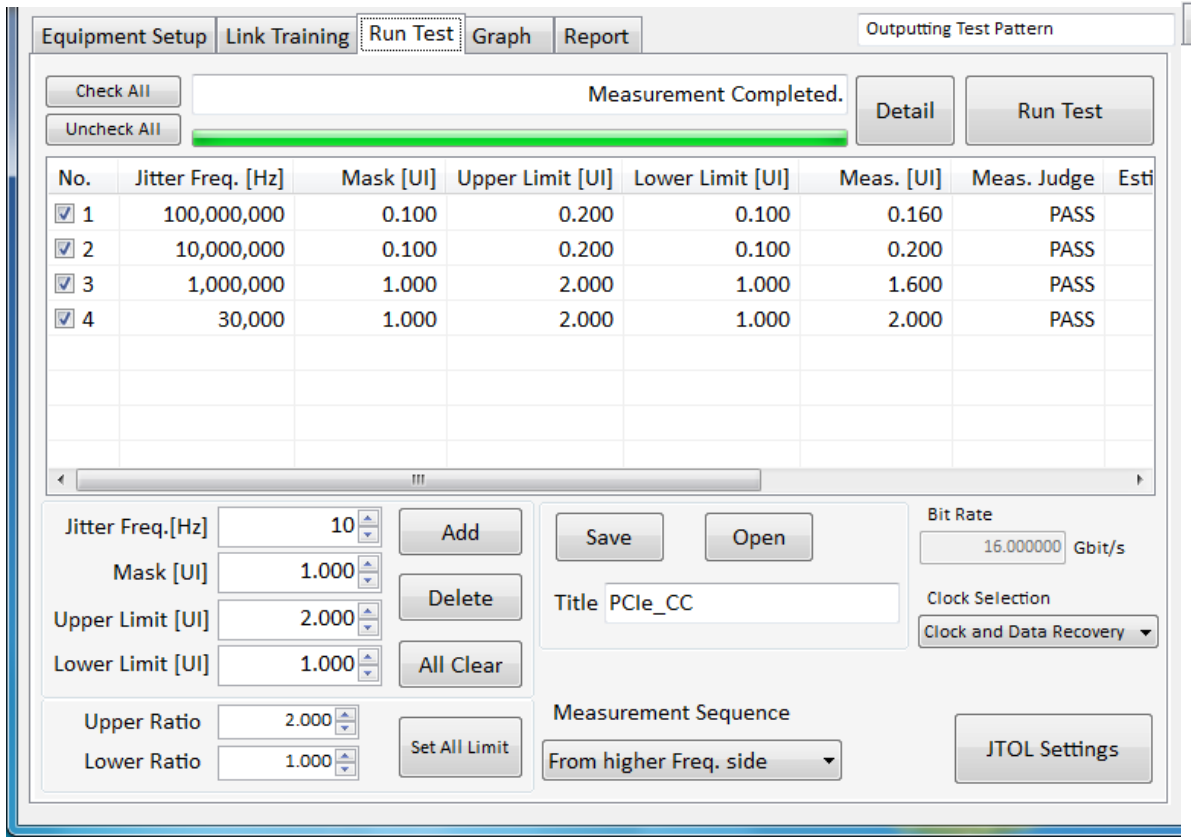


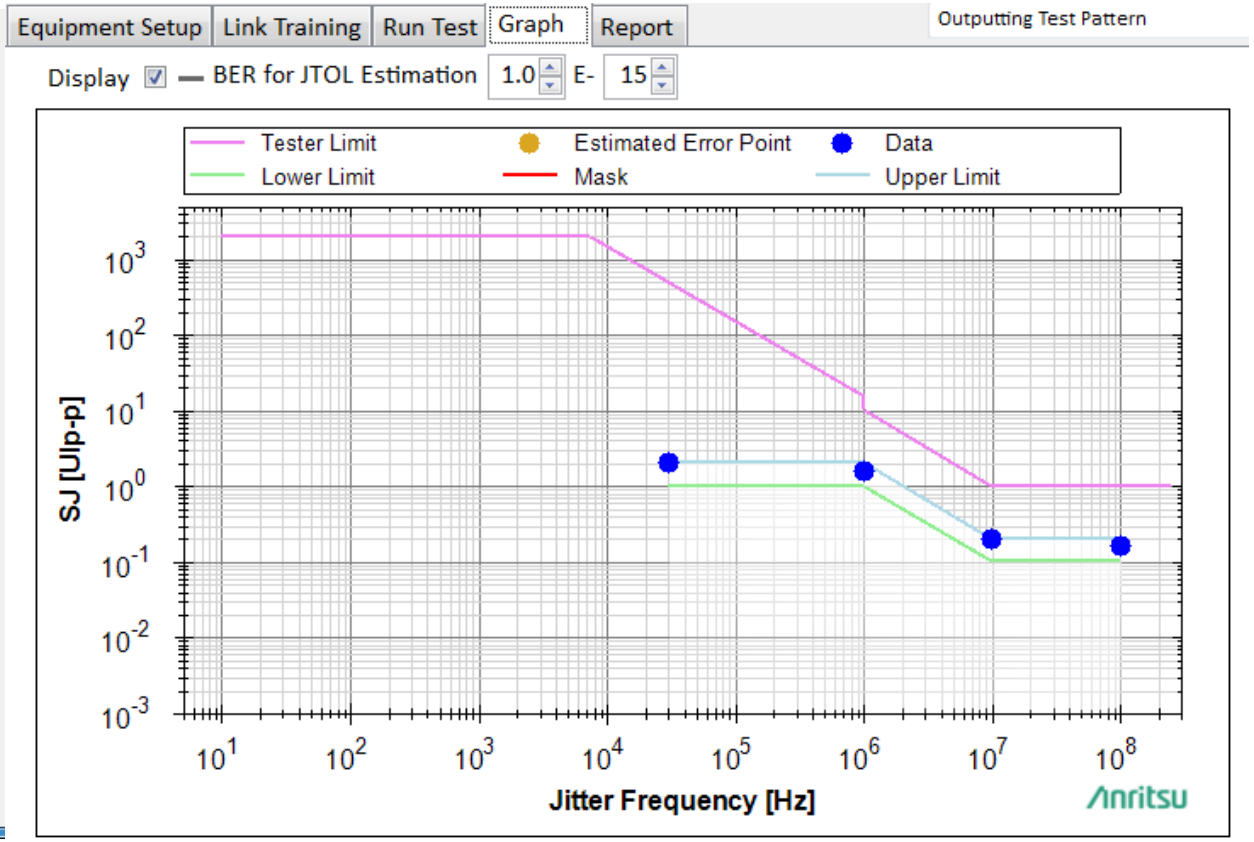
Automated Jitter Control and Tolerance Measurement

- Impresses SJ and Tests PHY Device Jitter Tolerance
- Tests Device Margin using Low BER Estimation
- Outputs Measurement Results in HTML and CSV Formats

Item	MX183000A-PL001 Specifications
Direction Search	Binary, Downward Linear, Downward Log, Upward Linear, Upward Log, Binary + Linear
Detection	Error Rate, Error Count, Estimate, FEC Uncorrectable Burst Error
Error Threshold	1.0E-3 to 1.0E-14
Highlight Error Rate	9.9E-9 to 1.0E-20 (at estimate)
Report Function	Reports results in HTML and CSV formats

Jitter Tolerance Test Example





Anritsu/Tek Stressed Eye Calibration Demonstration Video