Model 4200A-SCS
Capacitance-Voltage Unit (CVU)

User's Manual

KEITHLEY

A Tektronix Company

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Safety precautions

The following safety precautions should be observed before using this product and any associated instrumentation. Although some instruments and accessories would normally be used with nonhazardous voltages, there are situations where hazardous conditions may be present.

This product is intended for use by personnel who recognize shock hazards and are familiar with the safety precautions required to avoid possible injury. Read and follow all installation, operation, and maintenance information carefully before using the product. Refer to the user documentation for complete product specifications.

If the product is used in a manner not specified, the protection provided by the product warranty may be impaired.

The types of product users are:

Responsible body is the individual or group responsible for the use and maintenance of equipment, for ensuring that the equipment is operated within its specifications and operating limits, and for ensuring that operators are adequately trained.

Operators use the product for its intended function. They must be trained in electrical safety procedures and proper use of the instrument. They must be protected from electric shock and contact with hazardous live circuits.

Maintenance personnel perform routine procedures on the product to keep it operating properly, for example, setting the line voltage or replacing consumable materials. Maintenance procedures are described in the user documentation. The procedures explicitly state if the operator may perform them. Otherwise, they should be performed only by service personnel.

Service personnel are trained to work on live circuits, perform safe installations, and repair products. Only properly trained service personnel may perform installation and service procedures.

Keithley products are designed for use with electrical signals that are measurement, control, and data I/O connections, with low transient overvoltages, and must not be directly connected to mains voltage or to voltage sources with high transient overvoltages. Measurement Category II (as referenced in IEC 60664) connections require protection for high transient overvoltages often associated with local AC mains connections. Certain Keithley measuring instruments may be connected to mains. These instruments will be marked as category II or higher.

Unless explicitly allowed in the specifications, operating manual, and instrument labels, do not connect any instrument to mains.

Exercise extreme caution when a shock hazard is present. Lethal voltage may be present on cable connector jacks or test fixtures. The American National Standards Institute (ANSI) states that a shock hazard exists when voltage levels greater than 30 V RMS, 42.4 V peak, or 60 VDC are present. A good safety practice is to expect that hazardous voltage is present in any unknown circuit before measuring.

Operators of this product must be protected from electric shock at all times. The responsible body must ensure that operators are prevented access and/or insulated from every connection point. In some cases, connections must be exposed to potential human contact. Product operators in these circumstances must be trained to protect themselves from the risk of electric shock. If the circuit is capable of operating at or above 1000 V, no conductive part of the circuit may be exposed.

Do not connect switching cards directly to unlimited power circuits. They are intended to be used with impedance-limited sources. NEVER connect switching cards directly to AC mains. When connecting sources to switching cards, install protective devices to limit fault current and voltage to the card.

Before operating an instrument, ensure that the line cord is connected to a properly-grounded power receptacle. Inspect the connecting cables, test leads, and jumpers for possible wear, cracks, or breaks before each use.

When installing equipment where access to the main power cord is restricted, such as rack mounting, a separate main input power disconnect device must be provided in close proximity to the equipment and within easy reach of the operator.

For maximum safety, do not touch the product, test cables, or any other instruments while power is applied to the circuit under test. ALWAYS remove power from the entire test system and discharge any capacitors before: connecting or disconnecting cables or jumpers, installing or removing switching cards, or making internal changes, such as installing or removing jumpers.

Do not touch any object that could provide a current path to the common side of the circuit under test or power line (earth) ground. Always make measurements with dry hands while standing on a dry, insulated surface capable of withstanding the voltage being measured.

For safety, instruments and accessories must be used in accordance with the operating instructions. If the instruments or accessories are used in a manner not specified in the operating instructions, the protection provided by the equipment may be impaired.

Do not exceed the maximum signal levels of the instruments and accessories. Maximum signal levels are defined in the specifications and operating information and shown on the instrument panels, test fixture panels, and switching cards.

When fuses are used in a product, replace with the same type and rating for continued protection against fire hazard.

Chassis connections must only be used as shield connections for measuring circuits, NOT as protective earth (safety ground) connections.

If you are using a test fixture, keep the lid closed while power is applied to the device under test. Safe operation requires the use of a lid interlock.

If a ⏚ screw is present, connect it to protective earth (safety ground) using the wire recommended in the user documentation.

The ⚠ symbol on an instrument means caution, risk of hazard. The user must refer to the operating instructions located in the user documentation in all cases where the symbol is marked on the instrument.

The ⚡ symbol on an instrument means warning, risk of electric shock. Use standard safety precautions to avoid personal contact with these voltages.

The ♨ symbol on an instrument shows that the surface may be hot. Avoid personal contact to prevent burns.

The ⏚ symbol indicates a connection terminal to the equipment frame.

If this (Hg) symbol is on a product, it indicates that mercury is present in the display lamp. Please note that the lamp must be properly disposed of according to federal, state, and local laws.

The **WARNING** heading in the user documentation explains hazards that might result in personal injury or death. Always read the associated information very carefully before performing the indicated procedure.

The **CAUTION** heading in the user documentation explains hazards that could damage the instrument. Such damage may invalidate the warranty.

The **CAUTION** heading with the ⚠ symbol in the user documentation explains hazards that could result in moderate or minor injury or damage the instrument. Always read the associated information very carefully before performing the indicated procedure. Damage to the instrument may invalidate the warranty.

Instrumentation and accessories shall not be connected to humans.

Before performing any maintenance, disconnect the line cord and all test cables.

To maintain protection from electric shock and fire, replacement components in mains circuits — including the power transformer, test leads, and input jacks — must be purchased from Keithley. Standard fuses with applicable national safety approvals may be used if the rating and type are the same. The detachable mains power cord provided with the instrument may only be replaced with a similarly rated power cord. Other components that are not safety-related may be purchased from other suppliers as long as they are equivalent to the original component (note that selected parts should be purchased only through Keithley to maintain accuracy and functionality of the product). If you are unsure about the applicability of a replacement component, call a Keithley office for information.

Unless otherwise noted in product-specific literature, Keithley instruments are designed to operate indoors only, in the following environment: Altitude at or below 2,000 m (6,562 ft); temperature 0 °C to 50 °C (32 °F to 122 °F); and pollution degree 1 or 2.

To clean an instrument, use a cloth dampened with deionized water or mild, water-based cleaner. Clean the exterior of the instrument only. Do not apply cleaner directly to the instrument or allow liquids to enter or spill on the instrument. Products that consist of a circuit board with no case or chassis (e.g., a data acquisition board for installation into a computer) should never require cleaning if handled according to instructions. If the board becomes contaminated and operation is affected, the board should be returned to the factory for proper cleaning/servicing.

Safety precaution revision as of June 2017.

Table of contents

Introduction

In this section:

Introduction

This document provides information about the 4210-CVU and 4215-CVU capacitance-voltage units, including:

- Connections (on page 2-1): Basic information on connecting CVUs to DUTs, making test equipment connections, making control and data connections, and configuring the system in KCon.

- Setting up CVUs in Clarius (on page 3-1): Provides a brief example of setting up CVUs in Clarius and descriptions of the terminal and test settings.

- C-V projects (on page 4-1): Provides descriptions of the C-V projects in Clarius.

- Make C-V measurements on a MOSCAP (on page 5-1): Presents a step-by-step application example.

Capacitance-Voltage Unit (CVU)

The 4210-CVU and 4215-CVU Multi-Frequency Capacitance-Voltage Units are impedance measurement modules that can be installed in the 4200A-SCS.

Capacitance-voltage (C-V) measurements are often used to characterize the gate oxide thickness, oxide defect density, and doping profile of MOSFETs. In these measurements, as the gate voltage varies, the capacitance of the gate to the drain and source changes. Capacitance measurements are typically made using an ac technique. The CVUs measure ac impedance by applying a dc bias voltage and sourcing an ac voltage across the device under test (DUT) and then measuring the resultant ac current and phase angle.

The 4210-CVU operates from 1 kHz to 10 MHz. The ac test signal (10 mV$_{RMS}$ to 100 mV$_{RMS}$) can be dc voltage biased from -30 V to $+30$ V.

The 4215-CVU operates from 1 kHz to 10 MHz at 1 kHz resolution. The ac test signal (10 mV to 1 V$_{RMS}$) can be dc voltage biased from -30 V to $+30$ V.

Test signal

The test signal can be set for the following frequencies.

For the 4210-CVU:

- 1 kHz to 10 kHz in 1 kHz increments

- 10 kHz to 100 kHz in 10 kHz increments

- 100 kHz to 1 MHz in 100 kHz increments

- 1 MHz to 10 MHz in 1 MHz increments

The ac signal output level can be set from 10 mV$_{RMS}$ to 100 mV$_{RMS}$ (1 mV$_{RMS}$ resolution). The output impedance is 100 Ω (typical). The ac voltage measure range is 100 mV$_{RMS}$.

The ranges available to measure current are 1 µA, 30 µA, or 1 mA. With autorange selected, range selection is done automatically.

For the 4215-CVU:

- 1 kHz to 10 MHz in 1 kHz increments

The ac signal output level can be set from 10 mV$_{RMS}$ to 1 V$_{RMS}$ (1 mV$_{RMS}$ resolution). The output impedance is 100 Ω (typical). The ac voltage measure range is 1 mV$_{RMS}$.

The ranges available to measure current are 1 µA, 30 µA, or 1 mA. With autorange selected, range selection is done automatically.

Connections

In this section:

CVU connections

The CVU is shipped with four red 1.5 m SMA cables (male-to-male, 100 Ω). These characterized cables must be used for connection to the CVU to achieve optimum performance.

If you have the 4200-CVU-PROBER-KIT, you also have four red 3 m SMA cables (male-to-male, 100 Ω).

Connection notes

- Use only the supplied red SMA cables for connections to the 4210-CVU or 4215-CVU.

- Do not use a mix of cable lengths on different CVU terminals.

- Use the supplied torque wrench to tighten SMA cable connectors to 8 in. lb.

- In Clarius, the cable length setting of a test must match the length of the SMA cables used for your setup.

- If you need to run connection compensation, do it after setting up connections or after making changes to existing connections, but before running any tests. See the Connection compensation (on page 2-8) topic.

- When making connections from the CVU to the device under test (DUT), make sure the shields of the SMA cables are connected as close as possible to the DUT.

- Use coaxial cables to extend SMA shielding to the DUT, then connect them.

Prober accessories for the CVU

The Model 4200-CVU-PROBER-KIT is an accessory kit that provides connections to a wide variety of prober and manipulator types. This kit contains a combination of triaxial and BNC adaptors and barrels that accommodate most prober connection requirements.

The following figure shows the accessories that are included in the kit.

Figure 1: Model 4200-CVU-PROBER-KIT
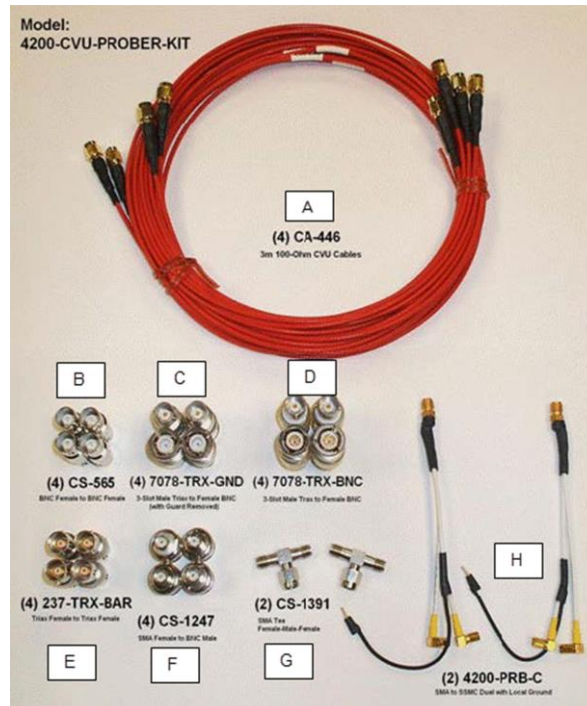
The following table lists the cables and adapters provided with the prober kit.

Supplied cables and adapters for the Model 4200-CVU-PROBER-KIT

Item	Quantity	Keithley part number or model number	Description
A	4	CA-446	Red SMA cables, male to male, 100 Ω, 3 m
B	4	CS-565	BNC female to BNC female adapter
C	4	7078-TRX-GND	Triaxial male to BNC female adapter (with guard removed)
D	4	7078-TRX-BNC	Triaxial male to BNC female adapter (with guard connected to the inner shield of the adapter)
E	4	237-TRX-BAR	Triaxial female to triaxial female adapter
F	4	CS-1247	SMA female to BNC male adapter
G	2	CS-1391	SMA Tee adapter (female, male, female)
H	2	4200-PRB-C	SMA to SSMC dual (with local ground)

When using the Model 4200-PRB-C cables (item H), be sure you jumper the shields together at the probe tips. Each stackable black banana plug is connected to the outer shield of the cables.

Typical CVU test connections to a DUT

The shields of the SMA cables must be connected together and extended as far as possible to the device under test (DUT), as shown in the following figure.

Use the supplied torque wrench to tighten the SMA connections to 8 in. lb.

Figure 2: Measurement circuit (simplified)
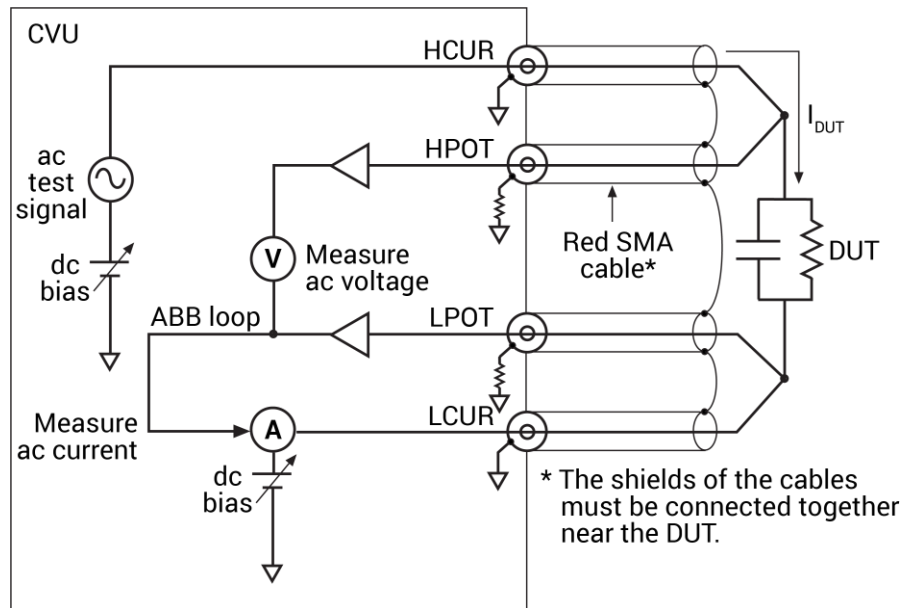
NOTE

You can swap the HCUR and HPOT and LCUR and LPOT terminal functionality in Clarius.

The following figure shows typical connections to a DUT installed in a test fixture that has BNC bulkhead connectors. Use a conductive test fixture with the bulkhead connectors mounted directly to the test fixture. Do not use insulators between the connectors and test fixture. The cables and adapters shown are the ones supplied with the 4210-CVU or 4215-CVU.

Figure 3: Typical CVU connections to a DUT in a test fixture
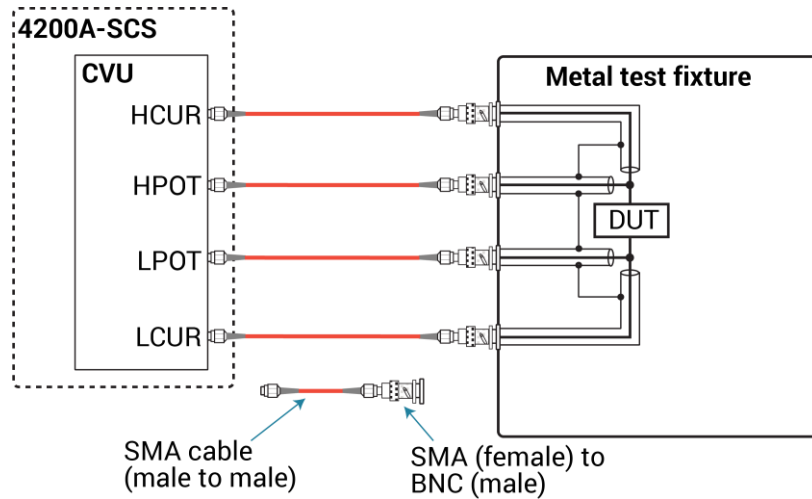
Simplified model of a DUT

The CVU makes ac impedance measurements (Z_{DUT}) of the device under test (DUT) by sourcing an ac test voltage across the device and measuring the resulting ac current and ac voltage.

The ac current is measured as shown in Typical CVU test connections to a DUT (on page 2-3).

The HCUR/HPOT and LCUR/LPOT terminal pairs are interchangeable. Each provides the full capability of the other pair.

The simplified model of a DUT is a resistor and a capacitor. As shown in the next figure, the 4210-CVU or 4215-CVU can measure the DUT as a series configuration of the resistor-capacitor (RC) or as a parallel RC configuration.

Figure 4: Measure models (simplified)
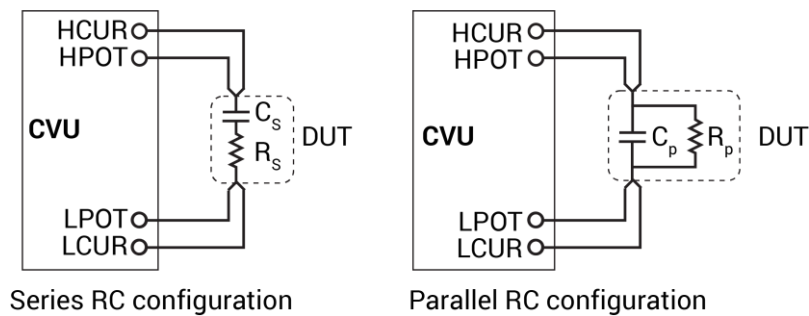
Typical test connections to a probe card

The 4200-CVU-PROBER-KIT includes 3-meter SMA cables and connection accessories to connect the 4210-CVU or 4215-CVU to a probe card. Refer to Prober accessories for the CVU (on page 2-2) for a list of the supplied items.

The following figure shows typical test connections to a probe card. The connections use triaxial female connectors. The probe kit includes two types of BNC to triaxial adapters. The 7078-TRX-BNC has the guard connected to the inner shield of the adapter. The 7078-TRX-GND has the guard disconnected. In most applications, the 7078-TRX-BNC is the preferred adaptor.

Figure 5: Typical connections to a probe card
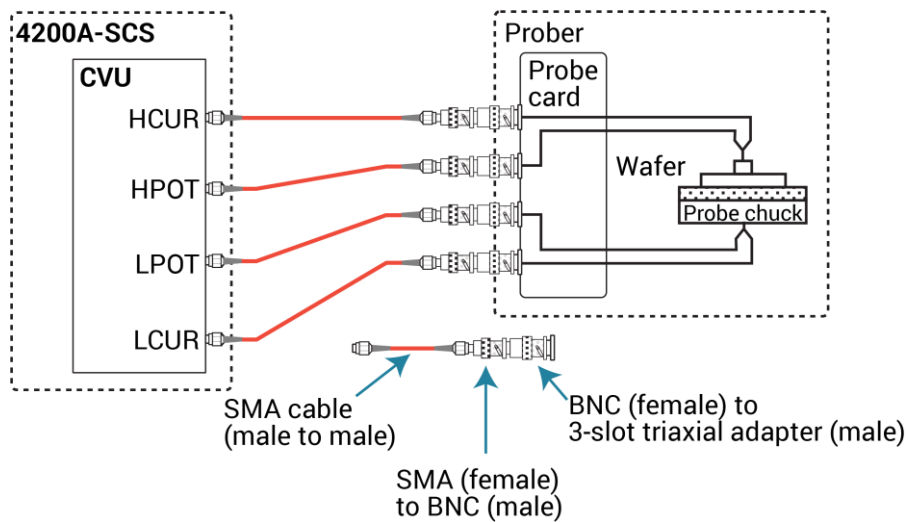
NOTE

The shields of the SMA cables must be connected together and extended as far as possible to the DUT, as shown in Typical CVU test connections to a DUT (on page 2-3).

NOTE

If the probe card uses BNC (female) connectors, you do not need the BNC-to-triaxial adapters.

Typical CVU matrix card connections

In your project, you can automate the use of a CVU and other instrumentation using a switching matrix and actions to control the switching. When the project is run, the switching matrix automatically makes the required instrument connections for each test in the project.

The next figures show typical connections for a switch system using a Series 700 Switching System with the 7174A Matrix Card installed.

NOTE

You can also use the 7072 Matrix Card for C-V testing. If you are using the 7072, you must use rows G and H and local (2-wire) sensing.

The SMA cables and adapters shown in the following figures are supplied with the CVU or the 4200-CVU-PROBER-KIT. The triaxial and BNC cables are not supplied. The prober kit includes two types of BNC-to-triaxial adapters that connect directly to the rows of the matrix. The 7078-TRX-BNC has the guard connected to the inner shield of the adapter. The 7078-TRX-GND has the guard disconnected.

This figure shows connections for local (2-wire) sensing with the CVU connected to rows E and F of the matrix. This is the connection scheme for the `cap-iv-cv-matrix` project. For details, see "cap-iv-cv-matrix" in the *Model 4200A-SCS Capacitance-Voltage Unit (CVU) User's Manual*.

Figure 6: Test connections for a switch matrix - local (2-wire) sensing
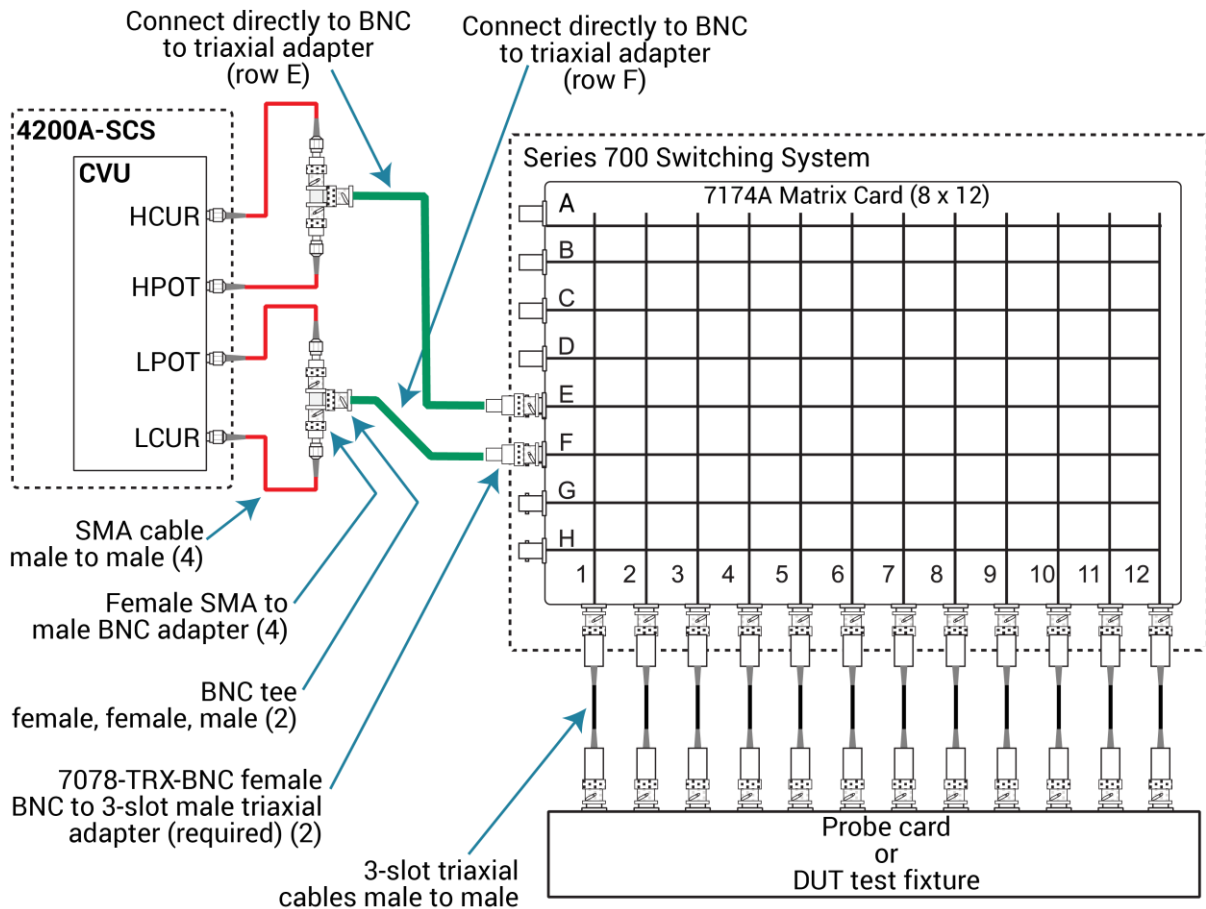
The following figure shows connections for remote (4-wire) sensing.

Figure 7: Test connections for a switch matrix - remote (4-wire) sensing
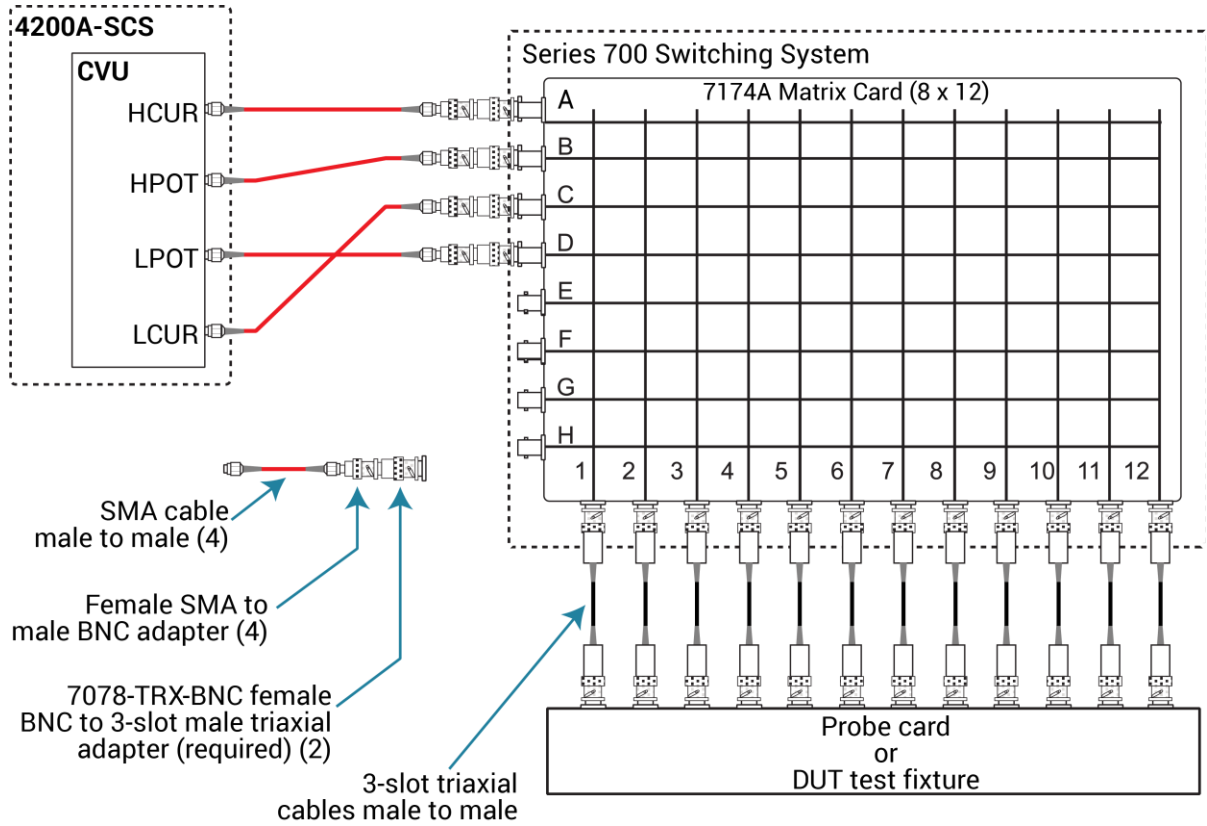
NOTE

The 7078-TRX-BNC adapters must be used in order to extend SMA shielding through the matrix card.

NOTE

The shields of the SMA cables must be connected together and extended as far as possible to the DUT, as shown in <u>Typical CVU test connections to a DUT</u> (on page 2-3).

Connection compensation

You can correct offset and gain errors caused by the connections between the CVU and the device under test (DUT) by using connection compensation. To use correction, you:

- Generate connection compensation data for open, short, and load conditions.

- Enable CVU connection compensation.

When a test is run, the enabled compensation values are factored in by each measurement.

If open, short, or load compensation is disabled, those compensation values are not used by the test.

Once compensation values are stored, they are available to any project that uses a CVU.

NOTE

Update connection compensation any time the connection setup is changed or disturbed. Changes in temperature or humidity do not affect connection compensation.

NOTE

If the CVU is connected to a 4200A-CVIV Multi-Switch, run the `cvu-cviv-comp-collect` action. Refer to the *4200A-CVIV Multi-Switch User's Manual* for detail.

Use the following general guidelines to determine which correction needs to be done:

- **Open** correction: Offset correction for small capacitances (>1 MΩ, large impedance).

- **Short** correction: Offset correction for large capacitances (<10 Ω, small impedance).

- **Load** correction: Resistive load correction for gain error. Keithley recommends a load that is as close in impedance to the cabling system (100 Ω) as possible. The load must have an impedance versus frequency characteristic that is purely resistive over the frequency range of subsequent measurements.

Generate open connection compensation data

Open connection compensation is usually done to offset correction for small capacitances.

Open compensation is done with all the cables, adaptors, switch matrices, and other hardware connections connected to the device under test in the test circuit. The probes must be lifted up or the device must be removed from the test fixture.

To generate open connection compensation data:

1. Make the connections to the CVU, as shown in the following figure. For remote (4-wire) sensing, the shields of the four SMA cables must be connected as close as possible.

Figure 8: Connections for open connection compensation CVU
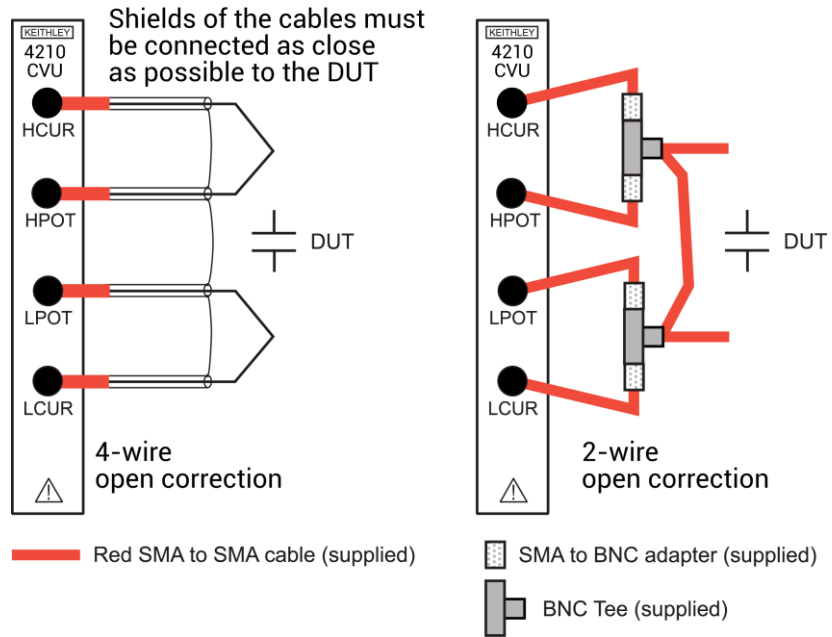
2. In Clarius, select **Tools**. The Clarius Tools dialog box opens.

Figure 9: Clarius Tools dialog box

3. Select **CVU Connection Compensation**.

Figure 10: CVU Connection Compensation dialog box

4. Select the **cable length**. You can select:
    - **0 m:** Use if measurements are made at the terminals of the CVU (no cables).
    - **1.5 m:** Use with the standard red SMA cables (part number CA-447A) that are supplied with the CVU.
    - **3 m:** Use with the red SMA cables (part number CA-446) that are supplied with the 4200-CVU-PROBER-KIT. You can also use this setting if you are using a switching matrix.
    - **Custom:** Cable length coefficients are measured by the user using the Measure Custom Cable Length option under Advanced Compensation.

5. If you selected Custom cable length, select **Advanced Compensation** and select **Measure Custom Cable Length**. Follow the on-screen instructions.

6. If you are using a switching matrix, close the matrix switches that connect the CVU to the open. Refer to "Switch matrix control" in *Model 4200A-SCS Prober and External Instrument Control*.

7. In the Clarius CVU Connection Compensation dialog box, select **Measure Open**.

8. Follow the instructions.

9. Select **OK**.

Generate short connection compensation data

Short connection compensation is usually done to offset correction for large capacitances.

Short compensation is done by connecting all the CVU terminals directly together. A known short is connected to the CVU terminals through all the cables, adaptors, and probes that may be in the test circuit. You can make a short at the wafer level by shorting all probes together.

To generate short connection compensation data:

1. Make the connections to the CVU, as shown in the following figure. For remote (4-wire) sensing, the shields of the four SMA cables must be connected.

Figure 11: Connections for short and load connection compensation
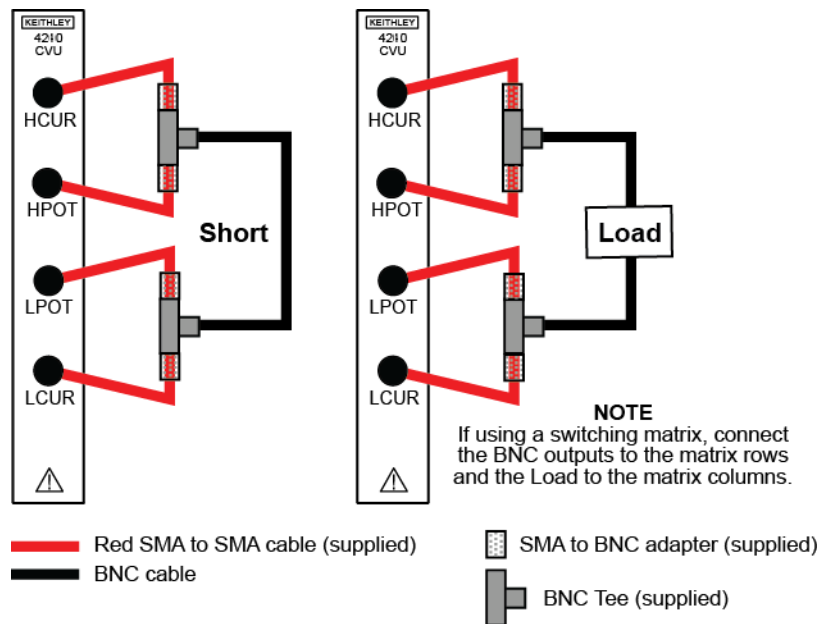
2. In Clarius, select **Tools**. The Clarius Tools dialog box opens.

Figure 12: Clarius Tools dialog box
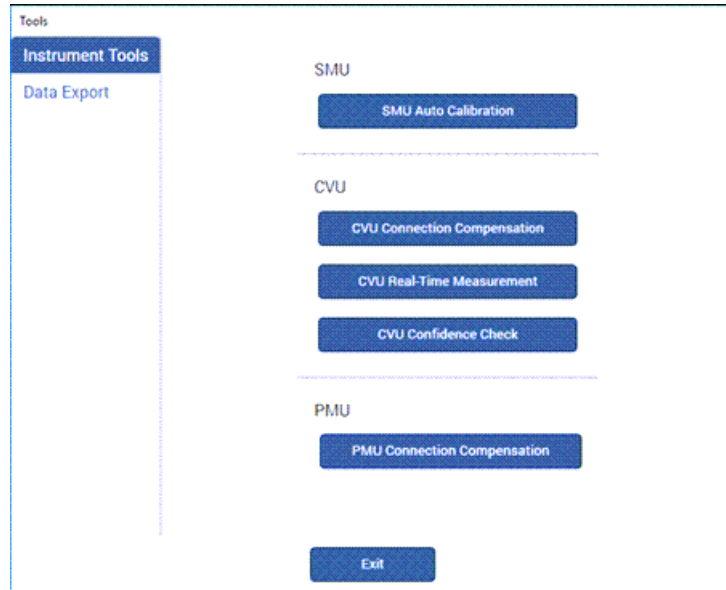
3. Select **CVU Connection Compensation**.

Figure 13: CVU Connection Compensation dialog box

4. Select the **cable length**. You can select:

    ▪   **0 m:** Use if measurements are made at the terminals of the CVU (no cables).

    ▪   **1.5 m:** Use with the standard red SMA cables (part number CA-447A) that are supplied with the CVU.

    ▪   **3 m:** Use with the red SMA cables (part number CA-446) that are supplied with the 4200-CVU-PROBER-KIT. You can also use this setting if you are using a switching matrix.

    ▪   **Custom:** Cable length coefficients are measured by the user using the Measure Custom Cable Length option under Advanced Compensation.

5. If you selected Custom cable length, select **Advanced Compensation** and select **Measure Custom Cable Length**. Follow the on-screen instructions.

6. If you are using a switching matrix, close the matrix switches that connect the CVU to the open. Refer to "Switch matrix control" in *Model 4200A-SCS Prober and External Instrument Control*.

7. In the Clarius CVU Connection Compensation dialog box, select **Measure Short**.

8. Follow the instructions.

9. Select **OK**.

Generate load connection compensation data

Loads are reference resistors, typically 50 or 100 Ω or less, that must be resistive and constant over the entire frequency range (1 kHz to 10 MHz). A load is connected to the output terminals using all the cables, adaptors, probes and other hardware in the test circuit.

To generate load correction data:

1. Make the connections to the CVU. See the "Test connections for a switch matrix" in the *Model 4200A-SCS Capacitance-Voltage Unit (CVU) User's Manual*.

2. In Clarius, select **Tools**. The Clarius Tools dialog box opens.

Figure 14: Clarius Tools dialog box
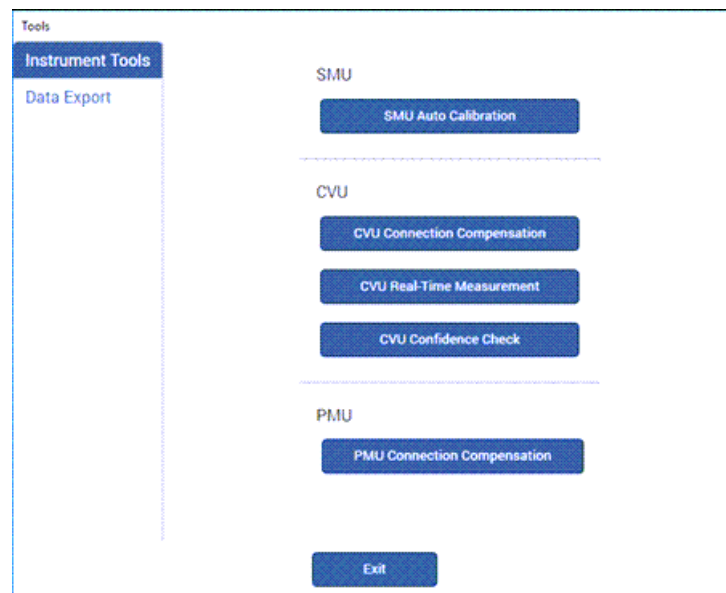
3. Select **CVU Connection Compensation**.

Figure 15: CVU Connection Compensation dialog box

4. Select the **cable length**. You can select:
    - **0 m:** Use if measurements are made at the terminals of the CVU (no cables).
    - **1.5 m:** Use with the standard red SMA cables (part number CA-447A) that are supplied with the CVU.
    - **3 m:** Use with the red SMA cables (part number CA-446) that are supplied with the 4200-CVU-PROBER-KIT. You can also use this setting if you are using a switching matrix.
    - **Custom:** Cable length coefficients are measured by the user using the Measure Custom Cable Length option under Advanced Compensation.

5. If you selected Custom cable length, select **Advanced Compensation** and select **Measure Custom Cable Length**. Follow the on-screen instructions.

6. If you are using a switching matrix, close the matrix switches that connect the CVU to the open. Refer to "Switch matrix control" in *Model 4200A-SCS Prober and External Instrument Control*.

7. If it is not open, select **Advanced Compensation**.

8. In Measure Load, enter the value of the load in ohms.

9. Select **Measure Load**.

10. Follow the instructions.

11. Select **OK**.

Compensation data

You can view the compensation data. Clarius lists R and jX compensation values for every test frequency and measurement range for open, short, and load.

To view the data generated by connection compensation:

1.   In Clarius, select **Tools**.

2.   Select **CVU Connection Compensation**.

3.   Select **Advanced Compensation**.

4.   Next to View Compensation Data, select the data you would like to display: **Open**, **Short**, or **Load**.

5.   Select **View Compensation Data**.

6.   Select the **HI** tab to review the high side values.

7.   Select the **LO** tab to review the low side values.

Figure 16: Open compensation values example

| | 1mA | | 30uA | | 1uA | |
Frequency	R	jX	R	jX	R	jX
1kHz	1e-012	0	1e-012	0	1e-012	0
2kHz	0.0192332	0.0092446	0.0192332	0.0092446	0.0192332	0.0092446
3kHz	0.0240222	0.00620513	0.0240222	0.00620513	0.0240222	0.00620513
4kHz	0.0251885	0.00343866	0.0251885	0.00343866	0.0251885	0.00343866
5kHz	0.0251798	-0.00192463	0.0251798	-0.00192463	0.0251798	-0.00192463
6kHz	0.0247988	-0.00374154	0.0247988	-0.00374154	0.0247988	-0.00374154
7kHz	0.0243094	-0.00494131	0.0243094	-0.00494131	0.0243094	-0.00494131
8kHz	0.0241997	-0.00483867	0.0241997	-0.00483867	0.0241997	-0.00483867
9kHz	0.0229851	-0.00625016	0.0229851	-0.00625016	0.0229851	-0.00625016
10kHz	0.0230555	-0.00879264	0.0230555	-0.00879264	0.0230555	-0.00879264

HI   LO

Note: A value of R=1e15 and jX=1e15 indicates that a measurement could not be made and default values will be used for the Open Compensation.

Open: Mon Sep 26 14:58:31 2016 ;

CVU Path: Direct

OK

Enable compensation

To use the values generated by connection compensation, you need to enable compensation for each test.

When compensation is enabled, the most recently acquired CVU compensation data is applied. Compensation values can be gathered using the CVU Connection Compensation option in Tools or through actions and user modules.

To enable compensation:

1. Select the test from the project tree.

2. Select **Configure**.

3. Select the terminal in the center pane.

4. In the right pane, select **Terminal Settings**.

5. Under Compensation, select the types of compensation as needed.

6. Make sure **Cable Length** is the same as the setting that was used in the Tools > CVU Connection Compensation dialog box to generate connection compensation data.

Figure 17: Enable connection compensation

ABB unbalance errors

The CVU uses the autobalancing bridge (ABB) technique to achieve accurate impedance measurements. ABB creates a virtual ground at the DUT to minimize measurement error. Every CVU measurement is made with ABB active. The ABB always attempts to lock the low side of the DUT to virtual ground.

If the ABB fails to lock, the measurement is made, but may be out of specification. If this occurs, the returned data is flagged and shown in yellow on a blue background on the Analyze sheet.

The most common reasons that ABB fails to lock are:

- The cable lengths on the CVU terminals are not the same

- HPOT or LPOT terminals were disconnected

- Excessive noise on the LPOT terminal

- High frequency sources

- Physical cable lengths do not match the cable length set in Clarius

- Improperly torqued SMA cables

- Sub-optimal I_{RANGE} setting

- Too much parasitic load on the low side of the DUT

You can use CVU Confidence Check to help troubleshoot ABB errors. Refer to Run an open check and short check (on page 2-17) for instructions on performing a confidence check.

Run an open check and short check

CVU Confidence Check is a diagnostic tool that allows you to check the integrity of open and short connections and connections to a device under test (DUT). When the CVU is connected to the DUT, the Confidence Check displays the measured readings in real time in the Messages area of Clarius.

An open or short confidence check makes a measurement on the high and the low sides of the test circuit.

To do a CVU confidence check:

1. If you are using a switching matrix, connect the switching matrix to the CVU and DUT or the short as explained in "Test connections for a switch matrix" in the *Model 4200A-SCS Capacitance-Voltage Unit (CVU) User's Manual*.

2. For the short check, close the matrix switches to connect the CVU to the DUT or short. For the open check, also close the matrix switches, but lift the probes or disconnect the DUT.
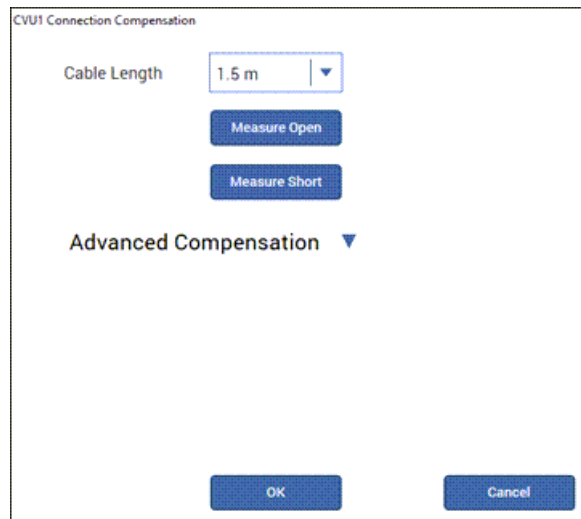
3. In Clarius, select **Tools**. The Clarius Tools dialog box opens.

Figure 18: Clarius Tools dialog box

4. Select **CVU Confidence Check**.
5. Select **Check Open** or **Check Short**.

Figure 19: CVU Confidence Check dialog box
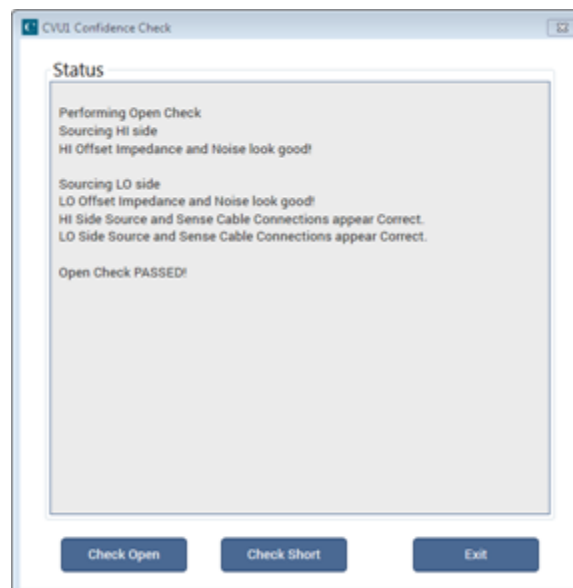
6. Follow the instructions and click **OK**.

When the check is complete, the dialog box displays the results of the test. If the test failed, the results include suggestions for troubleshooting.

CVU Real-Time Measurement

The CVU Real-Time Measurement provides a direct real-time user interface to the CVU to help you set up and debug your system. For example, you can use it to confirm that contact has been made with the pads on a wafer. The measurements are independent of the open and short confidence checks.

To make real-time measurements:

1. In Clarius, select **Tools**. The Clarius Tools dialog box opens.

Figure 20: Clarius Tools dialog box

2. Select **Instrument Tools**.
3. Select **CVU Real-Time Measurement**.

Figure 21: Real-Time Measurement dialog box

4. Select the parameters for which you want to return results.

5. Set the Speed, AC Drive Conditions, and DC Bias Conditions for the conditions you want to test.

6. Select **Run**. The results for the selected parameters are displayed at the top of the dialog box.

Setting up CVUs in Clarius

In this section:

CVU project example

The following example shows you how to use the 4210-CVU or 4215-CVU in a project to make a capacitance measurement.

The example assumes you have a CVU connected to a test fixture as described in Typical CVU test connections to a DUT (on page 2-3).

In this test, you sweep the dc bias from −5 V to 5 V in 0.2 V steps, with a 1 MHz capacitance measurement made at each step.

Select a project

Select a project:

1. Start **Clarius**.
2. Run Connection compensation (on page 2-8) to correct for offset and gain errors caused by the connections.
3. Choose **Select**.
4. Select **Projects** to display the Project Library in the center pane.
5. Search for demo. The Demo Project is displayed, as shown in the following figure.

Figure 22: Demo Project selected
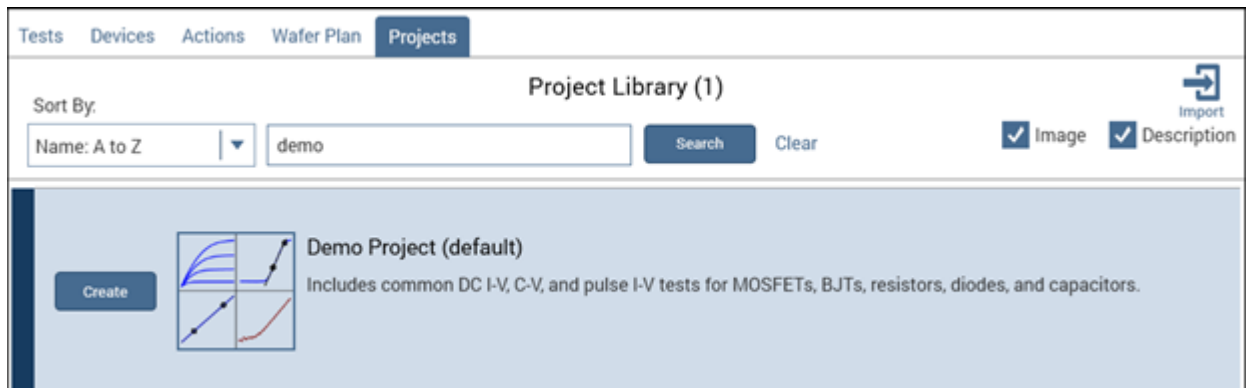
6. Select **Create**. You are prompted to replace the existing project.
7. Select **Yes**. The project is displayed in the project tree.

Figure 23: Demo Project (default) in the project tree
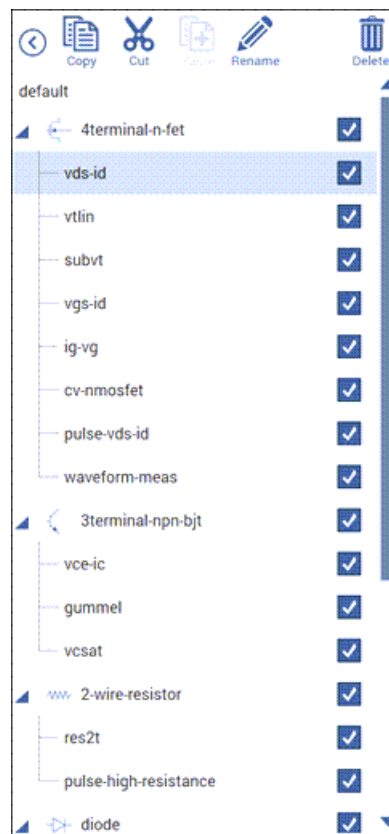
Configure the test

This example uses the `cv-cap` test, which measures the capacitance as a function of a linear voltage sweep of a capacitor.

Configure the cv-cap test:

1. In the project tree, select the **cv-cap** test.
2. Select **Configure**. The key parameters are displayed in the center pane.

Figure 24: cv-cap key parameters
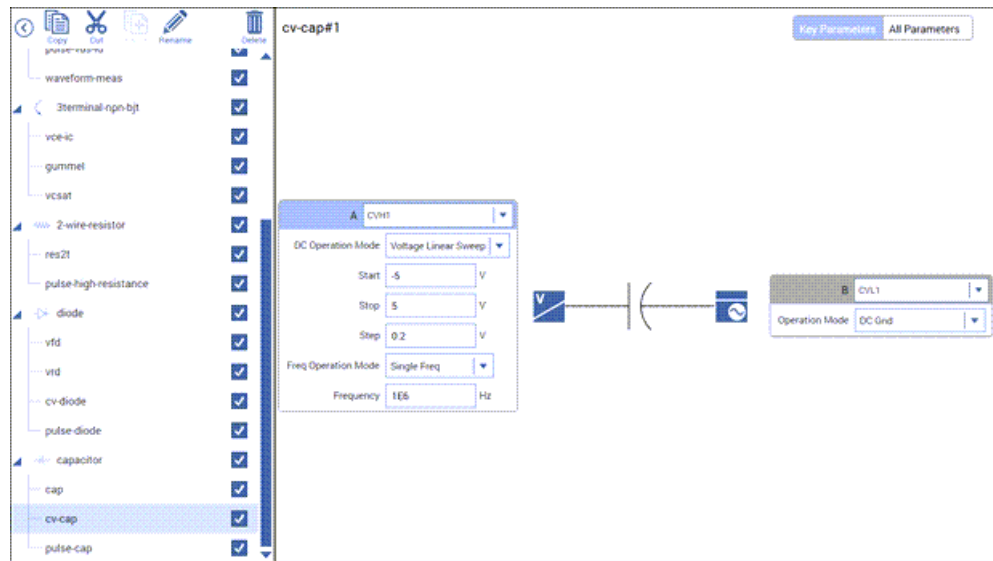
3. Verify the settings for CVH1:
   - Operation Mode: Voltage Linear Sweep
   - Start: −5 V
   - Stop: 5 V
   - Step: 0.2 V
   - Frequency Operation Mode: Single Freq
   - Frequency: 1 MHz

Run the test and review results

To run the cv-cap test and review the results:

1. Select **Run**.
2. Select **Analyze**. The test results are shown as data in a spreadsheet and on the graph, as shown in the figure below.
3. To export the data, select **Save Data**.

4. To save the information in the Run sheet, select **Save Sheet**. The information is saved in a Microsoft® Excel® spreadsheet format.

5. To save the information in the graph, select the **Graph File Format** and select **Save Graph1**. The graph is saved into the selected file type.

Note that the extracted NOISE parameter is displayed on the graph.

For information on changing how the graph is displayed, refer to "Change the graph settings" in the *Model 4200A-SCS Clarius User's Manual*.

Figure 25: cv-cap test results
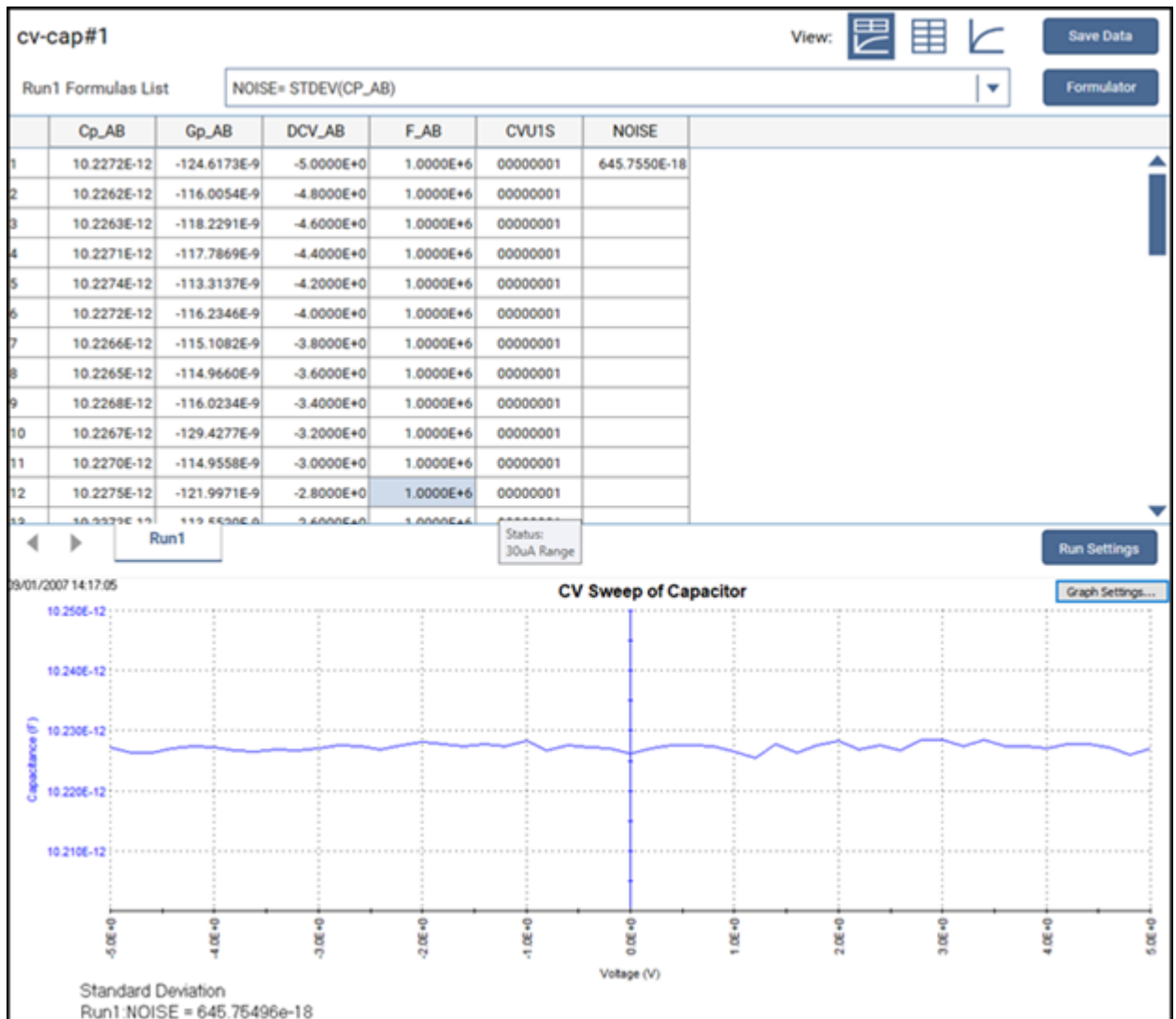
Selecting the DC Operation Mode

DC Operation Mode selects the most common settings for the selected test type. Selecting the appropriate mode simplifies terminal and test configuration. The following topics describe the operation modes that are available when a CVU is selected as the instrument.

For descriptions of the parameters that you can set for the operation modes, refer to CVU - all terminal parameters (on page 3-23).

Voltage Bias

The Voltage Bias operation mode maintains a selected constant-voltage state at the terminal.

Voltage Linear Sweep

When you select the Voltage Linear Sweep operation mode, the test increments through a series of constant voltage steps. You define the start and stop voltages and the voltage size between each step. An example is shown in the next figure.

Figure 26: Example linear sweep
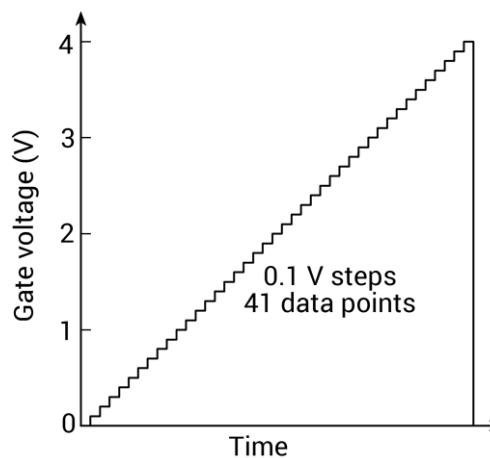
The voltage sweep generates parametric curve data that is recorded in the Analyze pane.

Voltage List Sweep

The Voltage List Sweep operation mode allows you to customize the voltage values for each step of the sweep. List Sweeps allow you to make measurements only at selected forced voltages. For example, they allow you to skip unimportant measurement points or to synthesize a custom sweep that is based on a special mathematical equation. You can also use list sweeps to make pulsed measurements to avoid overheating of sensitive devices. The following figure illustrates a possible list sweep.

Figure 27: Example voltage list sweep
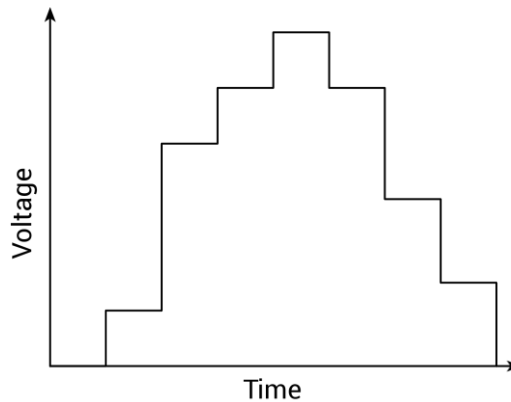
The voltage list sweep generates parametric curve data that is recorded in the Analyze pane.

Voltage Step

The Voltage Step operation mode increments through evenly-spaced, constant voltage steps over a range that you specify. The time interval for each step is determined automatically by the time required to complete a sweep.

For each step, parametric curve data is generated. The data is recorded in the Analyze pane.

DC Gnd operation mode - CVU

Automatically selected for the CVL terminal.

Selecting the Freq Operation Mode

The Frequency Operation Mode selects the most common settings for the selected test type. Selecting the appropriate mode simplifies terminal and test configuration.

If you have a 4210-CVU, you can select Single Freq, Freq Linear Sweep, or Freq Step. If you have a 4215-CVU, you can also select Freq Log Sweep or Freq List Sweep.

The following topics describe these operation modes.

Frequency Single Freq

The CVU makes a single frequency reading.

Frequency Linear Sweep

When performing a frequency sweep, the CVU steps through all the frequency points from start to stop at the frequency intervals set by the step.

Freq Log Sweep

This sweep is similar to the linear sweep except that the steps are done on a logarithmic scale.

Freq List Sweep

The Freq List Sweep operation mode allows you to customize the voltage values for each step of the sweep. List Sweeps allow you to make measurements only at selected frequencies. For example, they allow you to skip unimportant measurement points or to synthesize a custom sweep that is based on a special mathematical equation.

Freq Step

When the Freq Step operation mode is selected, the CVU sweeps through all the frequency points from start to stop for each dc step.

Figure 28: Frequency sweep - DC step operation mode
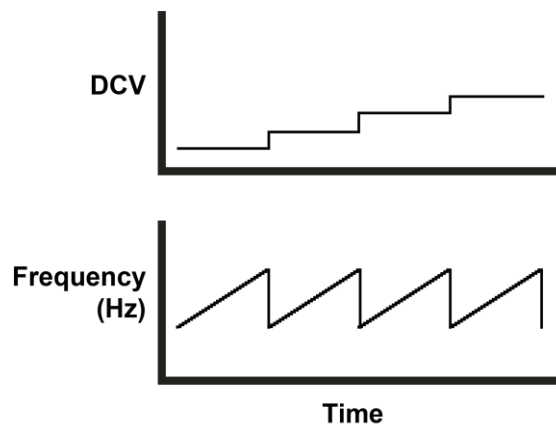
For example, if the:

- Start frequency is 800 kHz

- Stop frequency is 3 MHz

- The dc start value is −1

- Stop value is 1

- Step value is 0.5

The CVU sweeps through the frequency points 800 kHz, 900 kHz, 1 MHz, 2 MHz, and 3 MHz for dc biases −1 V, −0.5 V, 0 V, 0.5 V, and 1 V.

When this test is run, the following sequence occurs:

1. The dc source goes to the Presoak voltage.
2. After the hold time (set in the Test Settings), dc bias goes to the Start voltage.
3. After the delays, the CVU makes a measurement for the Start Frequency point. The ac signal is applied before the start of the measurement.
4. The CVU sweeps through the frequency points until it reaches the Stop Frequency point.
5. The dc bias goes to the next voltage as defined by the Step value.
6. Steps 4 and 5 are repeated until the dc bias reaches the Stop value.

Making additional test settings

You can refine your test settings using the Test Settings tab in the right pane.

Figure 29: CVU Test Settings pane

From the Test Settings pane, you can open additional options by selecting **Advanced**.

Figure 30: CVU Advanced Test Settings Pane
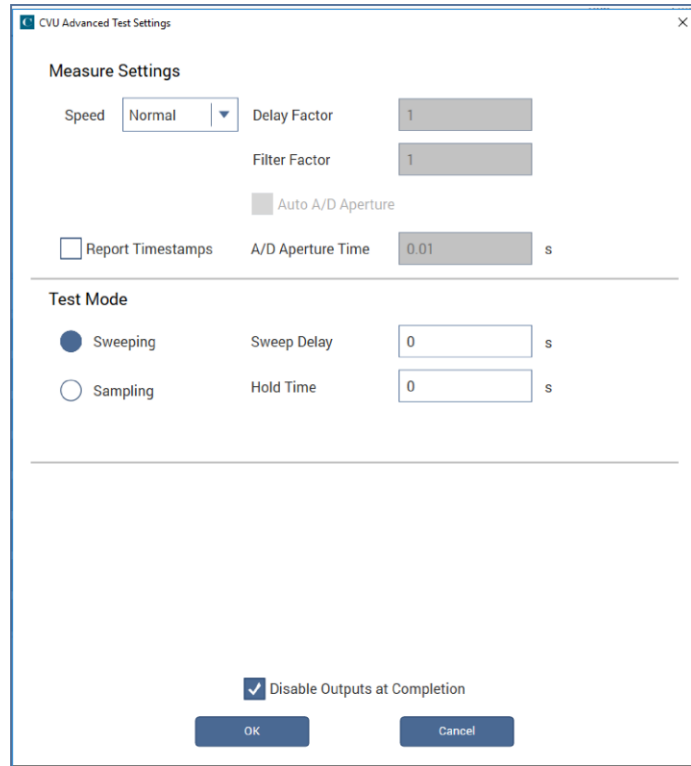
Refer to for descriptions of the test settings.

Typical test setups with timing diagrams

The following topics describe typical test setups with the related timing diagrams.

DC bias function and sweep characteristics

The ac test signal can be biased with a static dc level (-30 V to $+30$ V), or a voltage sweep (up or down). You can also perform a frequency sweep (up or down).

The following figure shows an example of dc bias waveform. In this example, the dc bias is set to 0 V, but you can set it to any valid dc bias level. You specify the number of measurements to make.

Figure 31: DC Bias waveform (example)
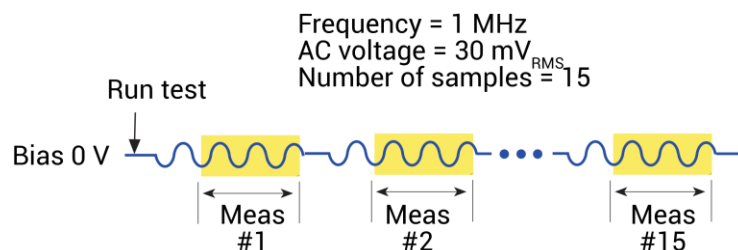
The following figure shows an example of dc voltage sweep. You specify the start voltage, stop voltage, and step voltage. The number of measure points is calculated by the CVU.

Figure 32: DC voltage sweep (example)
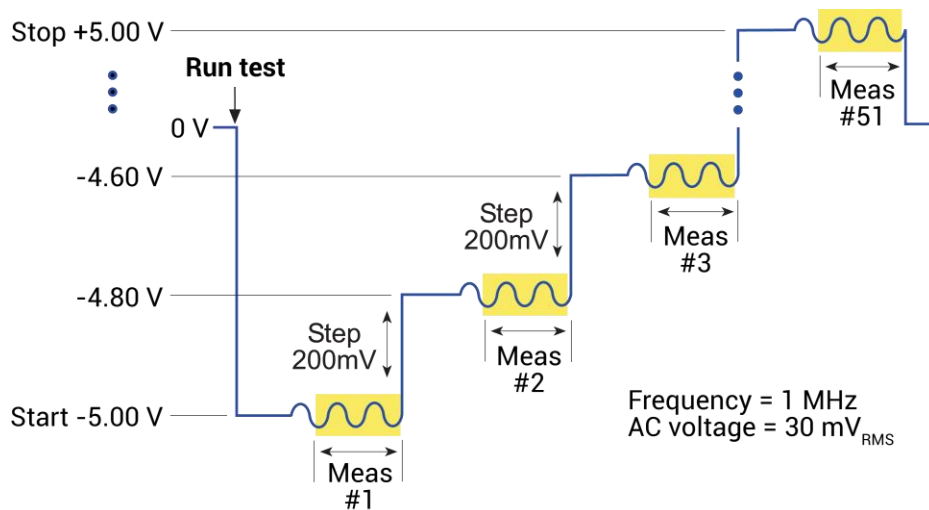
The following figure shows an example of a frequency sweep. You specify the start frequency and the stop frequency. The CVU calculates the number of measure points.

Figure 33: Frequency sweep (example)
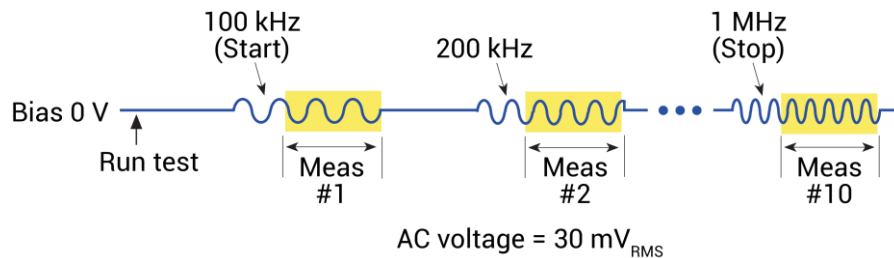
If you are setting up a voltage list sweep, you specify the voltage levels for the sweep.

If you are setting up a voltage step frequency sweep, the sweep includes voltage stepping. A frequency sweep is performed for every voltage step point.

If you are setting up a frequency step voltage sweep, the sweep includes frequency stepping. A voltage sweep is performed for every frequency point.

The following examples are examples of these setups in Clarius.

CVU using voltage bias

Make the following Test Settings for a dc bias with a single frequency. This sweep measures CP-Gp.

- Speed: Normal

- Report Timestamps: Selected

- Mode: Sampling

- Interval: 0.25 s

- Number of Samples: 10

- Hold Time: 1 s

Make the following Terminal Settings for CVH1:

- DC Operation Mode: Voltage Bias

- Presoak: 5 V

- DC Bias: 1 V

- Frequency Operation Mode: Single Freq

- Frequency: 100000 Hz

- Parameters: Cp-Gp

- Compensation as needed

When this test is run, the following force-measure sequence occurs:

1. The dc source goes to the Presoak voltage of 5 V for the hold time (1 s).
2. The dc source goes to the dc bias voltage of 1 V.
3. After the built-in system delay and interval (0.25 s), the CVU makes a measurement. The ac test signal is applied just before the start of the measurement. The ac drive is turned off after the measurement is completed. This step is repeated for every sample.

Figure 34: CVU Voltage Bias output
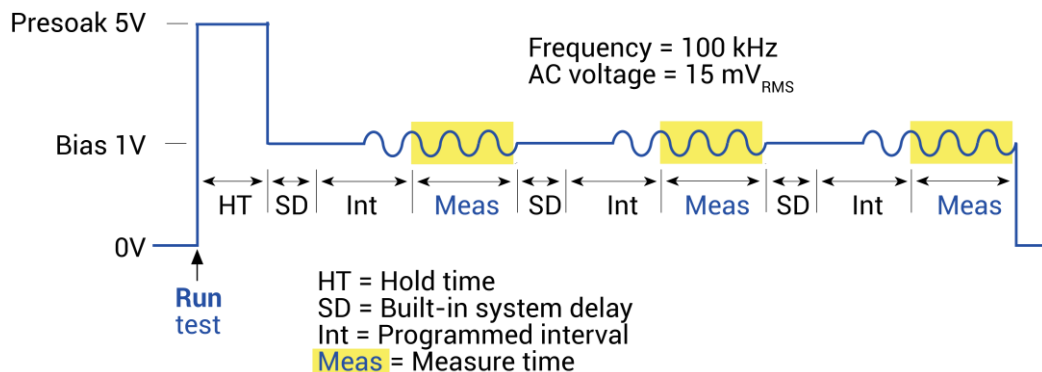
CVU using voltage sweep

Make the following Test Settings:

- Speed: Normal
- Report Timestamps: Selected
- Mode: Sweeping
- Sweep Delay: 0.1 s
- Hold Time: 1 s

For this test, make the following Terminal Settings for CVH1:

- DC Operation Mode: Voltage Linear Sweep
- Presoak: 5 V
- Start: 5 V
- Stop: 3 V
- Step: 1 V
- Frequency Operation Mode: Single Freq
- Frequency: 100000 Hz
- Dual sweep: Selected
- Parameters: Cp-Gp
- Compensation as needed

The following figure shows the Advanced terminal settings for a voltage linear sweep. This sweep measures Cp-Gp.

Figure 35: 4215-CVU voltage sweep

When this test is run, the following force-measure sequence occurs:

1. The dc source goes to the presoak voltage of −5 V for the hold time.

2. The dc bias voltage goes to the first step of the sweep (1 V).

3. After the built-in system delay and sweep delay, the 4210-CVU or 4215-CVU makes a measurement. The ac test signal is applied before the start of the measurement. The ac drive is turned off after the measurement is made.

4. Steps 2 and 3 are repeated for the 2 V and 3 V dc bias voltage steps. The sweep delay repeats at the beginning of each subsequent step.

The sweep delay and hold time are set from the Test Settings.

To do a dual CVU voltage sweep, select **Dual Sweep** in the Terminal Settings pane. If Dual Sweep is selected, after the stop step is measured, the sweep continues in the reverse direction. For the settings shown in the above figure, the dual sweep steps through 1 V, 2 V, 3 V, 3 V, 2 V, and 1 V. The number of measurements doubles to six.

Figure 36: CVU voltage sweep output
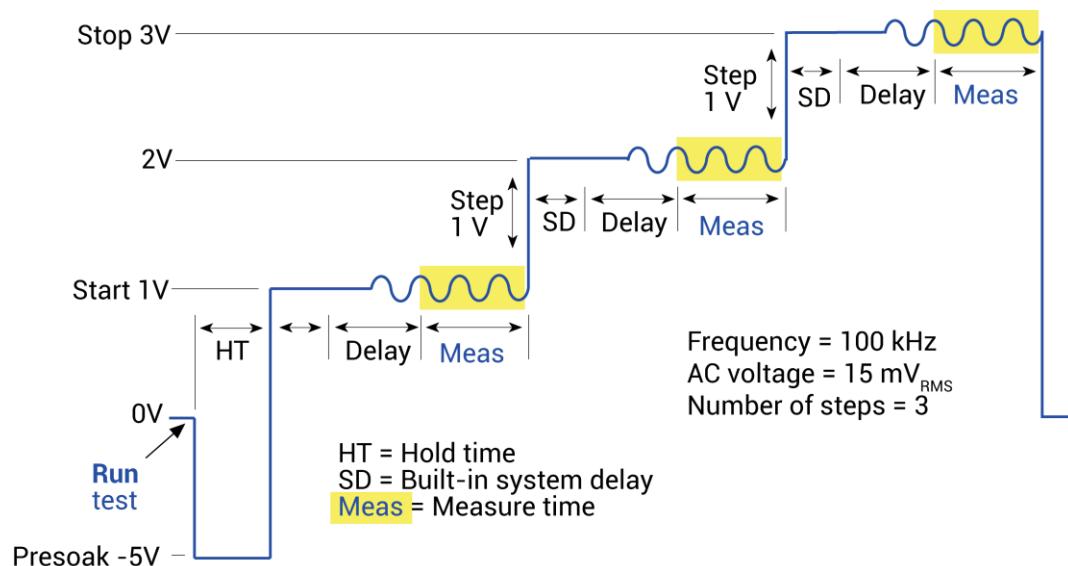
CVU using voltage list sweep

Make the following Test Settings:

- Speed: Normal

- Report Timestamps: Selected

- Mode: Sweeping

- Sweep Delay: 0.1 s

- Hold Time: 1 s

For this test, make the following Terminal Settings for CVH1:

- DC Operation Mode: Voltage List Sweep
- Presoak: 5 V
- Voltage: Enter Values in List
- Frequency Operation Mode: Single Freq
- Frequency: 100000 Hz
- AC Drive Signal: 30 mV RMS
- Parameters: Cp-Gp
- Compensation as needed

This figure shows an example of the Advanced Terminal Settings dialog box when the DC Operation Mode is set to Voltage List Sweep, the Freq Operation Mode is set to Single Freq, and the Measure Parameters are set to measure Cp-Gp.

Figure 37: CVU Voltage List Sweep
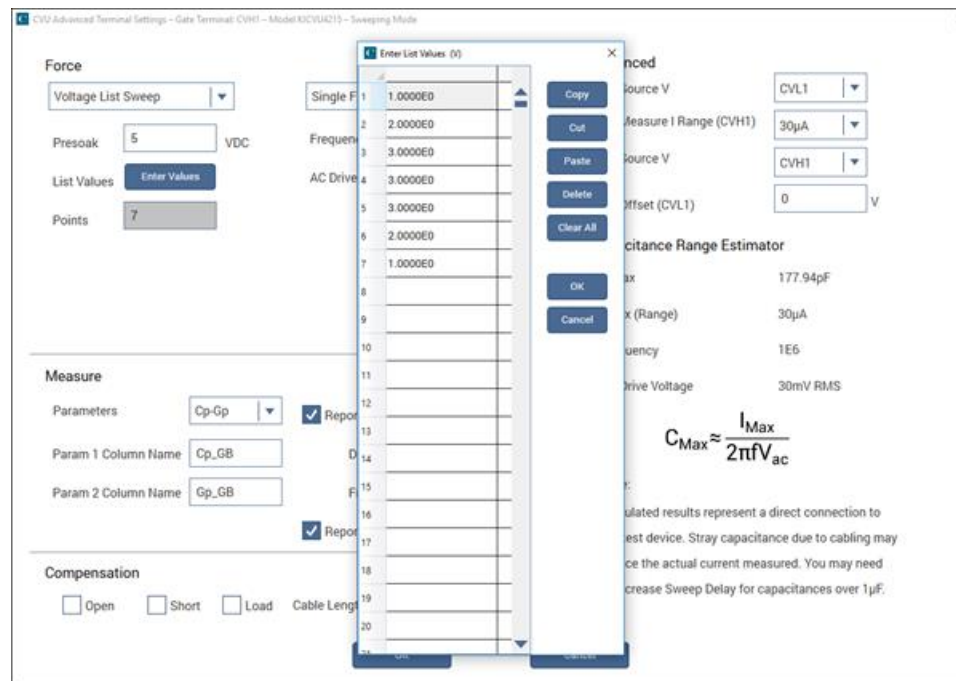
When this test is run, this sequence occurs:

1. The dc source goes to the presoak voltage for the hold time. Typically, the presoak voltage is at the same potential as the first point in the sweep to allow the device to charge up to equilibrium before measurements begin.
2. The dc bias goes to the first sweep point voltage.

3. After the built-in system delay and sweep delay, the 4210-CVU or 4215-CVU makes a measurement. The ac test signal is applied just before the start of the measurement. The ac drive is turned off after the measurement is completed.

4. Steps 2 and 3 are repeated for remaining dc bias voltages. The sweep delay repeats at the beginning of each step.

Figure 38: CVU Voltage List Sweep output
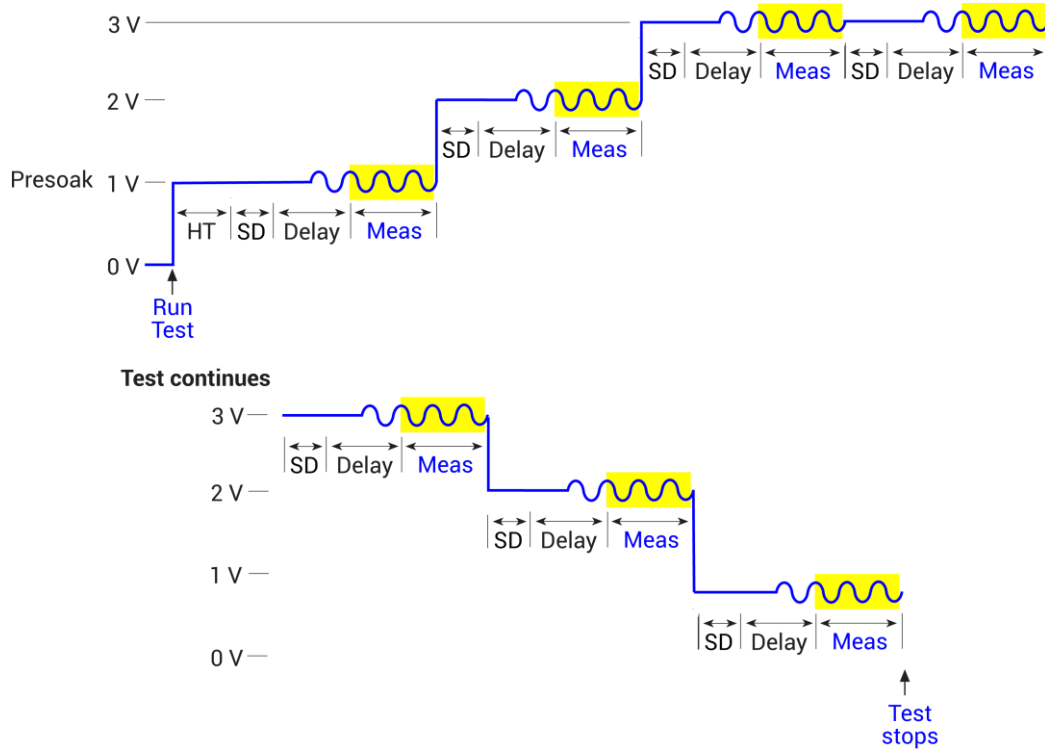
CVU using a dc voltage bias and a frequency sweep

Make the following Test Settings:

- Speed: Normal

- Report Timestamps: Selected

- Mode: Sweeping

- Hold Time: 1 s

- Sweep Delay: 0.1 s

For this test, make the following Terminal Settings for CVH1:

- DC Operation Mode: Voltage Bias

- Presoak: 5 V

- DC Bias: 1V

- Frequency Operation Mode: Freq Linear Sweep

- Start Frequency: 100000 Hz

- Stop Frequency: 300000 Hz

- Step Frequency: 100000 Hz

- AC Drive Signal: 15 mV RMS

- Parameters: Cp-Gp

- Compensation as needed

The following shows an example of the Advanced Terminal Settings dialog box when the DC Operation Mode is set to Voltage Bias and the Freq Operation Mode is set to Freq Linear Sweep. Note that this example also applies to the Freq Log Sweep and Freq List Sweep modes of the 4215-CVU.

Figure 39: DC Voltage Bias and Freq Linear Sweep

When this test is run, the following force-measure sequence occurs:

1. The dc source goes to the Presoak voltage of 5 V for the hold time.
2. The dc bias goes to 1 V for the system delay and sweep delay times and remains on during the frequency sweep.
3. The 4210-CVU or 4215-CVU makes a measurement for the first frequency point (100 kHz). The ac test signal is applied before the start of the measurement. The ac drive is turned off after the measurement is made.
4. Step 3 is repeated for the other frequency points. The system delay and sweep delay are repeated for each subsequent measurement.

The sweep delay and hold time are set in the Test Settings pane.

Figure 40: CVU Frequency Sweep (bias) output
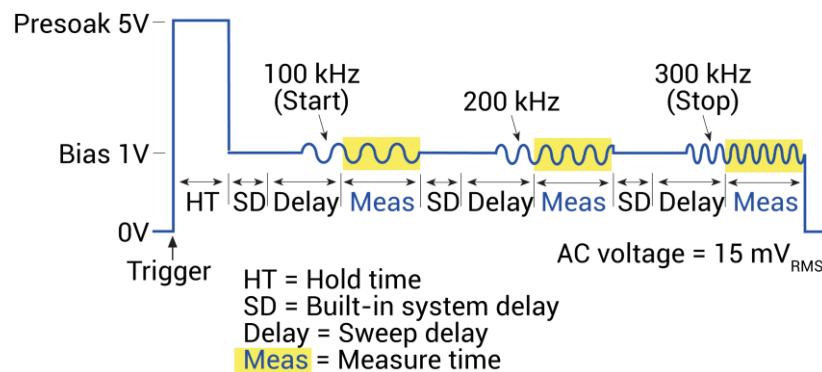
CVU frequency sweep - DC step

Make the following Test Settings:

- Speed: Normal
- Report Timestamps: Selected
- Mode: Sweeping
- Sweep Delay: 0.1 s
- Hold Time: 1 s

For this test, make the following Terminal Settings for CVH1:

- DC Operation Mode: Voltage Step

- Presoak: -1 V

- Start: 0 V

- Stop: 2 V

- Step: 1 V

- Frequency Operation Mode: Freq Linear Sweep

- Start Frequency: 100000 Hz

- Stop Frequency: 200000 Hz

- Step Frequency: 100000 Hz

- AC Drive Signal: 30 mV RMS

- Parameters: Cp-Gp

- Compensation as needed

The following figures show examples of the Advanced Terminal Settings dialog box for a test set to Voltage Step and Frequency Linear Sweep Note that this example also applies to Freq Log Sweep and Freq List Sweep modes of the 4215-CVU. This test is set to measure Cp-Gp.

Figure 41: Voltage Step and Freq Linear Sweep

When this test is run, the following source-measure sequence occurs:

1. The dc source goes to the presoak voltage of −1 V.

2. After the hold time, dc bias goes to 0 V.

3. After the system delay and the sweep delay, the 4210-CVU or 4215-CVU makes a measurement for the 100 kHz frequency point. The ac signal is applied before the start of the measurement.

4. After another system delay and sweep delay, a measurement is made for the 200 kHz frequency point.

5. The dc bias goes to 1 V.

6. Steps 3 and 4 are repeated.

7. The dc bias goes to 2 V.

8. Steps 3 and 4 are repeated.

The sweep delay and hold time are set in the Test Settings pane for the test.

Figure 42: CVU Frequency Sweep (step) output
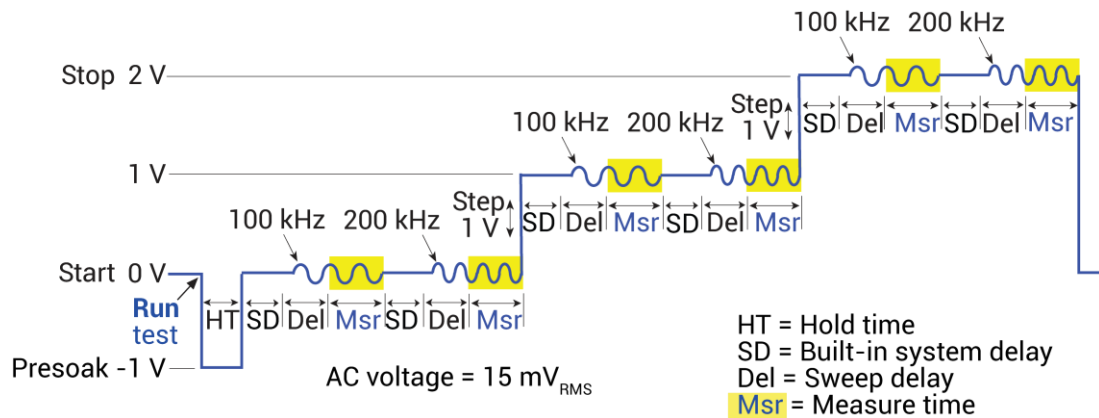
CVU voltage linear sweep - frequency step

Make the following Test Settings:

- Speed: Normal

- Report Timestamps: Selected

- Mode: Sampling

- Sweep Delay: 0.1 s

- Hold Time: 1 s

For this test, make the following Terminal Settings for CVH1:

- DC Operation Mode: Voltage Linear Sweep

- Presoak: -1 V

- Start: 0 V

- Stop: 2 V

- Step: 1 V

- Frequency Operation Mode: Freq Step

- Start Frequency: 100000 Hz

- Stop Frequency: 200000 Hz

- Step Frequency: 100000 Hz

- AC Drive Signal: 30 mV RMS

- Parameters: Cp-Gp

- Compensation as needed

The following figure shows an example of the Advanced Terminal Settings dialog box for a test set to DC Sweep - Frequency Step. The test is set to measure Cp-Gp.

Figure 43: 4210-CVU Voltage Linear Sweep - Freq Step
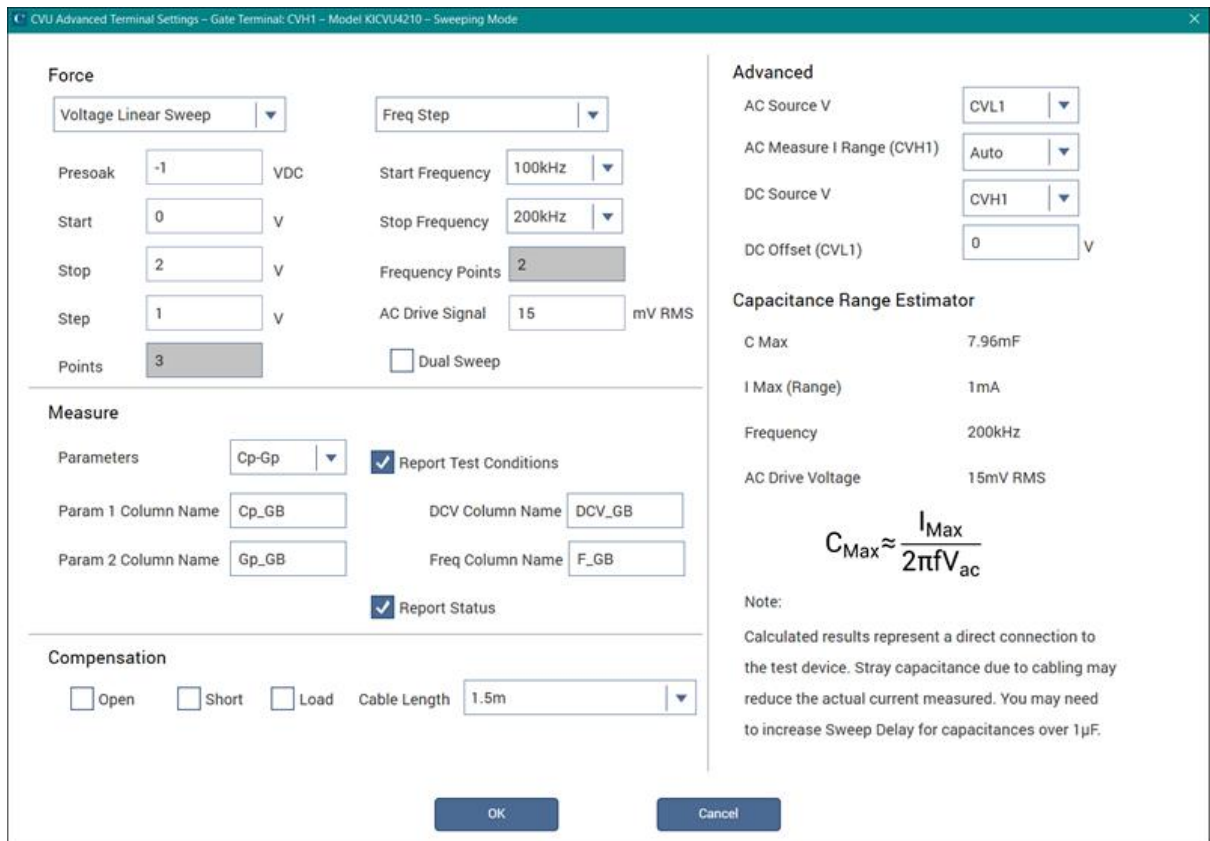
Figure 44: 4215-CVU Voltage Linear Sweep and Freq Step
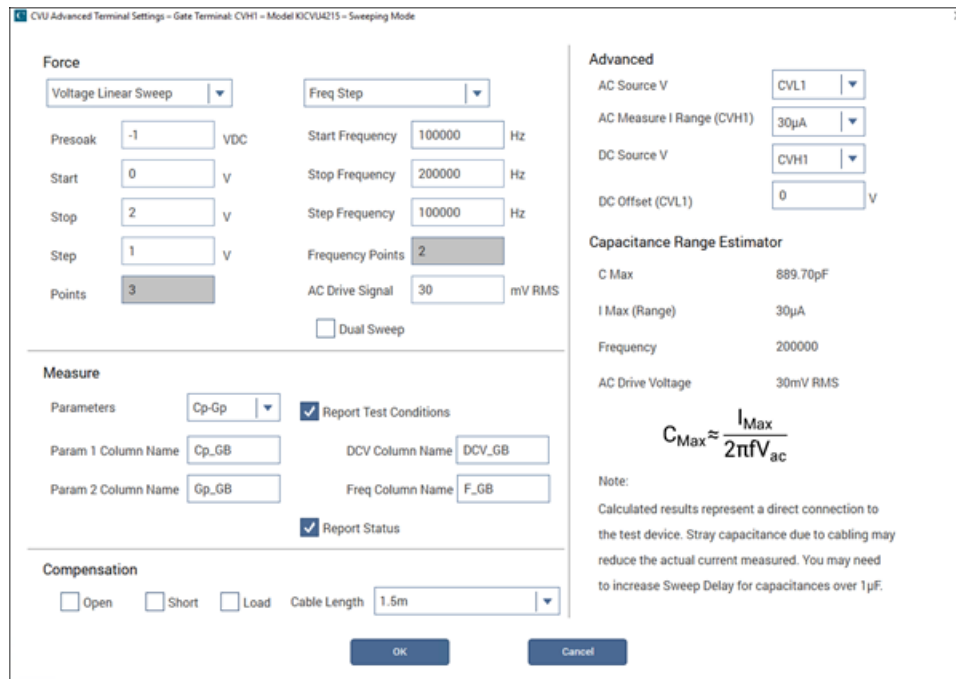
When this test is run, the following source-measure sequence occurs:

1. The dc source goes to the presoak voltage of -1.

2. After the hold time, dc bias goes to 0 V.

3. The 100 kHz frequency step point is set. The ac signal is applied before the start of the measurement.

4. After the system delay and sweep delay, a measurement is made for the 0 V dc sweep point.

5. After another system delay and sweep delay, a measurement is made for the next dc sweep point. This is repeated until the last sweep point measurement is made.

6. The frequency goes to 200 kHz.

7. Steps 4 and 5 are repeated.

The sweep delay and hold time are set in the Test Settings pane for the test.

Figure 45: CVU DC Sweep - Freq Step output
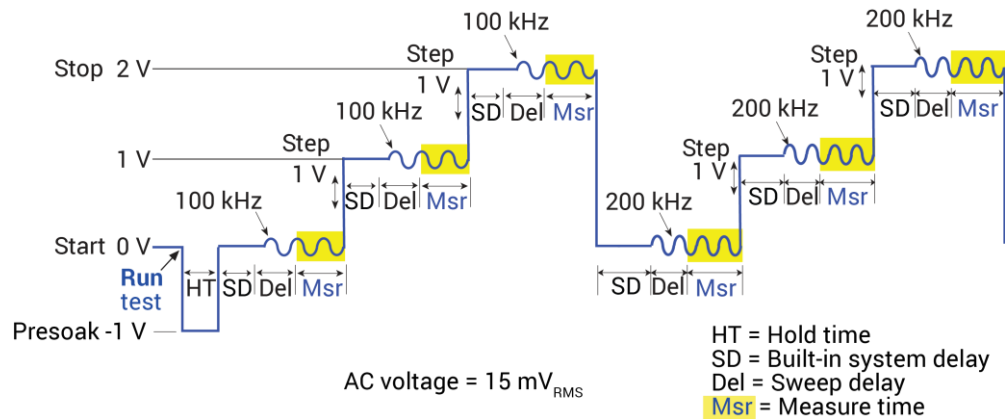
Force-measure timing

Timing diagrams for the force-measure process for bias and sweep functions are shown in the next two topics.

Bias function timing

You can apply dc voltage bias to the DUT (±30 V).

Timing for the force-measure process for a bias function is shown in the following figure. When the test is started, the following timing sequence takes place:

1. The dc source outputs the presoak voltage for the hold time.

2. The dc source goes to the dc bias voltage.

3. After the built-in system delay and time intervals, the CVU makes a measurement. The ac test signal is applied just before the start of the measurement. The ac drive is turned off after the measurement is completed. This step is repeated for every measurement.

Figure 46: Force-measure timing
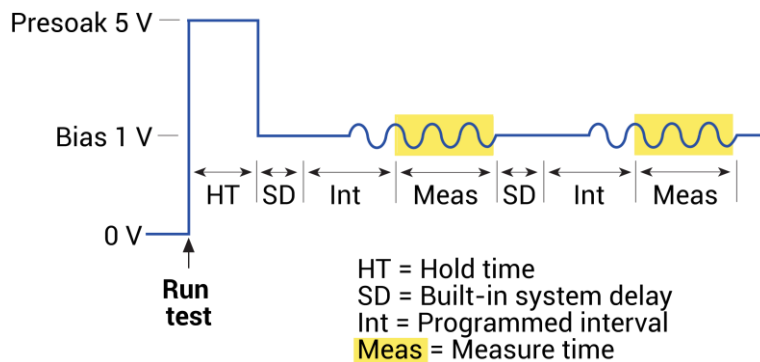
Sweep function timing

Force-measure timing for a sweep function is similar to the timing for a bias function (shown in Bias function timing (on page 3-22)), with the following differences:

- The hold time is repeated at the beginning of each subsequent sweep step.
- A sweep delay is used in place of the interval.

CVU - all terminal parameters

When you select **All Parameters**, the Configure pane displays all available parameters for the test that is selected in the project tree.

Parameter descriptions are provided in the following sections.

Presoak

Type a presoak voltage of −30 V to +30 V.

Start

The voltage source level at which the sweep starts.

Stop

The voltage source level at which the sweep stops.

Step (voltage sweep)

The voltage size of each step of the sweep. The source level changes in equal steps of this size from the start level to the stop level. A measurement is made at each source step (including the start and stop levels).

Clarius never steps the force voltage beyond the value specified by the stop parameter, even if you specify a step value that is larger than the stop value.

Use a step value that does not result in a fractional number of points. If the point is fractional, the step value is forced to a value that results in a whole number of points. To calculate the points:

$$points = \frac{(stop - start)}{step} + 1$$

The points are rounded to the nearest value.

For example, if Start = 0 V, Stop = 5 V, and Step = 0.6 V:

$$points = \frac{(5 - 0)}{0.6} + 1$$

In this case, the Step value is forced to 0.625 V, which results in a point value of 9.333, which is rounded to 9. The instrument forces nine voltages at 0 V, 0.625 V, 1.25 V, 1.875 V, 2.5 V, 3.125 V, 3.75 V, 4.375 V, and 5 V.

List Values

Select **Enter Values** to open a dialog box in which you can type the current or voltage level for each step of the sweep in the rows. You can type any valid instrument current or voltage.

You can select a value or multiple values in the list and copy, cut, or delete them. Use Paste to add values that you copied or cut to a new location in the list.

Note that you cannot have blank rows in between values.

You can use the Ctrl key plus mouse selections to pick selected rows, then use the buttons to copy, cut, or delete those rows. Note that when you paste the rows, any skipped rows are ignored (there will be no blank rows).

You can use the Shift key plus mouse selections to pick a range of rows. When you paste the rows, any blank rows are ignored.

Freq Operation Mode

The Frequency Operation Mode selects the most common settings for the selected test type. Selecting the appropriate mode simplifies terminal and test configuration.

If you have a 4210-CVU, you can select Single Freq, Freq Linear Sweep, or Freq Step. If you have a 4215-CVU, you can also select Freq Log Sweep or Freq List Sweep.

Start (Freq Operation Mode)

The frequency at which the sweep starts.

Stop (Freq Operation Mode)

The frequency at which the sweep stops.

Step (Freq Operation Mode)

The frequency size of each step of the sweep. The level changes in equal steps of this size from the start level to the stop level. A measurement is made at each step (including the start and stop levels).

Frequency Points (Freq Operation Mode)

The number of frequency points to sweep. This is calculated from the start and stop frequency values.

AC Drive Signal

You can set the ac drive signal to a value between 10 mV$_{RMS}$ and 1000 mV$_{RMS}$.

Points

The number of points that are measured. This value is calculated by Clarius using the information entered for the Start, Stop, and Step parameters, using the equation:

$$points = \frac{(stop - start)}{step} + 1$$

Points (list or segment sweep)

The number of sweep points that were defined in the List Values or Segments list. This number is automatically generated.

Dual Sweep

When you select Dual Sweep, the instrument sweeps from start to stop, then from stop to start. When you clear Dual Sweep, the instrument sweeps from start to stop only.

The following figure compares a single sweep to a dual sweep.

Figure 47: Single and dual sweep examples (linear voltage sweep; 0 V to 4 V in 1 V steps)
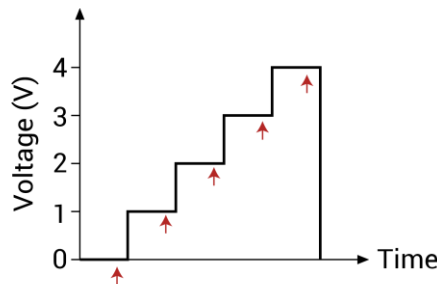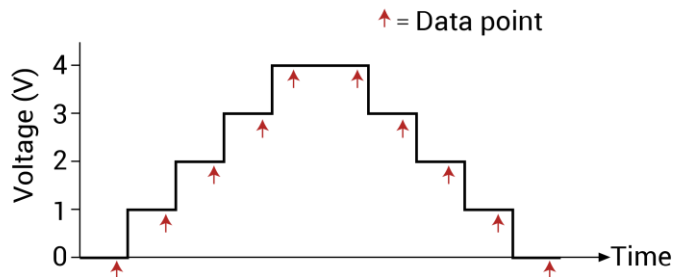
DC Bias

You can set a dc bias range from −30 V to 30 V.

Frequency

Set a frequency from 1E3 to 10E6 Hz.

For sweeps, the ac drive conditions include frequency (Hz) and voltage (mV$_{RMS}$). You can set frequency to the following values:

- 1 kHz through 10 kHz in 1 kHz steps

- 10 kHz to 90 kHz in 10 kHz steps

- 100 kHz to 900 kHz in 100 kHz steps

- 1 MHz to 10 MHz in 1 MHz steps

Parameters

CAUTION

If you change the Parameters, it will change the Column names, which can cause Formulator functions to be erased. When using any of the tests or libraries supplied by Keithley Instruments, leave the Parameters set to Cp-Gp.

The 4210-CVU or 4215-CVU can measure these parameters:

- **Z,Theta:** Impedance and phase angle (degrees)

- **R+jX:** Resistance and reactance

- **Cp-Gp:** Parallel capacitance and conductance

- **Cs-Rs:** Series capacitance and resistance

- **Cp-D:** Parallel capacitance and dissipation factor

- **Cs-D:** Series capacitance and dissipation factor

- **Y,Theta:** Admittance and phase angle (Y-theta)

The time domain of the ac current and ac voltage must be processed into the frequency domain to produce the phasor form of the DUT impedance.

The capacitive impedance and conductance are calculated based on the measured ac impedance and phase.

The following figure shows the vector diagram and fundamental equations for impedance.

Figure 48: Vector diagram for impedance (Z)
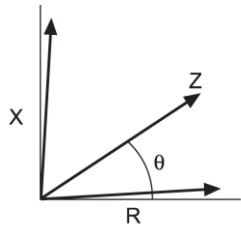
$$|Z| = \sqrt{R^2 + X^2} \qquad R = Z\cos\theta$$

$$Z = R + jX \qquad X = Z\sin\theta$$

$$\theta = \arctan\left(\frac{X}{R}\right) \qquad Y = \frac{1}{Z} = (G + jB)$$

Z = Impedance
θ = Phase angle
R = Resistance
X = Reactance
Y = Admittance
G = Conductance
B = Susceptance

The capacitance is calculated from the capacitive impedance and the test frequency using the formula:

$$C_{DUT} = \frac{I_{DUT}}{2\pi f V_{AC}}$$

Where:

- C_{DUT} = Capacitance of the DUT (F)
- I_{DUT} = Current of the DUT (A)
- f = Test frequency (Hz)
- V_{AC} = Measured AC voltage (V)

The inductance (L) can be calculated from the reactance (X) and test frequency (f):

$$L = \frac{X}{2\pi f}$$

Param1 Column Name

The name that is used for parameter 1 in the Analyze sheet.

If you do not define a name, Clarius assigns a name. The assigned name is a combination of the parameter name and the terminal label.

This cannot be left blank. If it is left blank, Clarius uses the previous value.

If you change the name, it is updated when the test is run. The results from earlier tests that are available through Run History are not changed to the new name.

Param2 Column Name

The name that is used for parameter 2 in the Analyze sheet.

If you do not define a name, Clarius assigns a name. The assigned name is a combination of the parameter name and the terminal label.

This cannot be left blank. If it is left blank, Clarius uses the previous value.

If you change the name, it is updated when the test is run. The results from earlier tests that are available through Run History are not changed to the new name.

Report Test Conditions

If you select Report Test Conditions, the dc bias voltage and drive frequency values that were used for the test are displayed on the Analyze sheet.

When this option is selected, column name fields are available. These are the names of the columns in the Analyze sheet where this data is reported. You can change the names of the columns by entering new values for DCV Column Name and Freq Column Name.

DCV Column Name

Available if you select Report Test Conditions. Determines the name of the column that contains the dc bias information in the Analyze sheet where this data is reported. You can change the name of the column by typing a new value.

This cannot be left blank. If it is left blank, Clarius uses the previous value.

If you change the name, it is updated when the test is run. The results from earlier tests that are available through Run History are not changed to the new name.

Freq Column Name

Available if you select Report Test Conditions. Determines the name of the column that contains the frequency information in the Analyze sheet where this data is reported. You can change the name of the column by typing a new value.

This cannot be left blank. If it is left blank, Clarius uses the previous value.

If you change the name, it is updated when the test is run. The results from earlier tests that are available through Run History are not changed to the new name.

Report Status (CVU)

When this option is selected, Clarius records measurement status information when the test executes. A column of the Analyze spreadsheet displays this information. Hover over a cell to review the information. An example of the status information is displayed in the following figure.

Figure 49: Report Status column for CVU in Analyze sheet

F_AB	CVU1S	NOISE
1.0000E+6	00000001	645.7550E-18
1.0000E+6	00000001	
1.0000E+6	Status: 30uA Range	
1.0000E+6	00000001	
1.0000E+6	00000001	

Open

Use the CVU connection compensation value that was generated for open connection compensation. Refer to Connection compensation (on page 2-8) for information on generating and using compensation values.

Short

Use the CVU connection compensation value that was generated for short connection compensation. Refer to Connection compensation (on page 2-8) for information on generating and using compensation values.

Load

Use the CVU connection compensation value that was generated for load compensation. Refer to Connection compensation (on page 2-8) for information on generating and using compensation values.

Cable Length

The cable length that was used to generate connection compensation data. Make sure this cable length is the same as the Cable Length setting in the Tools > CVU Connection Compensation dialog box. Refer to Connection compensation (on page 2-8) for additional information.

CVU Terminal Settings Advanced settings and circuits

You can apply ac drive voltage and dc bias voltage to either the CVH1 terminal or the CVL1 terminal. To change the options, select the **Terminals Settings** pane, then select **Advanced.**

By default, ac source voltage is applied to the CVH1 terminal and the current measurement is made at the CVL1 terminal. Also by default, the dc source voltage (bias) is applied to the CVL1 terminal. The settings and test circuits are shown in the following figures.

Figure 50: Test circuit with ac source and dc source applied to CVH1
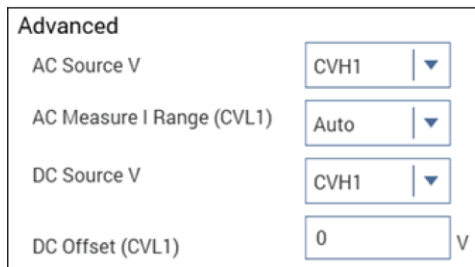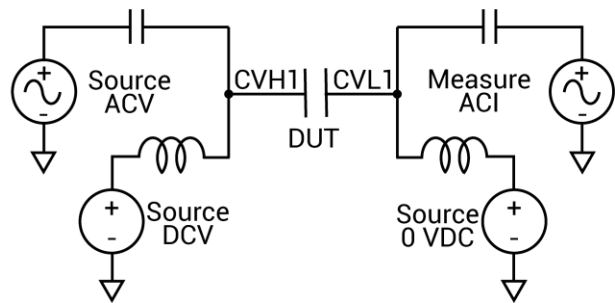
You can change the configuration to source ac voltage to CVL1 and dc source voltage to CVH1 while measuring ac current at CVH1, as shown in the following figure.

Figure 51: Test circuit with ac source applied to CVL1 and dc source applied to CVH1
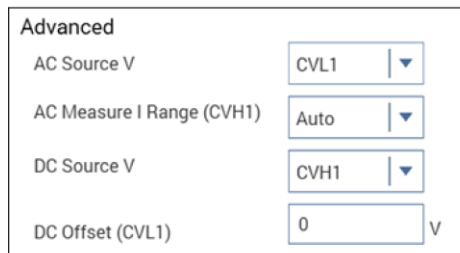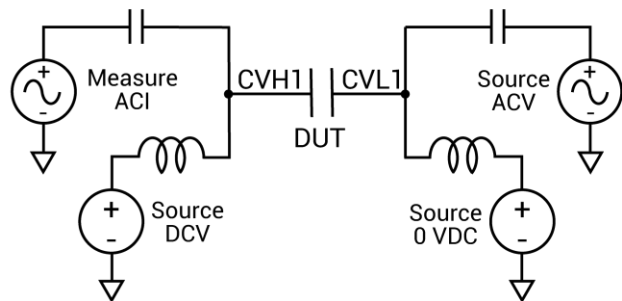
Another configuration sources ac drive voltage to the CVH1 terminal and sources dc bias voltage to the CVL1 terminal. The ac current is measured at CVL1.

Figure 52: Test circuit with ac voltage source applied to CVH1 and dc bias applied to CVL1
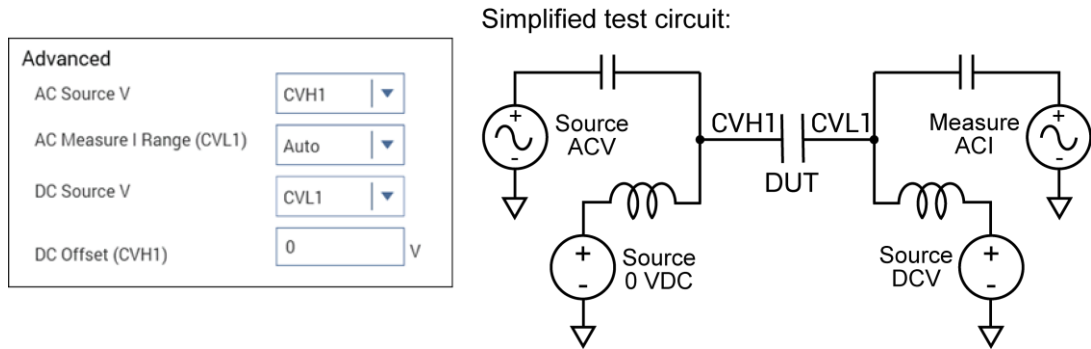
The following settings source ac drive voltage and dc bias voltage to the CVL1 terminal. The ac current is measured at CVH1.

Figure 53: Test circuit with ac voltage source and dc voltage bias applied to CVL1
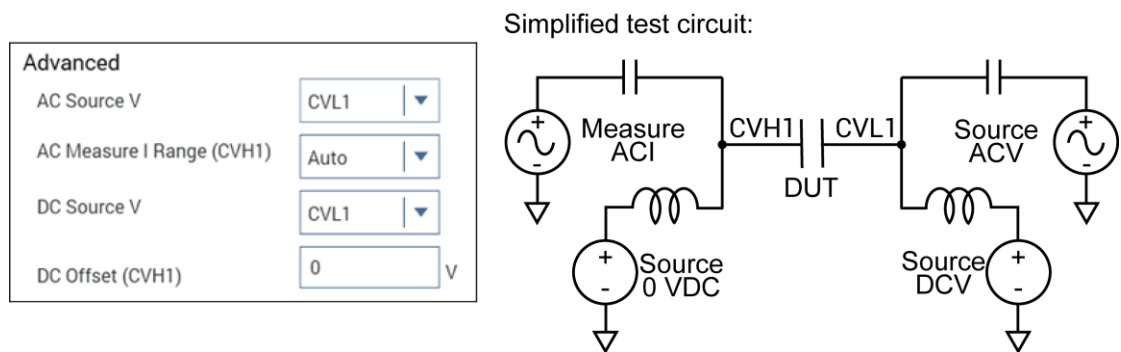
AC Source V

Selects the terminal to use to source ac drive voltage.

AC Measure I Range

The measure range determines the full-scale measurement span that is applied to the signal. Therefore, it affects both the accuracy of the measurements and the maximum signal that can be measured.

The current range options are:

- **Auto:** The instrument automatically optimizes the measurement range as the test progresses. This option provides the best resolution when the measurements span several decades. However, time delays can occur with range changes that can limit the measurement speed.

- **Specific ranges:** You can select a fixed measurement range.

DC Source V

Selects the terminal to use to source dc drive voltage.

DC Offset

Allows you to offset the voltage by up to ±30 V on one terminal. For example, this allows you to output voltage from 0 V to 60 V instead of −30 V to +30 V.

Capacitance Range Estimator

The measurement accuracy of the 4210-CVU or 4215-CVU is specified to 1 pF. However, the CVU can make much higher capacitance measurements. The maximum capacitance is based on the test frequency, ac drive signal, and range.

The Capacitance Range Estimator automatically calculates the maximum capacitance value based on the parameter settings. It shows the maximum capacitance values in the mF ranges. Note that capacitance values above 100 nF are not tested or calibrated.

In general, to measure high capacitances, use the lowest test frequency (1 kHz), the smallest ac drive voltage (10 mV$_{RMS}$), and the maximum current range (1 mA or autorange).

To use the Capacitance Range Estimator:

1. Select **Configure**.
2. In the Key Parameters pane, click the CVH1 terminal.
3. Select the **Terminal Settings** pane.
4. Select **Advanced**.
5. Change the parameters as needed to view the maximum capacitor value for those settings.

CVU test settings

The settings that are available for CVU tests are described in the following topics.

To access the Test Settings pane:

1. In the project tree, select the test.
2. Select **Configure**.
3. Select **Test Settings** in the right pane.
4. If needed, select **Advanced** to access additional settings.

CVU speed settings

To make successful C-V measurements, you must choose the appropriate speed settings. Adjustments to the speed settings can help prevent noisy measurements and allow you to acquire readings in equilibrium.

The Speed settings allow you to select trade-offs between speed and noise. You can select:

- **Fast:** Optimizes the CVU for speed at the expense of noise performance. It is a good choice for measurements where noise and settling time are not concerns.
- **Normal:** The default and most commonly used setting. It provides a balanced combination of speed and low noise and is the best setting for most cases.
- **Quiet:** Optimizes the CVU for low-noise measurements at the expense of speed. If speed is not a critical consideration, it is a good choice when you need the lowest noise and most accurate measurements.
- **Custom:** While Fast, Normal, or Quiet should be appropriate for most applications, Custom allows you to fine-tune the timing parameters if needed.

Considerations when making Custom speed settings

You can optimize your measurements by adjusting the custom speed settings. With Custom, you can configure the A/D aperture time and individual delay and filtering factors to produce a composite setting that is faster than the Fast setting, quieter than the Quiet setting, or anything in between.

If you select Custom speed, you can fine-tune the speed using the Delay Factor, Filter Type, Filter Factor, and the Auto A/D Aperture or A/D Aperture Time.

Each measured reading by a CVU is the result of one or more analog to digital (A/D) conversions. Reducing the aperture time for each A/D conversion results in a relatively fast measurement speed with increased noise. Increasing the A/D Aperture reduces noisy readings.

You can set the Filter Type to Point Averaging or Noise Reduction Factor. When Point Averaging is selected, you select the Filter Count to determine how many points are averaged. The value for Filter Count is multiplied by the A/D Aperture Time to determine the measurement window.

When Noise Reduction Factor is selected, the measurement window is determined by the formula:

$$Measurement\ Window = A/D\ Aperture\ Time \times (Filter\ Factor)^2$$

An overview of the effects you may want and the types of adjustments you can make to achieve them are provided in the following table. Additional detail on each setting is provided after the table.

Effect	Adjustments
Reduce noise	■ Increase Filter Factor ■ Increase the A/D aperture time ■ Use Quiet mode
Increase measurement speed	■ Use a fixed measurement range ■ Reduce Filter Factor ■ Reduce A/D aperture time ■ Reduce the Delay Factor
Increase settling time (often needed for long cables or switch matrices)	■ Increase the Delay Factor ■ Use sweep delay and hold times to charge up the device to equilibrium; refer to Selecting the DC Operation Mode (on page 3-5) for more information on working with sweeps
Get more consistent time intervals between measurements	■ Used a fixed measurement range ■ Specify the A/D aperture time ■ Set Filter Factor and Delay Factor to zero

Delay Factor

The Delay Factor adjusts the delay time for the selected speed. In some cases, you may need an additional delay before making a measurement to allow for range changes and to accommodate the number of points, especially for dc bias. The Delay Factor is a multiple of the default delay time:

Applied delay time = (Default delay time) x (Delay Factor)

For example, if the default delay time is 1 ms and the Delay Factor is 0.7, the actual applied delay time is 0.7 ms (1 ms x 0.7).

The following table shows the default Delay Factor settings for Fast, Normal, and Quiet, and the range of values available when Custom is selected.

Speed Mode	Delay Factor
Fast	0.7
Normal	1.0
Quiet	1.3
Custom	0 to 100

When typing a custom Delay Factor setting, consider the following:

- A Delay Factor of 1 allows for settling before the A/D converter is triggered to make a measurement.

- Each doubling of the Delay Factor doubles the time allowed for settling.

- A delay factor of 0 multiplies the default delay by zero, resulting in no additional delay. However, instrument processing time may cause some small delay.

NOTE

If you set the Filter Factor and Delay Factor to `0`, the internal pre-programmed values are ignored.

In general, cables and matrices increase the settling time. You may need to experiment to find the ideal time. However, for a good quality switch, such as the Keithley Instruments 7174A Ultra-Low Current matrix, you should not need to increase the Delay Factor by more than two times.

Filter Type

You can set the Filter Type to Point Averaging or Noise Reduction Factor.

When Point Averaging is selected, you select the Filter Count to determine how many points are averaged. The value for Filter Count is multiplied by the A/D Aperture Time to determine the measurement window.

When Noise Reduction Factor is selected, the measurement window is determined by the formula:

Measurement Window = A/D Aperture Time x (Filter Factor)^2

Filter Count

When the Filter Type is set to Point Averaging, the Filter Count determines how many points are averaged. The value for Filter Count is multiplied by the A/D Aperture Time to determine the measurement window.

Filter Factor

The Filter Factor adjusts how many readings are averaged before a measurement is recorded. In some cases, you may need adjust the default filtering.

The following table shows the default Filter Factor settings for Fast, Normal, and Quiet, and the range of values available when Custom is selected.

Speed Mode	Filter Factor
Fast	1
Normal	1
Quiet	1
Custom	1 to 707

When typing a custom Filter Factor, consider the following:

- A Filter Factor of 1 provides filtering that appropriate for most applications.

- Increase the Filter Factor to average multiple readings to reduce noise. As a rule of thumb, doubling the Filter Factor halves the measurement noise.

- Measurement time is increased by the square of the filter factor.

NOTE

When the Delay Factor is set to zero, the internal pre-programmed values are ignored.

Auto A/D Aperture

When Auto A/D Aperture is selected, the instrument picks the optimum A/D conversion time for most normal measurements.

A/D Aperture Time

If you do not achieve enough noise reduction through adjustments to the Delay and Filter Factors, you can adjust the A/D converter aperture time.

The A/D converter aperture time is the integration time that is used to measure a signal. Decreasing the aperture time for each A/D conversion results in a relatively fast measurement speed with increased noise. Increasing the aperture time results in a relatively low measurement speed with relatively low noise.

The CVU applies an optimum A/D converter time that is based on the Filter Type setting. When Filter Type is set to Point Averaging, you select the Filter Count to determine how many points are averaged. The value for Filter Count is multiplied by the A/D Aperture Time to determine the measurement window.

When the Filter Type is set to Noise Reduction Factor is selected, you also enter a Filter Factor, and the measurement window is determined by the formula:

Measurement Window = A/D Aperture Time x (Filter Factor)^2

The applied A/D converter time value is never less than the specified A/D Aperture Time.

The following table shows the default A/D Aperture Time settings for Fast, Normal, and Quiet, and the range of values available when Custom is selected.

Speed Mode	A/D Aperture Time (seconds)
Fast	0.001
Normal	0.01
Quiet	0.1
Custom	0.0001 to 10.002

To adjust the aperture time, you must set Speed to **Custom** and clear **Auto A/D Aperture**.

Report Timestamps

When this option is selected, every measurement in the Analyze sheet includes a timestamp. When this option is cleared, the timestamp is not included.

The timestamp records the elapsed time for each measurement. Each elapsed time value is placed in the Analyze sheet in the same row as the measurement.

Each elapsed time is measured relative to the beginning of the test when voltage or current is first applied to the device. If Clarius requires only one reading for each measurement, Clarius records the timestamp at the beginning of this reading, as shown in the following figure.

Figure 54: Timestamps when Clarius requires only one reading for a measurement
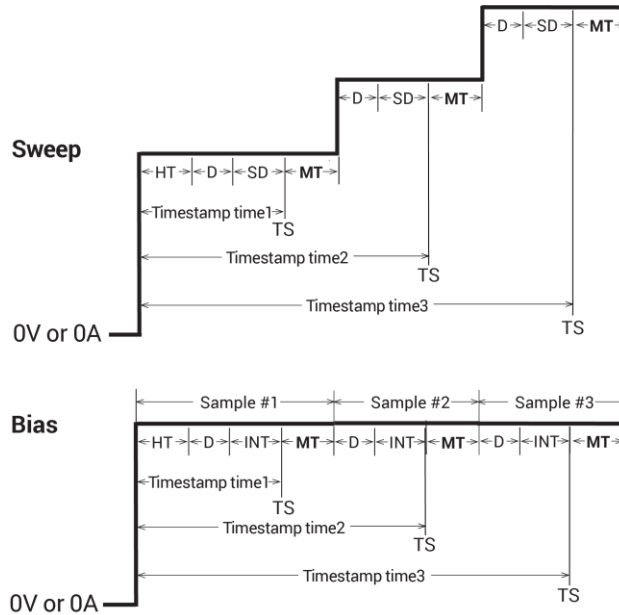
TS = Timestamp at the start of the reading when one reading is made
HT = Hold Time - applies presoak voltage
D   = Delay (default delay x delay factor)
SD = Sweep Delay
INT = Interval
MT = Measure Time

If Clarius makes and averages multiple readings for a measurement, then Clarius records the timestamp at the last of these readings, as shown in the following figure.

Figure 55: Timestamps when Clarius requires multiple readings for a measurement
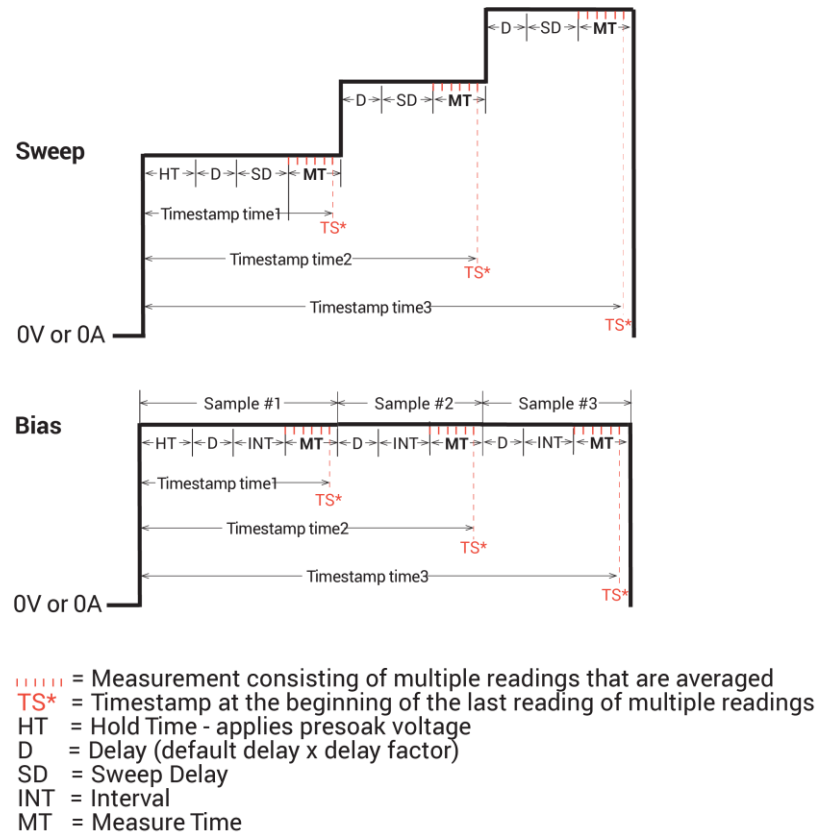
You can enable the timestamp for any of the measurement speeds**.**

Test Mode

You can set a test to the sweeping or sampling test mode.

Sweeping test mode is used for tests in which the voltage or frequency varies with time.

Sampling Mode allows you to measure capacitance or currents as a function of time while forcing constant voltages. The sampling test mode is used for tests in which the forced voltage and frequency are static, with measurements made at timed intervals. For example, you could use sampling mode to profile a capacitor charging voltage while forcing a constant current. Time is measured relative to when the instruments apply the forced voltage.

When Sampling Mode is selected, all device terminals are set to a static operation mode, such as Open or Voltage Bias.

Refer to Typical test setups with timing diagrams (on page 3-9) for additional detail.

Sweep Delay

If you are using a sweep operation mode and need extra settling time before each measurement, you can specify an additional delay with the Sweep Delay. The Sweep Delay is independent of the Delay Factor (on page 3-34). You can specify a Sweep Delay from 0 s to 999 s. The default Sweep Delay is 0 s.

Interval

Sampling mode only. The time between measurements (points). Interval can be set from 0 s to 1000 s.

Number of Samples

Sampling mode only. Specifies the number of points to be acquired. Set the number of samples to a value from 1 to 4096.

Hold Time

The starting voltages of a sweep may be substantially larger than the voltage increments of the sweep. Accordingly, the source settling time required to reach the starting voltages of a sweep may be substantially larger than the settling times required to increment the sweep. To compensate, you can specify a Hold Time delay to be applied at the beginning of each sweep. You can specify a Hold Time of 0 to 1000 s.

The presoak voltage set in the Terminal Settings pane are applied for the specified hold time.

Choose hold and sweep delay times for CVUs

The condition of a device when all internal capacitances are fully charged after an applied step voltage is referred to as equilibrium.

If capacitance measurements are made before the device is in equilibrium, you may get inaccurate results.

To choose the hold times for a C-V sweep:

1. Set up conditions of:
    - Hold time: 0 s
    - Interval time: 0 s
    - Presoak: 0 V
2. Step an applied voltage using the sampling mode.
3. Plot the capacitance as a function of time.
4. Observe the settling time from the graph.
5. Use this time for the hold time for the initial applied voltage or for the sweep delay time applied at each step in the sweep. The sweep delay time may not need to be as long as the first step.

Disable outputs at completion - CVU

When a test is complete, you can disable the outputs or leave them enabled.

When Disable Outputs at Completion is selected, the output turns off (0 V) when the test is complete. If this option is not selected, the dc Bias voltage remains at the last bias voltage level at the end of the previous test.

Output Values

If you are using subsites, each time a subsite is cycled, the measurements for the enabled Output Values are placed in the Analyze sheet for the subsite. For example, if the subsite is cycled five times, there are five measured readings (Output Values) for the test. For details, see "Cycle a subsite" in the *Model 4200A-SCS Clarius User's Manual*.

To select output values:

1. In the project tree, select the test.
2. Select **Configure**.
3. In the right pane, select **Test Settings**.
4. Select **Output Values**. The Output Values dialog box is displayed.
5. Select the data series that you want to send to the Analyze sheet.
6. Select **OK**.

Figure 56: Select Output Values
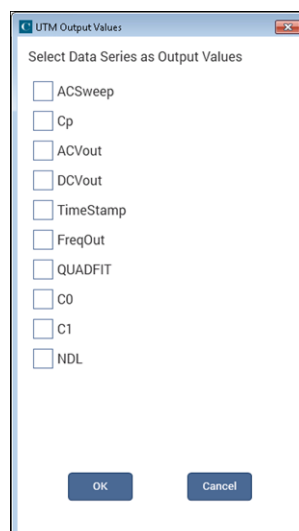
C-V projects

In this section:

C-V projects

A project contains tests for a testing application. The projects that support CVU testing are summarized in the following table.

CVU projects

Projects	Description
cvu-bjt (on page 4-3)	Measures capacitance (0 V bias) between two terminals of a bipolar junction transistor (BJT): CCB, CCE, and CBE.
cvu-bjt-cviv (on page 4-7)	This project has test modules that measure the capacitance as a function of time at 0 V between the terminals of a BJT: collector-base, collector-emitter, and base-emitter. You can measure this capacitance at 0 V or as a function of an applied voltage. The 4200A-CVIV switches the CVU to the BJT terminals.
cap-iv-cv-matrix (on page 4-8)	Combines a 4200-SMU or 4201-SMU, CVU, and matrix switching in one project. Closes switches on the matrix card to connect the SMUs to a device to measure I-V on a capacitor. Then it opens and closes another set of switches to make C-V measurements on a capacitor.

CVU projects

Projects	Description
cap-measurements (on page 4-13)	Performs both a C-V sweep and a C-f sweep on a metal-insulator-metal (MIM) capacitor. Standard deviation is calculated.
cntfet-characterization (on page 4-14)	This project contains dc I-V, pulsed I-V, and C-V tests for a carbon nanotube FET (CNTFET).
default (on page 4-15)	Summarizes the C-V tests that have been added to the default project. C-V testing for an n-MOSFET, diode, and a capacitor.
diode (on page 4-16)	This project contains dc I-V, C-V, and pulse I-V tests for a PN junction. Measures the capacitance of a PN junction or Schottky diode as a function of the dc bias voltage across the device. Has tests that include a basic C-V sweep, $1/C^2$ versus V, and a doping profile.
`femtofarad-capacitance`	Uses the 4215-CVU to measure the capacitance of a PN junction or Schottky diode as a function of the dc bias voltage across the device. Has tests that include a basic C-V sweep, $1/C^2$ versus V, and a doping profile.
cvu-highv (on page 4-21)	Contains tests for making high-voltage C-V measurements on a Zener diode, MOS capacitor, capacitor, and a Schottky diode.
cviv-bias-highv (on page 4-22)	Contains tests for making high-voltage C-V measurements on a Zener diode, MOS capacitor, capacitor, and a Schottky diode. These tests use the 4200A-CVIV bias tees to combine signals from a CVU and a SMU. The CVU measures the capacitance and the SMU supplies the dc bias.
cvu-moscap (on page 4-23)	Measures C-V on a MOS capacitor and extract parameters, including oxide capacitance, oxide thickness, doping density, depletion depth, debye length, flatband capacitance, flatband voltage, bulk potential, threshold voltage, metal-semiconductor work function difference, and effective oxide charge.
moscap-lifetime (on page 4-45)	Determines generation velocity and lifetime testing (Zerbst plot) of MOS capacitors. Performs both C-V and C-t sweeps and then generates a Zerbst plot, which is the generation rate plotted as a function of depletion depth.
moscap-mobile-ion (on page 4-53)	Determines mobile charge using bias-temperature stress method. Makes C-V measurements on a device at room temperature, and then repeats the C-V measurements for a hot chuck. The mobile charge is determined from the flatband shift.
mosfet-cviv-cv-bias-tees-400V (on page 4-61)	Contains test modules that perform high-voltage CV measurements in the off-state on a 3-terminal, n-channel MOSFET. This is a 400 V version of mosfet-cviv-cv-bias-tees.
mosfet-cviv-cv-bias-tees (on page 4-61)	This project contains test modules that perform high-voltage CV measurements in the off-state on a 3-terminal, n-channel MOSFET.
mosfet-cviv (on page 4-61)	Demonstrates how you can use a 4200A-CVIV Multi-Switch to automate I-V and C-V testing of a MOSFET. When the project is run, the 4200A-CVIV connects four SMUs to the MOSFET. The SMUs perform I-V tests on the MOSFET. The 4200A-CVIV then connects the CVU to the MOSFET. The CVU measures the gate to drain/source/bulk capacitance as a function of the dc voltage.
mosfet (on page 4-61)	Performs a two-terminal C-V sweep on a MOSFET device, and calculates oxide thickness, oxide capacitance, flatband capacitance, and flatband voltage. There is also a test that calculates and plots the doping concentration as a function of depletion depth.
`ofet`	Measures the capacitance of a PN junction or Schottky diode as a function of the dc bias voltage across the device. Has tests that include a basic C-V sweep, 1/C2 versus V, and a doping profile.

CVU projects

Projects	Description
solarcell (on page 4-69)	Measures both I-V and C-V. A SMU is used to measure the forward-biased characteristics of an illuminated solar cell and extract parameters (such as maximum power, maximum current, maximum voltage, short-circuit current, open-circuit voltage, and efficiency). The SMU also makes a reverse biased I-V measurement and performs C-V and C-f sweeps.
interconnect-cvsweep	Summarizes the C-V tests that have been added to the default project. C-V testing for an n-MOSFET, diode, and a capacitor.
Nanowire tests (on page 4-78)	These tests perform C-V sweeps on a two-terminal nanowire device. The tests are similar but use different drive frequencies. The tests generate capacitance versus voltage graphs.

BJT Capacitance Tests (cvu-bjt)

The internal capacitance measurements on bipolar junction transistors (BJTs) can affect the gain and frequency response of devices. This project includes test modules that measure the capacitance as a function of time at 0 V between the terminals of a BJT. Measurements are made between the collector-base, collector-emitter, and base-emitter. You can measure capacitance at 0 V or as a function of an applied voltage that you specify.

This project includes the following tests:

- c-cb0: Measures the capacitance as a function of time between the collector and base.

- c-ce0: Measures the capacitance as a function of time between the collector and emitter.

- c-be0: Measures the capacitance as a function of time between the base and emitter.

cvu-bjt connections

The next figures show the basic test configurations. Note that the untested terminal must be connected to the outer shield of the SMA cables to guard unwanted capacitance from affecting measurement accuracy. For example, when measuring the collector-base capacitance (c-cb0), the emitter terminal is guarded by connecting it to the outer shield of the SMA cables.

Refer to Typical CVU test connections to a DUT (on page 2-3) for connection details. Use only the supplied (red) 100 Ω SMA cables for connections to the 4210-CVU or 4215-CVU. Be sure that all SMA cables are the same length (1.5 m or 3 m).

NOTE

After making or changing connections, be sure to use the CVU Confidence Check diagnostic tool and do connection compensation tests. Refer to Run an open check and short check (on page 2-17) and Connection compensation (on page 2-8) for details.

Figure 57: Basic configurations for BJT c-cb0 test

c-cb0 connections
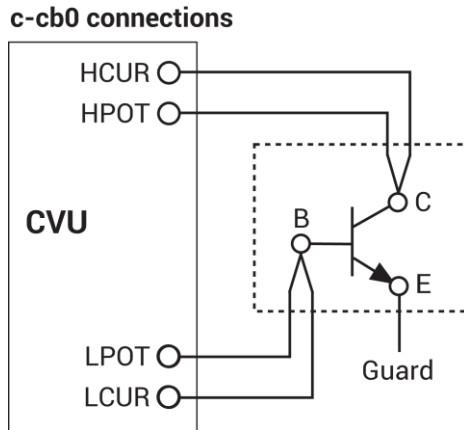
Figure 58: Basic configurations for BJT c-ce0 test

c-ce0 connections
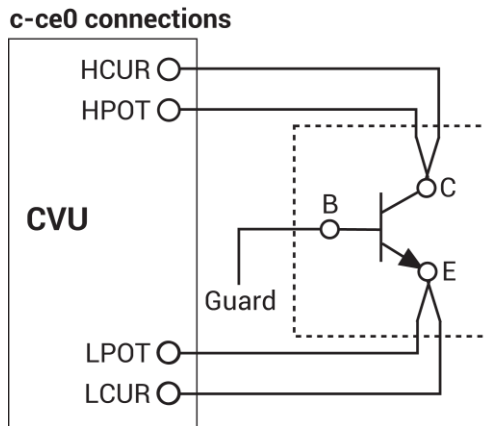
Figure 59: Basic configurations for BJT c-be0 test
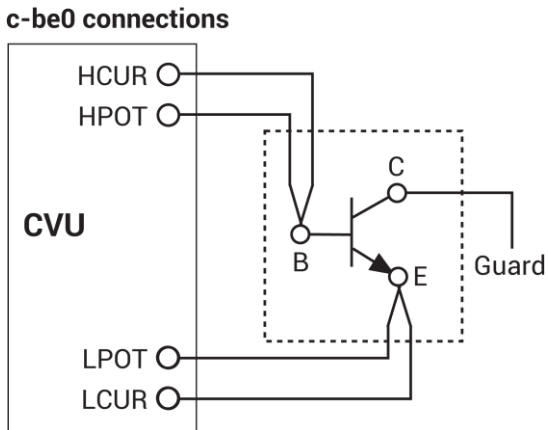
c-be0 connections

Formulas and constants

This project uses two formulas with no constants:

- AVG_CAP: Calculates the average capacitance in farads (F). The formula is:
  AVG_CAP = AVG(CP_AB)

- STD_DEV: Calculates the standard deviation of the capacitance measurements. The formula is:
  STD_DEV = STDEV(CP_AB)

c-cb0 test

This test measures the capacitance as a function of time between the collector and base terminals of a BJT at 0 V. The results (C versus t) are then plotted on a graph. This test also calculates the average capacitance and standard deviation.

Analyze sheet

Test data is displayed in the Analyze sheet:

- Time: Measured parallel capacitance.

- Cp_CB: Measured parallel capacitance.

- Gp_CB: Measure conductance.

- DCV_CB: Forced dc bias voltage.

- F_CB: Forced test frequency.

- CVU1S: Status code for each measurement. Rows highlighted in blue indicate a fault. For details, refer to "Measurement status" in the *Model 4200A-SCS Clarius User's Manual*.

- AVG_CAP: Calculated; the average capacitance in farads (F).

- STD_DEV: Calculated; the standard deviation of the capacitance measurements.

c-ce0 test

This test measures the capacitance as a function of time between the collector and emitter terminals of a BJT at 0 V. The results (C versus t) are plotted on a graph. This test also calculates the average capacitance and standard deviation.

Analyze sheet

Test data is displayed in the Analyze sheet:

- Time: Timestamp for each measurement.
- Cp_CE: Measured parallel capacitance.
- Gp_CE: Measured conductance.
- DCV_CE: Forced dc bias voltage.
- F_CE: Forced test frequency.
- CVU1S: Status code for each measurement. Rows highlighted in blue indicate a fault. For details, refer to "Measurement status" in the *Model 4200A-SCS Clarius User's Manual*.
- STD_DEV: Calculated value; the standard deviation of the capacitance measurements.
- AVG_CAP: Calculated value; the average capacitance in farads (F).

c-be0 test

This test measures the capacitance as a function of time between the base and emitter terminals of a BJT at 0 V. The results (C versus t) are plotted on a graph. This test also calculates the average capacitance and standard deviation.

Analyze sheet

Test data is displayed in the Analyze sheet:

- Time: Timestamp for each measurement.
- Cp_BE: Measured parallel capacitance.
- Gp_BE: Measured conductance.
- DCV_BE: Forced dc bias voltage.
- F_BE: Forced test frequency.
- CVU1S: Status code for each measurement. Rows highlighted in blue indicate a fault. For details, refer to "Measurement status" in the *Model 4200A-SCS Clarius User's Manual*.
- AVG_CAP: Calculated value; the average capacitance in farads (F).
- STD_DEV: Calculated value; the standard deviation of the capacitance measurements.

BJT I-V and C-V Tests Using 4200A-CVIV Multi-Switch Project (cvu-bjt-cviv)

This project has test modules that measure the capacitance as a function of time at 0 V between the terminals of a BJT: collector-base, collector-emitter, and base-emitter. You can measure this capacitance at 0 V or as a function of an applied voltage. The 4200A-CVIV switches the CVU to the BJT terminals.

This project includes several actions that perform CVU connection compensation through the 4200A-CVIV Multi-Switch using a user-defined configuration. They are:

- CVU Connection Compensation Using 4200A-CVIV (`cvu-cviv-comp-collect-cb`)

- CVU Connection Compensation Using 4200A-CVIV (`cvu-cviv-comp-collect-ce`)

- CVU Connection Compensation Using 4200A-CVIV (`cvu-cviv-comp-collect-be`)

The project also contains the following actions and tests:

- 4200A-CVIV Configure (`cviv-configure-collector-base`): Uses the 4200A-CVIV Multi-Switch to connect SMUs and the CVU to a device.

- BJT Capacitance collector-base (`c-cb0`): This test measures the capacitance as a function of time between the collector and base terminals of a BJT at 0 V. The results (C versus t) are then plotted on a graph. This test also calculates the average capacitance and standard deviation.

- 4200A-CVIV Configure (`cviv-configure-collector-emitter`): This action uses the 4200A-CVIV Multi-Switch to connect SMUs and the CVU to a device.

- BJT Capacitance collector-emitter (`c-ce0`): This test measures the capacitance as a function of time between the collector and emitter terminals of a BJT at 0 V. The results (C versus t) are plotted on a graph. This test also calculates the average capacitance and standard deviation.

- 4200A-CVIV Configure (`cviv-configure-base-emitter`): This action uses the 4200A-CVIV Multi-Switch to connect SMUs and the CVU to a device.

- BJT Capacitance base-emitter (`c-be0`): This test measures the capacitance as a function of time between the base and emitter terminals of a BJT at 0 V. The results (C versus t) are plotted on a graph. This test also calculates the average capacitance and standard deviation.

For additional information on using the 4200A-CVIV, refer to *Application Note: Making C-V and I-V Measurements Using the 4200A-CVIV Multi-Switch and 4200A-SCS Parameter Analyzer*.

Capacitor I-V and C-V Measurements with Series 700 Project (cap-iv-cv-matrix)

This project demonstrates how to use a Series 700 Switching System to automate I-V and C-V testing of a capacitor. When you run the project, the switching matrix connects two 4200-SMUs or 4201-SMUs to the capacitor and I-V measurements are made. Connections are shown in the following figure.

Figure 60: Switching matrix signal path for I-V testing
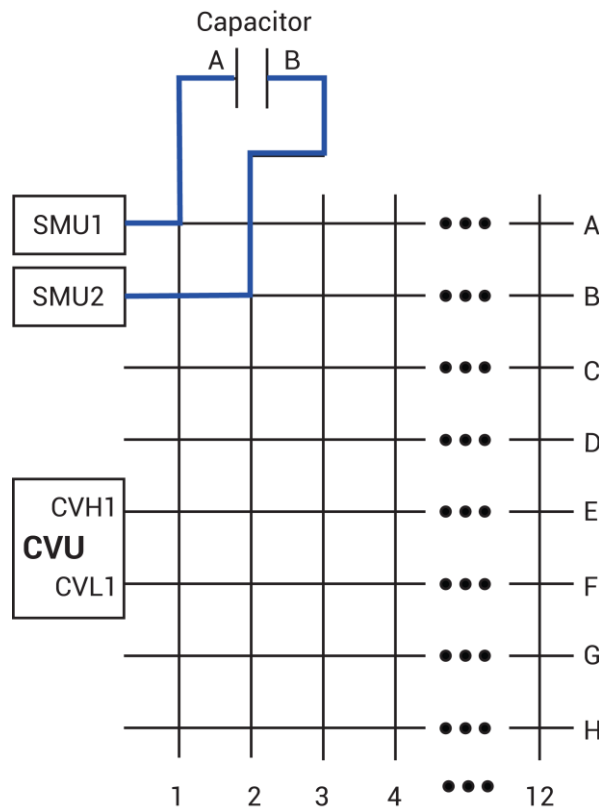
The switching matrix then connects the 4210-CVU or 4215-CVU to the capacitor and C-V measurements are made. Connections are shown in the following figure.

Figure 61: Switching matrix signal path for C-V testing
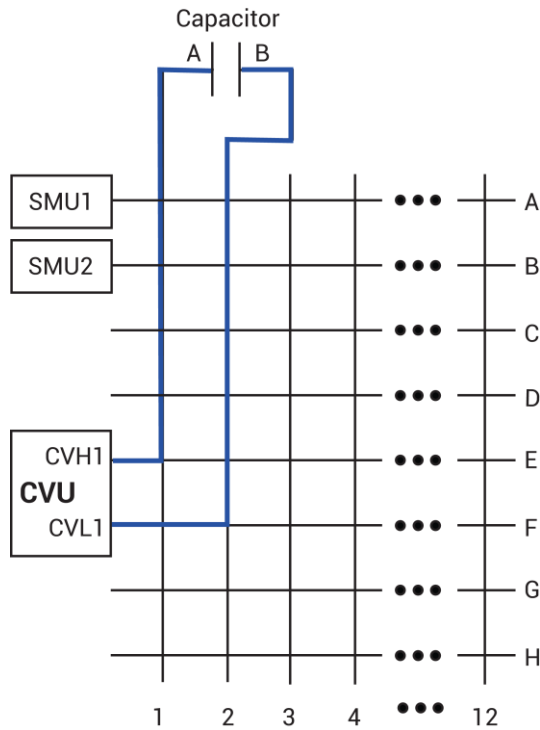
This project is set up for use with a Series 700 with a 7174A matrix card. You must configure the switching system and the matrix card in KCon (see "Add an external instrument" in *Model 4200A-SCS Setup and Maintenance*). Make sure sensing is set to Local (2-wire).

NOTE

You can also use the 7072 matrix card for this project. However, you must use Rows G and H with the 7072.

cap-iv-cv-matrix project summary

This project tests a capacitor by measuring leakage current (using a 4200-SMU or 4201-SMU) and capacitance (using 4210-CVU or 4215-CVU). These tests generate graphs for current versus time and capacitance versus time. The testing sequence is:

1. All switches for the matrix are opened.

2. Switches for the matrix card are closed to connect the SMUs to a capacitor. The SMU sources a fixed bias voltage to charge the capacitor, and measures leakage current as a function of time.

3. Switches are opened to disconnect the SMUs, and then closed to connect the CVU to the capacitor.

4. The CVU sources a fixed bias voltage to the capacitor and measures capacitance as a function of time. The average capacitance and standard deviation are calculated and displayed on the C-t graph.

cap-iv-cv-matrix connections

The following figure shows the basic test configuration. Details on CVU connections are provided in CVU connections (on page 2-1). For details on SMU connections, refer to "Connections and configuration" in the *Model 4200A-SCS Source-Measure Unit (SMU) User's Manual.* For details on CVU connections to the matrix card, refer to Test connections for a switch matrix (on page 2-5).

Use only the supplied (red) 100 Ω SMA cables for connections from the matrix card (rows E and F) to the CVU. Be sure that all used SMA cables are the same length.

Use triaxial cables to connect the matrix cards (columns 1 and 2) to the capacitor or prober card.

Use the supplied triaxial cables to connect the SMUs to the matrix card (rows A and B).

NOTE

After making or changing connections, be sure to use the CVU Confidence Check diagnostic tool and do connection compensation tests. Refer to Run an open check and short check (on page 2-17) and Connection compensation (on page 2-8) for details.

Figure 62: Simplified configuration to use a switching matrix for I-V and C-V testing
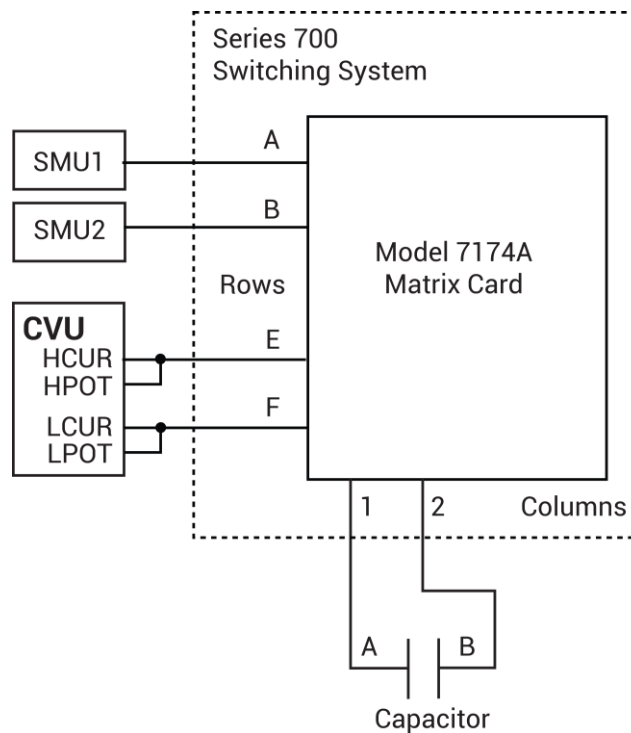
Formulas and constants

This project uses two formulas with no constants:

- AVG_CAP: Calculates the average capacitance in farads (F).
  AVG_CAP = AVG(CP_AB)

- STD_DEV: Calculates the standard deviation of the capacitance measurements.
  STD_DEV = STDEV(CP_AB)

connect test

The `connect` test controls the matrix card switches. It connects the SMUs to the capacitor.

The Configure settings are:

- The OpenAll parameter is selected. This opens all matrix switches at the beginning of the test sequence.

- The SMU1 parameter is set for pin 1. This connects SMU1 to column 1 of the matrix card. As shown in <u>cap-iv-cv-matrix connections</u> (on page 4-10), column 1 is connected to terminal A of the capacitor.

- The SMU2 parameter is set for pin 2. This connects SMU2 to column 2 of the matrix card. Column 2 is connected to terminal B of the capacitor.

- All the other instrument parameters are set for 0 (not used).

iv-cap test

In this test, SMU1 sources a fixed dc bias voltage to charge the capacitor and measures leakage current as a function of time.

Force, measure, and timing settings

The parameter settings for the two SMUs are:

- SMU1 is configured to bias 5 V.

- SMU2 is configured as a Common for the return signal path.

The test is set to perform 60 current measurements at 100 ms intervals

In the project tree, select `iv-cap` and then select Configure. From the Configure pane, parameters are set in the Test Settings pane and the Terminal Settings pane.

Analyze sheet

The test data is displayed in the Analyze sheet:

- Time: Timestamp of the measurement.

- AI: Measured current.

connect-cv test

This test controls the matrix card switches. It is used to disconnect the SMUs and then connect the 4210-CVU or 4215-CVU to a capacitor.

Configure settings are:

- The OpenAll parameter is selected. This opens all switches after the `iv-cap` test is finished.

- The CVH1 parameter is set for pin 1. This connects CVH1 to column 1 of the matrix card. Column 1 is connected to terminal A of the capacitor.

- The CVL1 parameter is set for pin 2. This connects CVL1 to column 2 of the matrix card. Column 2 is connected to terminal B of the capacitor.

- All the other instrument parameters are set to 0 (not used).

cv-capacitor test

This test applies a dc bias voltage to a capacitor and measures capacitance as a function of time. It generates a capacitance versus time graph and calculates average capacitance and standard deviation.

Analyze sheet

The test data is displayed in the Analyze sheet:

- Time: Timestamp for each measurement.

- Cp_AB: Measured parallel capacitance.

- Gp_AB: Measured conductance.

- DCV_AB: Forced dc bias voltage.

- F_AB: Forced test frequency.

- CVU1S: Status code for each measurement. For details, refer to "Measurement status" in the *Model 4200A-SCS Clarius User's Manual.*

- AVG_CAP: Formulator calculation result.

- STD_DEV: Formulator calculation result.

NOTE

AB = Terminal A to Terminal B.

Capacitor Measurements (cap-measurements)

This project performs a capacitance-voltage (C-V) sweep and a capacitance-frequency (C-f) sweep on a metal-insulator-metal (MIM) capacitor (10 pF). The following graphs are generated:

- C versus V: Using a voltage sweep, capacitance is measured at every step of the sweep to generate a capacitance versus voltage graph. Noise is also calculated.

- C versus F: Using a frequency sweep, capacitance is measured at every frequency point to generate a capacitance versus frequency graph.

cvu-capacitor connections

The test configuration is shown in the following figure. Use only the supplied (red) 100 Ω SMA cables for connections to the 4210-CVU or 4215-CVU. Be sure that all SMA cables are the same length.

NOTE

After making or changing connections, be sure to use the CVU Confidence Check diagnostic tool and do connection compensation tests. Refer to Run an open check and short check (on page 2-17) and Connection compensation (on page 2-8) for details.

Figure 63: Basic configuration to test a MIM capacitor
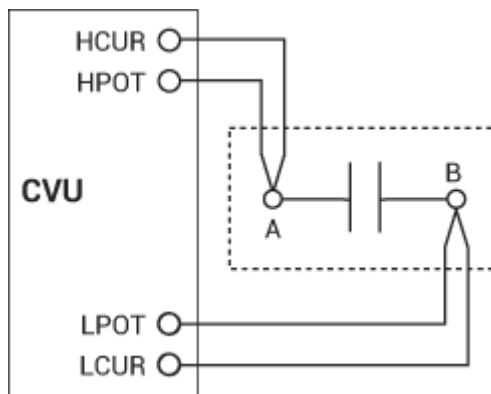
Formulas and constants

This project uses one formula with no constants.

- NOISE: Calculates the standard deviation of the capacitance measurements:
  NOISE = STDEV(CP_AB)

cv-10 pF test

This test performs a voltage sweep that measures capacitance on each step and generates a C versus V graph. It also calculates noise.

Analyze sheet

Test data is displayed in the Analyze sheet:

Cp_AB	Measured parallel capacitance.
Gp_AB	Measured conductance.
DCV_AB	Forced dc bias voltage.
F_AB	Forced test frequency.
CVU1S	Status code for each measurement. Rows highlighted in blue indicate a fault. For details, refer to "Measurement status" in the *Model 4200A-SCS Clarius User's Manual*.
NOISE	Formulator calculation result.

NOTE: AB = Terminal A to Terminal B.

cf-10 pF test

This test performs a frequency sweep that measures capacitance at each frequency point and generates a C versus F graph.

Analyze sheet

Test data is displayed in the Analyze sheet:

Cp_AB	Measured parallel capacitance.
Gp_AB	Measured conductance.
DCV_AB	Forced dc bias voltage.
F_AB	Forced test frequency.
CVU1S	Status code for each measurement. Rows highlighted in blue indicate a fault. For details, refer to "Measurement status" in the *Model 4200A-SCS Clarius User's Manual*.

NOTE: AB = Terminal A to Terminal B.

Carbon Nanotube Transistor Characterization Project (cntfet-characterization)

This project contains dc I-V, pulsed I-V, and C-V tests for a carbon nanotube FET (CNTFET).

The dc I-V tests include measurements for drain current versus drain voltage (V_{ds-Id}) at stepped gate voltages and drain current versus gate voltage (V_{gs-Id}) at a constant drain voltage.

The pulsed I-V tests include pulsed V_{ds-Id} and pulsed V_{gs-Id}.

The C-V test includes a C-V sweep test that measures the gate-to-drain capacitance as a function of the gate voltage of a CNTFET.

The tests include:

- CNTFET Drain Family of Curves (`cntfet-vds-id`): Generates a family of drain current versus drain voltage curves on a CNTFET. For each gate voltage step, the test sweeps the drain voltage and measures the resulting drain current. This test uses either two or three SMUs connected to the gate, drain, and source terminals of the device.

- CNTFET Drain Current versus Gate Voltage (`cntfet-vgs-id`): This test sweeps the gate voltage (V_g) and measures the resulting drain current (I_d) while the drain voltage (V_d) is kept constant.

- CNTFET Capacitance versus Voltage Sweep (`cntget-cvsweep`): Measures the gate-to-drain capacitance as a function of the gate voltage of a carbon nanotube FET. The test is made at a constant test frequency.

- CNTFET Pulsed Drain Family of Curves (`pulsed-vds-id`): Uses CH1 and CH2 of a PMU to generate a pulse I-V drain family of curves. CH1 outputs a pulse step output to the gate. CH2 outputs a pulsed drain voltage sweep and measures the drain current.

- CNTFET Single Pulse I-V (`cnt-pulse`): The waveform capture mode of the PMU shows the time-based response of the drain current and drain voltage of a CNTFET. CH1 outputs a single pulse to the gate. CH2 captures the transient response of the drain current and drain voltage.

Demo project (default)

The tests in this project represent the most common device tests.

The tests in the default project that use the CVU are `cv-nmosfet`, `cv-diode`, and `cv-cap`.

cv-nmosfet test

Measures the capacitance as a function of the gate voltage between the gate terminal and the drain, source, and bulk terminals tied together. Several parameters are extracted, including the flatband capacitance, doping density, flatband voltage, and oxide thickness.

cv-diode test

Measures the junction capacitance as a function of an applied voltage sweep. The depletion depth (W) and the doping density (N) are calculated as a function of the C-V data.

cv-cap test

Measures the capacitance as a function of voltage on a capacitor. The noise is calculated using the standard deviation of the data.

Diode Project (diode)

This project contains dc I-V, C-V, and pulse I-V tests for a PN junction.

The `diode` project measures the capacitance of a pn junction or Schottky diode as a function of the dc bias voltage across the device. The PN junctions must be highly asymmetrical p+n or n+p junctions, which means that one side of the junction is much more highly doped than the other side. If this is the case, the effects of the space charge region spreading into the more highly doped area can be ignored.

C-V measurements on semiconductor junctions are based on the fact that the width (W) of the depletion region of the junction is not constant, but varies with the dc voltage across the junction. This capacitance, related to the space charge region of the semiconductor junction, is known as the junction capacitance. This concept is illustrated in the next figures, showing a reverse-biased Schottky diode and a reverse-biased p+n junction.

Figure 64: Reverse-biased Schottky diode
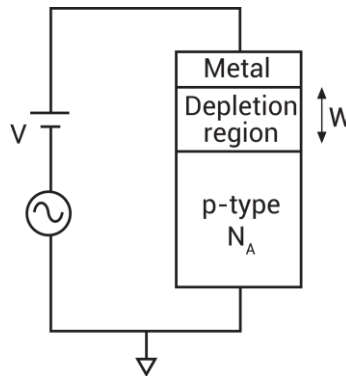
Figure 65: Reverse-biased p+n junction
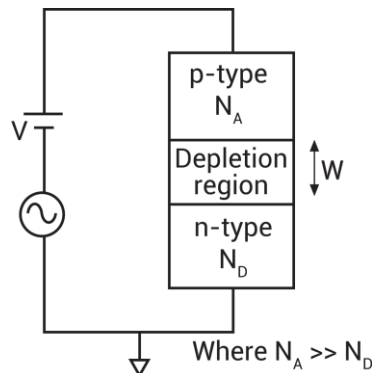
Since the junction can be modeled after a parallel plate capacitor, the junction capacitance is calculated as follows:

$$C = \frac{\varepsilon_S A}{W}$$

Where:

- C = junction capacitance (F)
- ε_S = semiconductor permittivity (1.034e-12 F/cm for silicon)
- A = area of junction (cm^2)
- W = depletion width (cm)

However, unlike the parallel plate capacitor, the depletion layer width (W) is not a constant, but is dependent on the applied voltage. From the previous equation the depletion depth, W, can be calculated as follows:

$$W = \frac{\varepsilon_S A}{C}$$

From the measured capacitance and the voltage, the doping density can be calculated as follows:

$$N(W) = \frac{2}{q \varepsilon_S A^2 \left[\dfrac{d\left(\frac{1}{C^2}\right)}{dV} \right]}$$

Where:

- $N(W)$ = doping density (cm^{-3})
- A = area of junction (cm^2)
- C = junction capacitance (F)
- ε_S = semiconductor permittivity (1.034e-12 F/cm for silicon)
- q = electron charge (1.60219e-19 C)
- V = junction voltage

diode connections

The following figure shows the basic test configuration. Refer to Typical test connections to a probe card (on page 2-5) for the connections to a semiconductor wafer.

Use only the supplied (red) 100 Ω SMA cables for connections to the 4210-CVU or 4215-CVU. Use SMA cables that are all the same length.

NOTE

After making or changing connections, be sure to use the CVU Confidence Check diagnostic tool and do connection compensation tests. Refer to Run an open check and short check (on page 2-17) and Connection compensation (on page 2-8) for details.

Figure 66: Basic configuration to test a semiconductor junction
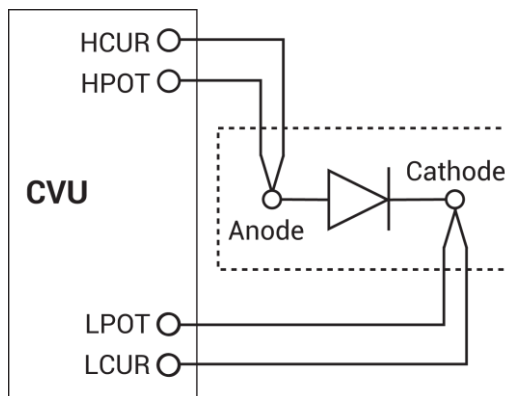
diode project formulas and constants

Formulas and user-defined constants that are used for the tests are listed in the next topics. The formulas and constants are set from the Formulator for each test.

Formula: DEPTH

Formula name: DEPTH (W)

Units: cm

Description: Width of depletion (junction) region.

Formulator entry:

DEPTH = (ES*AREA)/(CP_AC)

Simplified equation:

$$W = \frac{\varepsilon_S A}{C}$$

Formula: INV_C

Formula name: INV_C (C)

Units: 1/F

Description: Inverse capacitance.

Formulator entry: INV_C = 1/(CP_AC)^2

Simplified equation:

$$C = \frac{1}{C^2}$$

Formula: DOPING

Formula name: DOPING (N)

Units: $1/cm^3$

Description: Majority carrier concentration.

Formulator entry:

DOPING = ABS(2/Q/ES/AREA^2/DIFF(INV_C, DCV_AC))

Simplified equation:

$$N(W) = \frac{2}{q\varepsilon_S A^2 \left[\dfrac{d\left(\dfrac{1}{C^2}\right)}{dV} \right]}$$

Constants for the diode project

Constant	Default Value	Units	Description
AREA	0.0001	cm^2	Gate area of device
ES	1.034e-12	F/cm	ε_S - Semiconductor permittivity

diode-cvsweep test

This test measures the PN junction capacitance as a function of the dc bias voltage while the junction is reverse biased. The test makes a capacitance measurement at each step of a user-configured linear voltage sweep. From the acquired C-V data, the test uses the Formulator to calculate parameters.

diode-cvsweep Analyze sheet

The test data is displayed in the Analyze sheet:

- Cp_AC: Measured parallel capacitance.

- Gp_AC: Measured conductance.

- DCV_AC: Forced dc bias voltage.

- F_AC: Forced test frequency.

- INV_C: Inverse capacitance.

- DEPTH: Width of depletion (junction) region.

- DOPING: Majority carrier concentration.

- Formulas: Formulator calculation results.

NOTE

AC = Anode to cathode.

diode-c-2vsv test

This test displays the data as a $1/C^2$ versus V curve. You can derive the doping density (N) from the slope of this curve because N is linearly related to the capacitance.

You can derive the built-in potential (φ_B) of the diode from the intersection of the $1/C^2$ curve and the horizontal axis. Use the graph option Linear Line Fit to derive both the doping density (N) and the built-in voltage on the x-axis.

diode-c-2vsv test Analyze sheet

The test data is displayed in the Analyze sheet:

- Cp_AC: Measured parallel capacitance.

- Gp_AC: Measured conductance.

- DCV_AC: Forced dc bias voltage.

- F_AC: Forced test frequency.

- INV_C: Inverse capacitance.

- DEPTH: Width of depletion (junction) region.

- DOPING: Majority carrier concentration.

- Formulas: Formulator calculation results.

NOTE

AC = Anode to cathode.

diode-dopingprofile test

This test performs a C-V sweep and uses the measurements for doping profiling. At each voltage step, the doping density and corresponding depth (W) are calculated and plotted on the graph.

diode-dopingprofile Analyze sheet

The test data is displayed in the Analyze sheet:

- Cp_AC: Measured parallel capacitance.

- Gp_AC: Measured conductance.

- DCV_AC: Forced dc bias voltage.

- F_AC: Forced test frequency.

- INV_C: Inverse capacitance.

- DEPTH: Width of depletion (junction) region.

- DOPING: Majority carrier concentration.

- Formulas: Formulator calculation results.

NOTE

AC = Anode to cathode.

High-Voltage C-V Tests Project (cvu-highv)

This project contains tests for making high-voltage C-V measurements on a Zener diode, MOS capacitor, capacitor, and a Schottky diode.

The 4205-RBT is included in the 4200-CVU-PWR C-V Power Package.

The tests in this project include:

- Zener Diode High-Voltage C-V Sweep (`hvcv-zener`): Enables high voltage C-V measurements on a Zener diode using the CVU, SMU, and either the 4200A-CVIV multi-switch or 4205-RBT remote bias tee.

- MOS Capacitor High-Voltage C-V Sweep (`hvcv-moscap`): Enables a high-voltage C-V sweep on a MOS capacitor using the CVU, SMU, and the 4205-RBT remote bias tee. Common parameters are derived in the Formulator, including the oxide thickness, flatband voltage, threshold voltage, and doping concentration.

- Capacitor High-Voltage Bias Capacitance Measurements (`200vbias`): Makes a high-voltage C-V measurement on a capacitor using the CVU, SMU, and the 4200A-CVIV or 4200-CVU-PWR (two 4205-RBTs).

- Capacitor High-Voltage C-V Sweep (`200vsweep`): Enables a high-voltage C-V sweep on a capacitor using the CVU, SMU, and the 4200A-CVIV or 4200-CVU-PWR (two 4205-RBTs).

- Schottky Capacitor 400 V C-V Sweep (400vsweep): Enables a high-voltage C-V sweep on a Schottky diode using the CVU, SMU, and the 4200A-CVIV or 4200-CVU-PWR (two 4205-RBTs).

For additional information on high-voltage measurements, refer to *Application Note 1KW-60637: Using the Model 4200-CVU-PWR C-V Power Package to Make High Voltage and High Current C-V Measurements*.

High Voltage C-V Tests Using 4200A-CVIV Bias Tee Project (cviv-bias-highv)

This project contains tests for making high-voltage C-V measurements on a Zener diode, MOS capacitor, capacitor, and a Schottky diode. These tests use the 4200A-CVIV bias tees to combine signals from a CVU and a SMU. The CVU measures the capacitance and the SMU supplies the dc bias.

The tests in this project include:

- Zener Diode High-Voltage C-V Sweep (hvcv-zener): Enables high voltage C-V measurements on a Zener diode using the CVU, SMU, and either the 4200A-CVIV multi-switch or 4205-RBT remote bias tee.
- MOS Capacitor High-Voltage C-V Sweep (hvcv-moscap): Enables a high-voltage C-V sweep on a MOS capacitor using the CVU, SMU, and the 4205-RBT remote bias tee. Common parameters are derived in the Formulator, including the oxide thickness, flatband voltage, threshold voltage, and doping concentration.
- Capacitor High-Voltage Bias Capacitance Measurements (200vbias): Makes a high-voltage C-V measurement on a capacitor using the CVU, SMU, and the 4200A-CVIV or 4200-CVU-PWR (two 4205-RBTs).
- Capacitor High-Voltage C-V Sweep (200vsweep): Enables a high-voltage C-V sweep on a capacitor using the CVU, SMU, and the 4200A-CVIV or 4200-CVU-PWR (two 4205-RBTs).
- Schottky Diode 400V C-V Sweep (400vsweep): Enables a high-voltage C-V sweep on a Schottky diode using the CVU, SMU, and the 4200A-CVIV or 4200-CVU-PWR (two 4205-RBTs).

For additional information on high-voltage measurements, refer to the following application notes:

- Switching Between C-V and I-V Measurements Using the 4200A-CVIV Multi-Switch and 4200A-SCS Parameter Analyzer
- Switching Between C-V and I-V Measurements Using the 4200A-CVIV Multi-Switch and 4200A-SCS Parameter Analyzer (Japanese)
- Using the 4200A-CVIV Multi-Switch to Make High Voltage and High Current C-V Measurements

MOS Capacitor C-V Project (cvu-moscap)

Maintaining the quality and reliability of gate oxides of MOS structures is a critical task in semiconductor fabrication. A commonly used tool for studying gate-oxide quality in detail is the capacitance-voltage technique. C-V measurements are typically made on a capacitor-like device called a MOS capacitor.

An example of the construction of a MOS capacitor is shown in the following figure. As shown, the MOS capacitor is an oxide placed between a semiconductor and a metal gate. The semiconductor and the metal gate are the two plates of the capacitor. The oxide functions as the dielectric. The area of the metal gate defines the area of the capacitor.

Figure 67: MOS capacitor
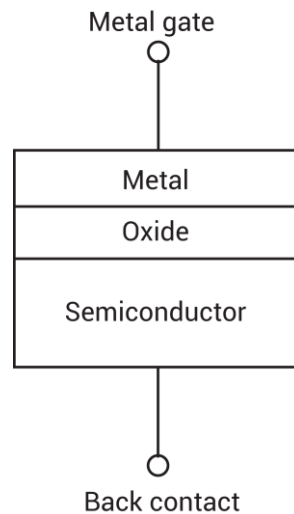
The most important property of the MOS capacitor is that its capacitance changes with changes to applied voltage. As a result, the modes of operation of the MOS capacitor change as a function of the applied voltage. As a dc sweep voltage is applied to the gate, it causes the device to pass through accumulation, depletion, and inversion.

MOS capacitor C-V curves

The following figure illustrates a high-frequency C-V curve for a p-type semiconductor substrate. A C-V curve can be divided into three regions: accumulation, depletion, and inversion. Each of the three regions is described for a p-type MOS capacitor.

Figure 68: C-V curve example for p-type MOS-C
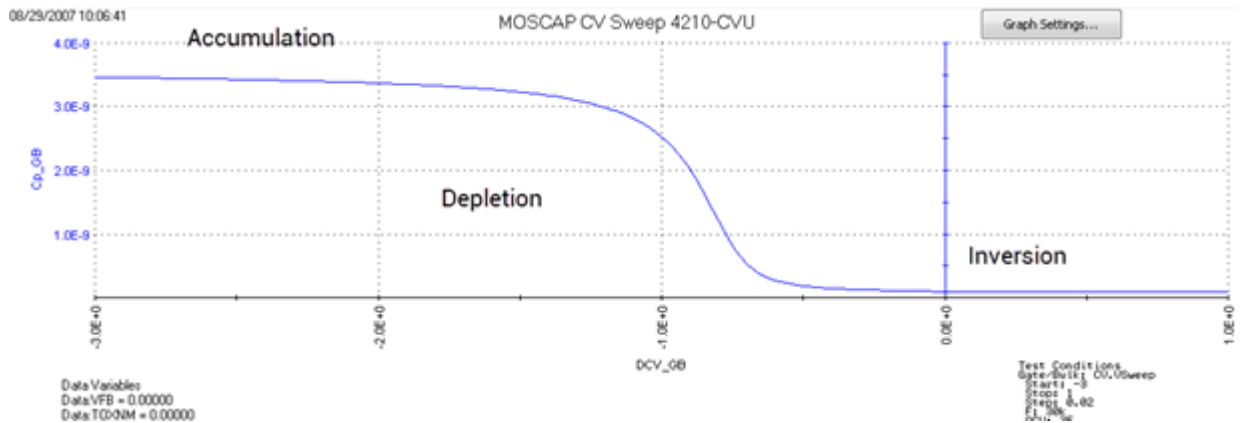
The C-V curve for an n-type MOS capacitor is analogous to a p-type, except that:

- The majority carriers are electrons.

- The n-type MOS capacitor curve shape is essentially a mirror image of the p-type MOS capacitor curve shape.

- The accumulation region occurs at positive polarities.

- The inversion region occurs at negative polarities.

Accumulation region

For a p-type MOS capacitor, the accumulation region of the C-V curve is observed when negative voltages are applied to the gate. The negative polarity causes majority carriers (holes) to be attracted toward the gate. Because the oxide is a good insulator, these holes accumulate at the substrate-to-oxide/well-to-oxide interface.

A C-V test measures the oxide capacitance in the strong accumulation region, where for a p-type MOS capacitor, the voltage is negative enough that the capacitance is essentially constant and the C-V curve slope is essentially flat. There, the oxide thickness can be extracted from the oxide capacitance. However, the C-V curve for a very thin oxide often does not saturate to a flat slope. In that case, the measured oxide capacitance differs from the true oxide capacitance.

Depletion region

For a p-type MOS capacitor, as the gate voltage moves toward positive values, the MOS capacitor starts to differ from a parallel-plate capacitor. Roughly at the point where the gate voltage becomes positive, the following occurs:

- The positive gate electrostatically repels holes from the substrate-to-oxide/well-to-oxide interface.

- A carrier-depleted area forms beneath the oxide, creating an insulator (recall that the absence of free-moving charges distinguishes an insulator from a conductor).

As a result, the high-frequency 4210-CVU or 4215-CVU measures two capacitances in series: the oxide capacitance and the depletion capacitance. As the gate voltage becomes more positive, the following occurs:

- The depletion zone penetrates more deeply into the semiconductor.

- The depletion capacitance becomes smaller, and consequently, the total measured capacitance becomes smaller.

Therefore, the C-V curve slope is negative in the depletion region.

Inversion region

For a p-type MOS capacitor, as the gate voltage increases beyond the threshold voltage, dynamic carrier generation and recombination move toward net carrier generation. Although the average net concentration of carriers in a semiconductor is stable at equilibrium, carrier generation and recombination occur dynamically.

The positive gate voltage both generates electron-hole pairs and attracts electrons (the minority carriers) toward the gate. Again, because the oxide is a good insulator, these minority carriers accumulate at the substrate-to-oxide / well-to-oxide interface. The accumulated minority-carrier layer is called the inversion layer, because the carrier polarity is inverted. Above a certain positive gate voltage, most available minority carriers are in the inversion layer, and further gate-voltage increases do not further deplete the semiconductor. That is, the depletion region reaches a maximum depth.

However, inversion-charge generation is slower than the 1 MHz or 100 kHz frequency of the high frequency-CV (HF-CV) measurement. The average time to generate an inversion charge is ~$10\tau_g N_a/n_i$, where τ_g is the generation lifetime (seconds), N_a is the doping concentration (cm^{-3}), and n_i is the intrinsic carrier concentration (cm^{-3}). For a 10^{15} cm^{-3} doping concentration and microsecond generation lifetime, electron-hole-pair (ehp) generation cannot keep up with the high frequency measurement signal. Therefore, once the depletion region reaches a maximum depth, the capacitance that is measured by the HF-CV analyzer is still based on the majority carrier position and distribution. The following applies:

- The capacitance that is measured by the HF-CV analyzer is the oxide capacitance in series with maximum depletion capacitance. This capacitance is often referred to as minimum capacitance.

- The C-V curve slope is almost flat.

NOTE
The measured inversion-region capacitance at the maximum depletion depth depends on the measurement frequency. Therefore, C-V curves measured at different frequencies may have different appearances. Generally, such differences are more significant at lower frequencies and less significant at higher frequencies.

cvu-moscap connections

The following figure shows the basic test configuration for testing a MOS capacitor.

Figure 69: Simplified configuration to test MOS capacitor
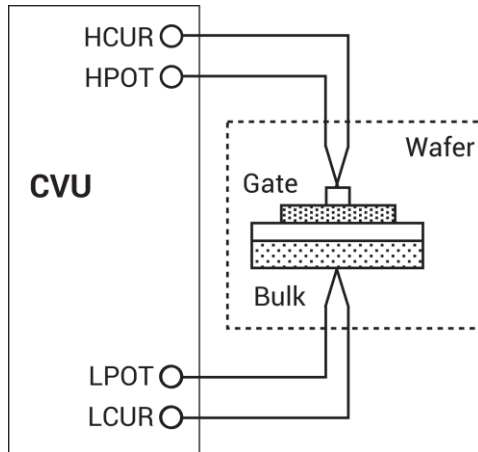
[CVU connections](#) (on page 2-1) provides details on connections to a semiconductor wafer. Use only the supplied (red) 100 Ω SMA cables for connections to the 4210-CVU or 4215-CVU. Be sure that all SMA cables are the same length.

NOTE

After making or changing connections, be sure to use the CVU Confidence Check diagnostic tool and do connection compensation tests. Refer to [Run an open check and short check](#) (on page 2-17) and [Connection compensation](#) (on page 2-8) for details.

cvu-moscap project formulas

Formulas and user-defined constants that are used for the application tests are summarized (in alphabetical order) in the following.

Formula: AR

Formula name: AR (aR)

Units: None

Description: Intermediate parameter for calculation of corrected capacitance.

Formulator entry:

AR = GP_GB-(GP_GB^2 + (2*PI*F_GB*CP_GB)^2)*RS

Simplified equation:

$$a_R = G - \left(G^2 + (2\pi f C)^2 R_s \right)$$

Formula: BEST_HI

Formula name: BEST_HI

Units: None

Description: Index from DEPTHM array that is 95% of maximum depletion length or twice the screening length in the semiconductor, whichever is larger.

Formulator entry:

BEST_HI = FINDD(DEPTHM,COND(2*DEBYEM*SQRT(LN(ABS(N90W/NI))),MAX(DEPTHM), 2*DEBYEM*SQRT(LN(ABS(N90W/NI)))), 0.95*MAX(DEPTHM), 2)

Formula: BEST_LO

Formula name: BEST_LO

Units: None

Description: Index from DEPTHM array that is three Debye lengths from the surface.

Formulator entry:

BEST_LO = FINDD(DEPTHM, 3*DEBYEM, 2)

Formula: CADJ

Formula name: CADJ (C$_{ADJ}$)

Units: F

Description: Corrected capacitance by compensating series resistance.

Formulator entry:

CADJ = ((GP_GB^2 + (2*PI*F_GB*CP_GB)^2)*(CP_GB)/(AR^2 + (2*PI*F_GB*CP_GB)^2)

Simplified equation:

$$C_{ADJ} = \frac{(G^2 + (2\pi fC)^2)C}{a_R^2 + 2\pi fC^{\ 2}}$$

Formula: CFB

Formula name: CFB (C_{FB})

Units: F

Description: Flatband capacitance.

Formulator entry:

CFB = (COX*ES*AREA/(DEBYEM*1E2))/(COX+(ES*AREA/(DEBYEM*1E2)))

Simplified equation:

$$C_{FB} = \frac{C_{OX}\left(\frac{\varepsilon_S A}{\lambda}\right)(1 \times E^2)}{C_{OX} + \left(\frac{\varepsilon_S A}{\lambda}\right)(1 \times E^2)}$$

Formula: CMIN

Formula name: CMIN

Units: F

Description: Minimum capacitance.

Formulator entry:

CMIN = MIN(MAVG(CADJ, 10))+1E-15

Formula: COX

Formula name: COX (C_{OX})

Units: F

Description: Oxide capacitance, usually set to maximum capacitance in accumulation.

Formulator entry:

COX = MAX(MAVG(CADJ, 10))+1E-15

Formula: DEBYEM

Formula name: DEBYEM (λ)

Units: m

Description: Debye length (in meters).

Formulator entry:

DEBYEM = SQRT(ES*K*TEMP/(ABS(N90W)*Q^2))*1E-2

Simplified equation:

$$\lambda = \left(\frac{\varepsilon_S kT}{q^2 N_X}\right)^{1/2} (1xE^{-2})$$

Formula: DEPTHM

Formula name: DEPTHM (W)

Units: m

Description: Depletion depth (in meters).

Formulator entry:

DEPTHM = 1E-2*AREA*ES*(1/CADJ-1/COX)

Simplified equation:

$$W = A\varepsilon_S \left(\frac{1}{C} - \frac{1}{C_{OX}}\right)(1xE^{-2})$$

Formula: INVCSQR

Formula name: INVCSQR

Units: $1/F^2$

Description: Inverse square of capacitance.

Formulator entry:

INVCSQR = 1/(MAVG(CADJ, 5))^2

Simplified equation:

$$INVCSQR = \frac{1}{C^2}$$

Formula: MAXINVSQR

Formula name: MAXINVSQR

Units: $1/F^2$

Description: Finds row position of maximum point on $1/C^2$ curve.

Formulator entry:

MAXINVSQR = MAXPOS(INVCSQR)

Formula: N90W

Formula name: N90W

Units: None

Description: Doping density at 90% of maximum depletion depth.

Formulator entry:

N90W = AT(NDOPING, FINDD(DEPTHM, 0.9*MAX(DEPTHM), 2))

Formula: NAVG

Formula name: NAVG (N_{AVG})

Units: None

Description: Average doping calculated between index BEST_HI and BEST_LO.

Formulator entry:

NAVG = AVG(SUBARRAY(NDOPING, COND(BEST_HI, BEST_LO, BEST_HI, BEST_LO), COND(BEST_HI, BEST_LO, BEST_LO, BEST_HI))))

Formula: NDOPING

Formula name: NDOPING (N)

Units: $1/cm^3$

Description: Doping density.

Formulator entry:

NDOPING = ABS((-2)/(AREA^2*Q*ES)/(DELTA(INVCSQR)/DELTA(DCV_GB)))

Simplified equation:

$$N(W) = \frac{2}{q\varepsilon_S A^2 \left[\dfrac{d\left(\dfrac{1}{C^2}\right)}{dV}\right]}$$

Formula: NSLOPE

Formula name: NSLOPE

Units: None

Description: Finds slope of $1/C^2$ curve.

Formulator entry:

NSLOPE = LINFITSLP(DCV_GB, INVCSQR, VFBPOS, MAXINVSQR)

Formula: NSUB

Formula name: NSUB

Units: $1/cm^3$

Description: Calculated substrate doping concentration.

Formulator entry:

NSUB = 2/(NSLOPE*Q*ES*AREA^2)

Formula: PHIB

Formula name: PHIB (φ_B)

Units: V

Description: Bulk potential.

Formulator entry:

PHIB = (-1)*K*TEMP/Q*LN(ABS(N90W)/NI)*DOPETYPE

Simplified equation:

$$\phi_B = \frac{kT}{q} Ln\left(\frac{N_{BULK}}{N_i}\right) (DopeType)$$

Formula: QEFF

Formula name: QEFF (Q_{EFF})

Units: C/cm^2

Description: Effective oxide charge.

Formulator entry:

QEFF = COX*(WMS-VFB)/AREA

Simplified equation:

$$Q_{EFF} = \frac{C_{OX}(W_{MS} - V_{FB})}{A}$$

Formula: RS

Formula name: RS (R_S)

Units: Ω

Description: Series resistance calculated from capacitance.

Formulator entry:

RS = (AT(MAVG(GP_GB, 5)/((2*PI*F_GB)*MAVG(CP_GB, 5)), MAXPOS(MAVG(CP_GB,5))))^2
((1+(AT (MAVG(GP_GB, 5)/((2*PI*F_GB)*MAVG(CP_GB, 5)),MAXPOS(MAVG(CP_GB,5))))^2)
*(AT(MAVG (GP_GB, 5),MAXPOS(MAVG(CP_GB, 5)))))

Simplified equation:

$$R_S = \frac{\left(\frac{G}{2\pi f C}\right)^2}{\left[1 + \left(\frac{G}{2\pi f C}\right)^2\right] G}$$

Formula: TOXNM

Formula name: TOXNM (T_{OX})

Units: nm

Description: Calculated thickness of oxide (in nanometers).

Formulator entry: TOXNM = (1E7*AREA*EOX)/COX

Simplified equation:

$$T_{OX} = \left(\frac{A\varepsilon_{OX}(1xE^7)}{C_{OX}}\right)$$

Formula: VFB

Formula name: VFB (V_{FB})

Units: V

Description: Flatband voltage. Once CFB (CFB) is derived, V_{FB} is interpolated from the closest V_{GS} values.

Formulator entry:

VFB = AT(DCV_GB,FINDD(CADJ, CFB, 2))

Formula: VFBPOS

Formula name: VFBPOS

Units: None

Description: Finds row position of flatband voltage.

Formulator entry:

VFBPOS = FINDD(DCV_GB, VFB, 2)

Formula: VTH

Formula name: VTH (V_{TH})

Units: V

Description: Threshold voltage

Formulator entry:

VTH = VFB+DOPETYPE*(AREA/COX*SQRT(4*ES*Q*ABS(N90W*PHIB)) + 2*ABS(PHIB))

Simplified equation:

$$V_{TH} = \left[\pm \frac{A}{10^{12}C_{OX}} \sqrt{4\,\varepsilon_S\,q|N_{BULK}||\phi_B|} + 2|\phi_B| \right] + V_{FB}$$

Formula: WMS

Formula name: WMS (W_{MS})

Units: V

Description: Work function difference between metal and semiconductor (W_M and W_S are defined in the constants area of the Formulator).

Formulator entry:

WMS = WM-(WS+(EBG/2)-PHIB)

Simplified equation:

$$W_{MS} = W_M - \left[W_S + \frac{E_G}{2} - \phi_B \right]$$

cvu-moscap project constants

The user-defined constants that are used for the application tests are summarized (in alphabetical order) in the next tables.

Constant	Default value	Units	Description
AREA	0.010404	cm^2	Gate area of device
DOPETYPE	1	none	1 = P-type, −1 = N-type
EBG	1.12	eV	E_{BG} - Semiconductor energy gap
EOX	3.4e-013	F / cm	ϵ_{OX} - Permittivity of oxide
ES	1.03e-012	F / cm	ϵ_S - Semiconductor permittivity
NI	1.45e+10	cm^{-3}	N_I - Intrinsic carrier concentration
TEMP	300	K	Test temperature
WM	4.15	V	W_M - Metal work function
WS	4.05	V	W_S - Silicon electron affinity

moscap-cvsweep test

This test makes a capacitance measurement at each step of a user-configured linear voltage sweep. Using the acquired C-V data, the Formulator calculates parameters, including oxide capacitance (C_{OX}), oxide thickness (T_{OX}), flatband capacitance (C_{FB}), flatband voltage (V_{FB}), doping density, depletion depth (DEPTHM), Debye length, threshold voltage (V_{TH}), and the effective oxide charge (Q_{EFF}).

The series resistance (R_S) is also calculated from the capacitance (in strong accumulation) and the conductance. The corrected capacitance (C_{ADJ}) is calculated by compensating for the series resistance.

From the acquired data, a capacitance versus voltage graph is generated.

moscap-cvsweep Analyze sheet

The test data is displayed in the Analyze sheet:

- Cp_GB: Measured parallel capacitance.

- Gp_GB: Measured conductance.

- DCV_GB: Forced dc bias voltage.

- F_GB: Forced test frequency.

- Formulas: Formulator calculation results.

NOTE

GB = gate-to-bulk.

moscap-c-2vsv test

This test performs a C-V sweep and displays the inverse squared capacitance ($1/C^2$) as a function of the gate voltage (V_G). This sweep can yield important information about the doping profile because the substrate doping concentration (N_{SUB}) is inversely related to the reciprocal of the slope of the $1/C^2$ versus V_G curve. A positive slope indicates acceptors and a negative slope indicates donors. The substrate doping concentration is extracted from the slope of the $1/C^2$ curve and is displayed on the graph. The doping concentration is the result of the NSUB Formulator calculation.

In the following equation, *N* (NDOPING) is related to the reciprocal of the slope of the $1/C^2$ versus V_G curve.

$$N(W) = \frac{2}{q\varepsilon_S A^2 \left[\frac{d\left(\frac{1}{C^2}\right)}{dV} \right]}$$

Where:

- $N(W)$ = doping concentration (cm^{-3})

- A = gate area (cm^2)

- C = measured capacitance (F)

- ε_s = permittivity of the substrate material (F/cm)

- q = electron charge (1.60219×10^{-19} C)

- V = gate voltage (V)

moscap-c-2vsv Analyze sheet

The test data is displayed in the Analyze sheet:

- Cp_GB: Measured parallel capacitance.

- Gp_GB: Measured conductance.

- DCV_GB: Forced dc bias voltage.

- F_GB: Forced test frequency.

- Formulas: Formulator calculation results.

NOTE

GB = gate-to-bulk.

moscap-dopingprofile test

This test generates a doping profile, which is a plot of the doping concentration versus depletion depth. The difference in capacitance at each step of the gate voltage is proportional to the doping concentration. The depletion depth is computed from the high-frequency capacitance and oxide capacitance at each measured value of the gate voltage. The results are plotted on the graph.

The doping concentration (*N*) is calculated in the `moscap-c-2vsv` test. The depletion depth (*W*), which is called `DEPTHM` in the Formulator, is computed from the high frequency capacitance and the oxide capacitance at each measured value of the gate voltage (from Nicollian and Brews, p. 386; see References (on page 4-45)). The program computes each *W* element of the calculated data array as shown below:

$$W = A\varepsilon_S \left(\frac{1}{C} - \frac{1}{C_{OX}} \right) \left(1xE^{-2} \right)$$

Where:

- W = depth (m)

- A = gate area (cm^2)

- C = measured capacitance (F)

- ε_s = permittivity of the substrate material (F/cm)

- C_{ox} = oxide capacitance (F)

- $1xE^{-2}$ = units conversion from cm to m

moscap-dopingprofile Analyze sheet

The test data is displayed in the Analyze sheet:

- Cp_GB: Measured parallel capacitance.

- Gp_GB: Measured conductance.

- DCV_GB: Forced dc bias voltage.

- F_GB: Forced test frequency.

- CVU1S: Status code for each measurement. Rows highlighted in blue indicate a fault. For details, refer to "Measurement status" in the *Model 4200A-SCS Clarius User's Manual.*

- Formulas: Formulator calculation results.

NOTE

GB = gate-to-bulk.

Compensating for series resistance

After generating a C-V curve, you may need to compensate the measurements for series resistance. The series resistance (R_{SERIES}) can be attributed to either the substrate (well) or the backside of the wafer. For wafers typically produced in fabrication plants, the substrate bulk resistance is small (<10 Ω) and has negligible impact on C-V measurements. However, if the backside of the wafer is used as an electrical contact, the series resistance due to oxides can significantly distort a measured C-V curve.

Without series compensation, capacitance can be lower than normal and C-V curves can be distorted. Tests for this project compensate for series resistance using the simplified 3-element model shown in the following figure.

In this model, C_{OX} is the oxide capacitance while CA is the capacitance of the accumulation layer. The series resistance is represented by R_{SERIES}.

Figure 70: Simplified model to determine series resistance

Three-element model of MOS capacitor in strong accumulation

Simplified model of three-element model that is used to determine R_{SERIES}
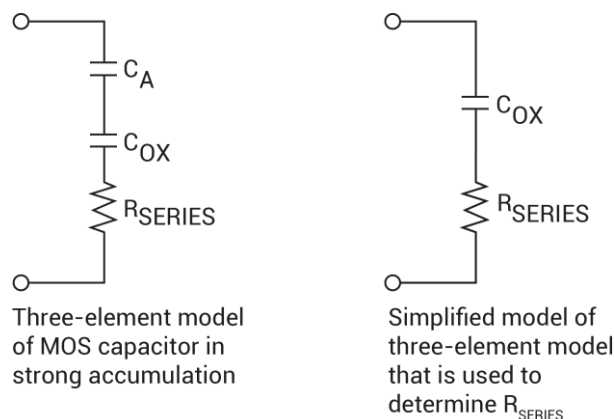
The corrected capacitance (C_{ADJ}) and corrected conductance (G_{ADJ}) are calculated from the formulas shown below (from Nicollian and Brews, p. 222-264; see References (on page 4-45)).

$$C_{ADJ} = \frac{(G^2+(2\pi fC)^2)C}{a_R^2 + (2\pi fC)^2}$$

$$G_{ADJ} = \frac{(G^2+(2\pi fC)^2)Q_R}{a_R^2 + (2\pi fC)^2}$$

Where:

$$a_R = G - \left(G^2+(2\pi fC)^2 R_s\right)$$

Where:

- C_{ADJ} = series resistance compensated parallel model capacitance

- G_{ADJ} = series resistance compensated conductance

- C = measured parallel model capacitance

- G = measured conductance

- f = test frequency as set in Clarius

- R_S = series resistance

The series resistance, R_S, may be calculated from the capacitance and conductance values that are measured while biasing the DUT (device under test) in the accumulation region. The series resistance is calculated as follows:

$$R_S = \frac{\left(\frac{G}{2\pi fC}\right)^2}{\left[1+\left(\frac{G}{2\pi fC}\right)^2\right]G}$$

Where:

- R_S = series resistance

- G = measured conductance

- C = measured parallel model capacitance (in strong accumulation)

- f = test frequency as set in Clarius

NOTE

The above equations for compensating for series resistance require that the CVU is using the parallel model (Cp-Gp).

In this project, these formulas have been added into the Clarius Formulator so the capacitance and conductance can be automatically compensated for the series resistance.

Extracting MOS device parameters from C-V measurements

The following topics describe how MOS device parameters are extracted from C-V measurements.

Oxide thickness

For a relatively thick oxide (>50Å), the oxide capacitance (C_{OX}) is the high-frequency capacitance when the device is biased for strong accumulation. In the strong accumulation region, the MOS capacitor acts like a parallel-plate capacitor, and the oxide thickness (T_{OX}) may be calculated from C_{OX} and the gate area using the following equation:

$$T_{OX} = \left(\frac{A\varepsilon_{OX}(1xE^7)}{C_{OX}} \right)$$

Where:

- T_{OX} = oxide thickness (nm)

- A = gate area (cm^2)

- ε_{OX} = permittivity of the oxide material (F/cm)

- C_{OX} = oxide capacitance (F)

- $1 \times E^7$ = units conversion from cm to nm

NOTE

Oxide thickness calculations based on C-V measurements can be very precise. Oxide thickness must be extracted from the strong accumulation region, where the capacitance measured truly reflects the oxide capacitance.

The oxide capacitance, C_{OX}, is set in the Formulator to be the maximum capacitance in accumulation.

Flatband capacitance and flatband voltage

Application of a certain gate voltage, the flatband voltage (V_{FB}), results in the disappearance of band bending. At this point, known as the flatband condition, the semiconductor band is said to become flat. Because the band is flat, the surface potential is zero, with the reference potential being taken as the bulk potential deep in the semiconductor. Flatband voltage and its shift are widely used to extract other device parameters, such as oxide charges.

V_{FB} can be identified from the C-V curve. One way is to use the flatband capacitance method. For this method, the ideal value of the flatband capacitance (C_{FB}) is calculated using equations below. Once the value of C_{FB} is known, the value of V_{FB} can be obtained from the C-V curve data by interpolating between the closest gate-to-substrate (V_{GS}) values (from Nicollian and Brews pp 487-488; see References (on page 4-45)).

The Debye equation calculates the Debye length parameter (λ) that is used in the flatband capacitance equation. Based on the doping profile, the λ calculation requires one of the following doping concentrations: N at 90% of W_{MAX} (refer to Nicollian and Brews), a user-supplied NA (bulk-doping concentration for a p-type acceptor material), or a user-supplied ND (bulk doping concentration for an n-type donor material).

NOTE

The flatband capacitance method is invalid when the interface trap density (DIT) becomes very large (10^{12} to 10^{13} or greater). However, the method should give satisfactory results for most users. Those dealing with high DIT values should consult the appropriate literature for a more suitable method.

Use the next two equations to calculate the flatband capacitance:

$$C_{FB} = \frac{C_{OX}\left(\frac{\varepsilon_S A}{\lambda}\right)\left(1 \times E^2\right)}{C_{OX} + \left(\frac{\varepsilon_S A}{\lambda}\right)\left(1 \times E^2\right)}$$

Where:

- CFB = flatband capacitance (F)

- C_{ox} = oxide capacitance (F)

- ε_s = permittivity of the substrate material (F/cm)

- A = gate area (cm^2)

- $1 \times E^2$ = units conversion from m to cm

- λ = extrinsic Debye length, which is calculated as follows:

$$\lambda = \left(\frac{\varepsilon_S kT}{q^2 N_X}\right)^{1/2} \left(1 \times E^{-2}\right)$$

Where:

- ε_s = permittivity of the substrate material (F/cm)

- kT = thermal energy at room temperature (293 K) (4.046×10^{-21}J)

- q = electron charge (1.60219×10^{-19} C)

- Nx = *N* at 90% W_{MAX} or N90W (refer to Nicollian and Brews; see [References](#) (on page 4-45)) or, when input by the user, $N_X = N_A$ or $N_X = N_D$

- $1 \times E^{-2}$ = units conversion from cm to m

The extrinsic Debye length is an idea borrowed from plasma physics. In semiconductors, majority carriers can move freely. The motion is similar to a plasma. Any electrical interaction has a limited range. The Debye length is used to represent this interaction range. Essentially, the Debye length indicates how far an electrical event can be sensed within a semiconductor.

Threshold voltage

The turn-on region for a MOSFET corresponds to the inversion region on its C-V plot. When a MOSFET is turned on, the channel formed corresponds to strong generation of inversion charges. It is these inversion charges that conduct current. When a source and drain are added to a MOS capacitor to form a MOSFET, a p-type MOS capacitor becomes an n-type MOSFET, also called an n-channel MOSFET. Conversely, an n-type MOS capacitor becomes a p-channel MOSFET.

The threshold voltage, V_{TH}, is the point on the C-V curve where the surface potential ψ_S, equals twice the bulk potential, ϕ_B. This point on the curve corresponds to the onset of strong inversion. For an enhancement mode MOSFET, V_{TH} corresponds to the point where the device begins to conduct.

V_{TH} is calculated as follows:

$$V_{TH} = \left[\pm \frac{A}{10^{12}C_{OX}} \sqrt{4\,\varepsilon_S\,q|N_{BULK}||\phi_B| + 2|\phi_B|} \right] + V_{FB}$$

Where:

- V_{TH} = threshold voltage (V)

- A = gate area (cm^2)

- C_{OX} = oxide capacitance (pF)

- 10^{12} = units multiplier

- ε_S = permittivity of substrate material

- q = electron charge (1.60219×10^{-19} coulombs)

- N_{BULK} = bulk doping (cm^{-3})

- ϕ_B = bulk potential (V)

- V_{FB} = flatband voltage (V)

The physical meaning of the threshold voltage is the same for both a MOS capacitor C-V curve and a MOSFET I-V curve. However, in practice, the numeric V_{TH} value for a MOSFET may be slightly different, due to the particular method used to extract the threshold voltage.

The threshold voltage of a MOS capacitor can be calculated as follows:

$$V_{TH} = V_{FB} \pm \left[\frac{A}{C_{OX}} \sqrt{4\,\varepsilon_S\,q|N_{BULK}\phi_B|} + 2|\phi_B| \right]$$

Where:

- V_{TH} = threshold voltage (V)

- V_{FB} = flatband potential (V)

- A = gate area (cm^2)

- C_{OX} = oxide capacitance (F)

- ε_S = permittivity of substrate material (F/cm)

- q = electron charge (1.60219 x 10^{-19} coulombs)

- N_{BULK} = bulk doping (cm^{-3}); note that the Formulator name for N_{BULK} is N90W

- ϕ_B = bulk potential (V); note that the Formulator name for ϕ_B is PHIB

The bulk potential is calculated as follows:

$$\phi_B = \frac{kT}{q} Ln\left(\frac{N_{BULK}}{N_i}\right) (DopeType)$$

Where:

- ϕ_B = bulk potential (V); note that the Formulator name for ϕ_B is PHIB

- k = Boltzmann's constant (1.3807 x 10^{-23} J/K)

- T = Test temperature (K)

- q = electron charge (1.60219 x 10^{-19} coulombs)

- N_{BULK} = bulk doping (cm^{-3}); note that the Formulator name for N_{BULK} is N90W

- N_i = intrinsic carrier concentration (1.45 x 10^{10} cm^{-3})

- DopeType = +1 for p-type materials and -1 for n-type materials; note that the value for DopeType is changed in the Constants area of the Formulator

Metal semiconductor work function difference

The metal semiconductor work function difference, W_{MS}, is commonly referred to as the work function. It contributes to the shift in V_{FB} from the ideal zero value, along with the effective oxide charge (Nicollian and Brews 462-477; Sze 395402). The work function represents the difference in work necessary to remove an electron from the gate and from the substrate, and it is derived as follows:

$$W_{MS} = W_M - \left[W_S + \frac{E_G}{2} - \phi_B \right]$$

Where:

- W_M = metal work function (V)

- W_S = substrate material work function (electron affinity) (V)

- E_G = substrate material bandgap (V)

- ϕ_B = bulk potential (V)

In tests, the values for W_M, W_S, and E_G are listed in the Formulator as constants. You can change the values depending on the type of materials.

For silicon, silicon dioxide, and aluminum:

$$W_{MS} = 4.1 - \left[4.15 + \frac{1.12}{2} - \phi_B \right]$$

$$W_{MS} = -0.61 + \phi_B$$

$$W_{MS} = -0.61 - \left(\frac{kT}{q} \right) \ln \left(\frac{N_{BULK}}{n_i} \right) \ (DopeType)$$

Where:

- k = Boltzmann's constant (1.3807×10^{-23} J/K)

- T = Test temperature (K)

- q = Electron charge (1.60219×10^{-19} C)

- N_{BULK} = Bulk doping (cm^{-3})

- DopeType = is +1 for p-type materials and -1 for n-type materials; the value for DopeType is changed in the Constants area of the Formulator

For example, for a MOS capacitor with an aluminum gate and p-type silicon (N_{BULK} = $10^{16}cm^{-3}$), W_{MS} = −0.95 V.

For the same gate and n-type silicon (N_{BULK} = $10^{16}cm^{-3}$), W_{MS} = −0.27 V.

Because the supply voltage of modern CMOS devices is decreasing and since aluminum reacts with silicon dioxide, heavily doped polysilicon is often used as the gate material. The goal is to achieve a minimal work-function difference between the gate and the semiconductor, while maintaining the conductive properties of the gate.

Effective and total bulk oxide charge

The effective oxide charge, Q_{EFF}, represents the sum of oxide fixed charge (Q_F), mobile ionic charge (Q_M), and oxide trapped charge (Q_{OT}):

$$Q_{EFF} = Q_F + Q_M + Q_{OT}$$

Q_{EFF} is distinguished from interface-trapped charge (Q_{IT}), in that Q_{IT} varies with gate bias and Q_{EFF} does not (Nicollian and Brews pp. 424-429, Sze pp. 390-395; see). Simple measurements of oxide charge using C-V measurements do not distinguish the three components of Q_{EFF}. These three components can be distinguished from one another by temperature cycling, as discussed in Nicollian and Brews, p. 429, Fig. 10.2. Also, since the charge profile in the oxide is not known, the quantity, Q_{EFF}, should be used as a relative, not absolute, measure of charge. It assumes that the charge is located in a sheet at the silicon-silicon dioxide interface.

From Nicollian and Brews, Eq. 10.10, we have:

$$V_{FB} - W_{MS} = -\frac{Q_{EFF}}{C_{OX}}$$

Where:

- V_{FB} = flatband potential (V)
- W_{MS} = metal-semiconductor work function (V)
- Q_{EFF} = effective oxide charge (C)
- C_{OX} = oxide capacitance (F)

    Note that C_{OX} here is per unit of area. So that:

$$Q_{EFF} = \frac{C_{OX}(W_{MS} - V_{FB})}{A}$$

Where:

- Q_{EFF} = effective oxide charge (C)
- C_{OX} = oxide capacitance (F)
- W_{MS} = metal-semiconductor work function (V)
- V_{FB} = flatband potential (V)
- A = gate area (cm^{-2})

For example, assume a 0.01 cm^2, 50 pF, p-type MOS capacitor with a flatband voltage of -5.95 V; its N_{BULK} of 10^{16} cm^{-3} corresponds to a W_{MS} of -0.95 V. For this example, Q_{EFF} calculates to be 2.5 x 10^{-8} C/cm^2, which then causes the threshold voltage to shift ~5 V in the negative direction. Note that in most cases where the bulk charges are positive, there is a shift toward negative gate voltages.

The effective oxide charge concentration (N_{EFF}) is computed from effective oxide charge (Q_{EFF}) and the electron charge as follows:

$$N_{EFF} = \frac{Q_{EFF}}{q}$$

Where:

- N_{EFF} = effective oxide charge density (cm^2)

- Q_{EFF} = effective oxide charge (C)

- q = electron charge (1.60219 x 10^{-19} C)

References

Nicollian, E.H. and Brews, J.R., MOS Physics and Technology, Wiley, New York (2003).

Sze, S.M., Physics of Semiconductor Devices, 2nd edition. Wiley, New York (1985).

MOS Capacitor Lifetime Test Project (moscap-lifetime)

Generation lifetime is an important parameter of metal oxide semiconductor (MOS) capacitors because it determines the storage time of the device. The Zerbst method is a common technique for lifetime measurements. Generating a Zerbst plot requires both a C-V sweep and a C-t sweep.

The C-V sweep derives the oxide capacitance (C_{OX}), the minimum capacitance (C_{MIN}), and the doping concentration (N_{AVG} and N_{BULK}). The capacitance-time (C-t) sweep is then generated. During the C-t sweep, the MOS capacitor is initially held in accumulation and then biased into deep depletion. While holding this bias, the capacitance is measured as a function of time.

The results of the derived parameters (C_{OX}, C_{MIN}, N_{AVG}) from the C-V sweep are integrated with the data taken during the C-t measurements to compute the generation rate and depletion depth. The generation rate is graphed as a function of the calculated depletion depth.

moscap-lifetime connections

The following figure shows the basic test configuration; CVU connections (on page 2-1) provides connection details. Use only the supplied (red) 100 Ω SMA cables for connections to the 4210-CVU or 4215-CVU. Use SMA cables that are all the same length.

NOTE

After making or changing connections, be sure to use the CVU Confidence Check diagnostic tool and do connection compensation tests. Refer to Run an open check and short check (on page 2-17) and Connection compensation (on page 2-8) for details.

Figure 71: Basic configuration for lifetime testing
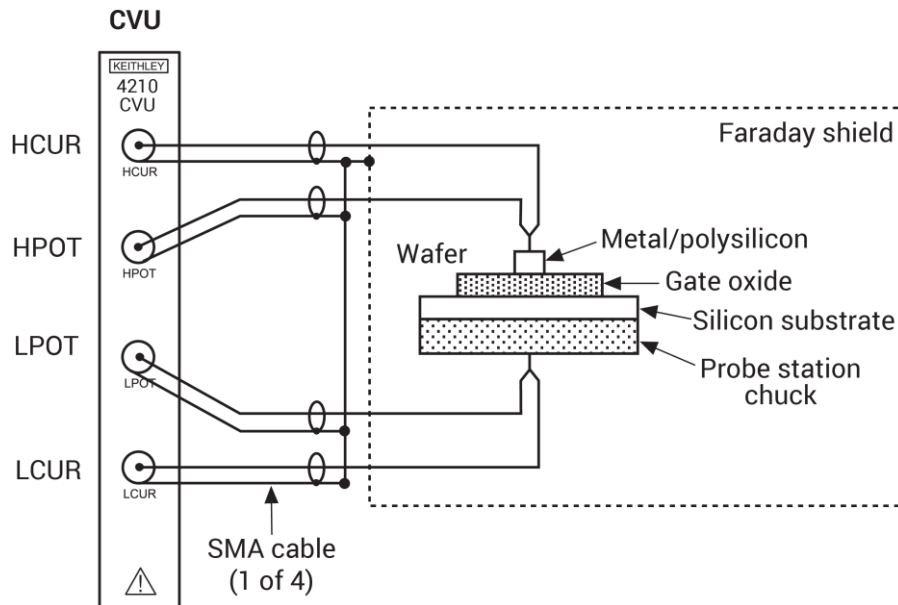
moscap-lifetime formulas and constants

Tests in this project use the same formulas as the ones for the `cvu-moscap` project. It also uses additional formulas (used by the `gni-w-wf` test) and user-defined constants, which are summarized in the following tables. The formulas and constants are set from the Formulator for the tests.

Note that results of the C_{OX}, C_{MIN}, and N_{AVG} formulas (used by the `c-v` test) are needed for the `gni-w-wf` test. You must manually input the results into the Formulator for the `gni-w-wf` test.

When configuring the project, you must input the area of the gate (in units of cm^2) and the dope type (-1 for P-type, 1 for N-type) of the device into the Constants area of the Formulator.

Zerbst analysis requires two types of data: C-V and C-t. Important data taken from the C-V measurement includes C_{OX}, C_{MIN}, and doping concentration (N_{AVG} and N_{BULK}). The results of the C-V analysis are integrated with data taken during a C-t measurement to compute generation velocity and generation lifetime of electron-hole pairs. These two parameters are computed from the slope and y-axis intercept of the graph of G/nI vs. w-w$_F$ as outlined in the following computation information.

$$G \,/\, n_I = -\,\varepsilon_S\, A N_{AVG}\, C_{OX} \bullet \left[\frac{\dfrac{1}{C^2_{t(i+1)}} - \dfrac{1}{C^2_{t(i-1)}}}{n_I t_{int}}\right] \bullet \left(\frac{1\times10^{12}}{2}\right)$$

Where:

- G = generation rate (s^{-1})

- ε_S = permittivity of semiconductor (F/cm)

- A = gate area (cm^2)

- N_{AVG} = average doping concentration (cm^{-3})

- C_{OX} = oxide (maximum) capacitance (pF)

- $C_{t(i+1)}$ = (i+1) value of measured C-t capacitance (pF)

- $C_{t(i-1)}$ = (i-1) value of measured C-t capacitance (pF)

- n_I = intrinsic carrier concentration (cm^{-3})

- t_{int} = time interval between C-t measurements (s)

- i = [2, #Rdgs-1]

w - wF computation

$$w - w_F = 1\times10^{12}\varepsilon_S A\left(\frac{1}{C_{ti}} - \frac{1}{C_{OX}}\right) - w_F$$

$$w_F = 1\times10^{12}\,\varepsilon_S\, A\left(\frac{1}{C_{ti}} - \frac{1}{C_{OX}}\right)$$

Where:

- w = depletion depth (cm)

- w_F = equilibrium inversion depth (cm)

- ε_S = permittivity of semiconductor (F/cm)

- A = gate area (cm^2)

- C_{ti} = i(th) value of measured C-t capacitance (pF)

- C_{MIN} = equilibrium minimum capacitance (pF)

The generation lifetime, τ_G, is equal to the reciprocal of the slope of the linear portion of the Zerbst plot, while the generation velocity, s, is the y-axis (G/n$_I$) intercept of the same linear section of the Zerbst plot.

Formula: GNI

Formula name: GNI (G/ni)

Units: s^{-1}

Description: Generation rate.

Formulator entry:

GNI = -(ES*AREA*NAVG*COX)*DIFF(MAVG(1/CP^2, 5), TIME)/NI

Simplified equation:

$$\frac{G}{ni} = \frac{\varepsilon_S A N_{AVG} C_{OX}}{2} \left[\frac{\dfrac{1}{C_{t(i+1)}^2} - \dfrac{1}{C_{t(i-1)}^2}}{n_i t_{int}} \right]$$

Where:

- G = generation rate (s^{-1})

- ε_S = permittivity of semiconductor (F/cm)

- A = gate area (cm^2)

- N_{AVG} = average doping concentration (cm^{-3})

- C_{OX} = oxide (maximum) capacitance (pF)

- $C_{t(i+1)}$ = (i+1) value of measured C-t capacitance (pF)

- $C_{t(i-1)}$ = (i-1) value of measured C-t capacitance (pF)

- n_I = intrinsic carrier concentration (cm^{-3})

- t_{int} = time interval between C-t measurements (s)

- i = [2, #Rdgs-1]

Formula: WF

Formula name: WF (WF)

Units: cm

Description: Equilibrium inversion depth.

Formulator entry:

WF = ES*AREA*(1/MIN(CP_GB)-1/COX)

Simplified equation:

$$w_F = \varepsilon_S A \left(\frac{1}{C_{MIN}} - \frac{1}{C_{OX}} \right)$$

Formula: WWF

Formula name: WWF (W-WF)

Units: cm

Description: Depletion depth (W-WF computation).

Formulator entry:

WWF = ES*AREA*(1/CP_GB-1/COX)-WF

Simplified equation:

$$W - W_F = \varepsilon_S A \left(\frac{1}{C_{ti}} - \frac{1}{C_{OX}} \right) - W_F$$

Constants

Constant	Default value	Units	Description
AREA	0.010404	cm^2	Gate area of device
DOPETYPE	1	none	1 = P-type, -1 = N-type
EBG	1.12	eV	E_{BG} - Semiconductor energy gap
EOX	3.4e-13	F / cm	ε_{OX} - Permittivity of oxide
ES	1.03e-12	F / cm	ε_S - Semiconductor permittivity
NI	1.45e+010	cm^{-3}	N_I - Intrinsic carrier concentration
TEMP	300	K	Test temperature
WM	4.15	V	W_M - Metal work function
WS	4.05	V	W_S - Silicon electron affinity

c-v test

This test generates a C-V sweep on a MOS capacitor and derives C_{OX}, C_{MIN}, and N_{AVG}. These parameters are input into the MOS Capacitor Zerbst C-t Sweep (C-t) test and the MOS Capacitor Generation Rate versus Depletion Depth (GNI_W-WF) test using the Formulator.

c-v Analyze sheet

Test data is displayed in the Analyze sheet:

- Cp_GB: Measured parallel capacitance.
- Gp_GB: Measured conductance.
- DCV_GB: Forced dc bias voltage.
- F_GB: Forced test frequency.
- Formulas: Formulator calculation results.

NOTE

GB = Gate-to-bulk.

c-t test

This test drives a MOS capacitor into accumulation by applying a negative hold voltage for a period (hold time). The bias voltage is then reversed to drive the capacitor into depletion. While in depletion, a series of capacitance measurements are made at a set time interval. The capacitance versus time measurements are plotted on a graph.

When configuring the test, you need to set the dc bias hold voltage (for accumulation) and the dc bias voltage level (for depletion). You also set the hold time for the bias hold voltage (in accumulation).

c-t Analyze sheet

The test data is displayed in the Analyze sheet:

- Time: Timestamp for each measurement.

- Cp_GB: Measured parallel capacitance.

- Gp_GB: Measured conductance.

- DCV_GB: Forced dc bias voltage.

- F_GB: Forced test frequency.

- CVU1S: Status code for each measurement. Rows highlighted in blue indicate a fault. For details, refer to "Measurement status" in the *Model 4200A-SCS Clarius User's Manual*.

- Formulas: Formulator calculation results.

NOTE

GB = Gate-to-bulk.

gni-w-wf test

This test is similar to the $c-t$ test because it creates a Zerbst plot by biasing the device in accumulation for a specified period. However, it calculates the generation rate (GN_I) and the depletion depth (WW_F) for every measurement, and then generates a GN_I versus WW_F Zerbst plot.

This test creates a Zerbst plot by first biasing the device in accumulation for a specified period. At time = 0, the polarity of the bias voltage is reversed to drive the device into deep depletion. While holding this bias, the capacitance is measured as a function of time. As more minority carriers are generated, the measured capacitance will rise. Eventually it will reach the minimum capacitance on the standard C-V curve. From both the C-t and the C-V data, the generation rate (G/n_i) is plotted as a function of depletion depth ($w-w_F$). You must manually input the values of C_{OX}, C_{MIN}, and N_{AVG} taken from the cv test into the Formulator in order to calculate the generation rate and depletion depth. Note that a known value of N_{AVG} can be input into the Formulator instead.

Once G/n_i versus $w-w_F$ is plotted, a linear line fit is applied to the graph. The generation lifetime (τ_G) is the reciprocal of the slope of the linear fitted region of the graph. The surface generation velocity (s_G) is the y-axis (G/n_i) intercept of the same linear section of the Zerbst plot.

The generation rate is calculated as follows:

$$\frac{G}{ni} = \frac{\varepsilon_S A N_{AVG} C_{OX}}{2} \left[\frac{\dfrac{1}{C^2_{t(i+1)}} - \dfrac{1}{C^2_{t(i-1)}}}{n_i t_{int}} \right]$$

Where:

- G/n_i = generation rate (s^{-1})

- ε_S = permittivity of the substrate material (F/cm)

- A = gate area (cm^2)

- N_{AVG} = average doping concentration (cm^{-3})*

- C_{OX} = oxide capacitance (F)

- $C^2_{t(i+1)}$ = (i+1) value of measured C-t capacitance (F)

- $C^2_{t(i-1)}$ = (i-1) value of measured C-t capacitance (F)

- n_i = intrinsic carrier concentration (cm^{-3})

- t_{int} = time interval between C-t measurements (s)

*N_{AVG} is calculated (with the result placed in the Analyze sheet) when the C-V test is run. The value for this parameter must be input into the Formulator for the `gni-w-wf` test. You can input a known value of N_{AVG} into the Formulator instead.

The equilibrium inversion depth (w_F) is calculated as:

$$w_F = \varepsilon_S A \left(\frac{1}{C_{MIN}} - \frac{1}{C_{OX}} \right)$$

Where:

- w_F = equilibrium inversion depth (cm)

- ε_S = permittivity of the substrate material (F/cm)

- A = gate area (cm^2)

- C_{MIN} = Minimum oxide capacitance (F)*

- C_{OX} = Oxide capacitance (F)*

*C_{MIN} and C_{OX} are calculated (with the results placed in the Analyze sheet) when the C-V test is run. The values for these parameters must be input into the Formulator for the `gni-w-wf` test.

The depletion depth is calculated from the following equation:

$$w - w_F = \varepsilon_s A \left(\frac{1}{C_{ti}} - \frac{1}{C_{OX}} \right) - w_F$$

Where:

- w = depletion depth (cm)

- w_F = equilibrium inversion depth (cm)

- ε_s = permittivity of the substrate material (F/cm)

- A = gate area (cm^2)

- C_{ti} = i(th) value of measured C-t capacitance (F)

- C_{OX} = oxide capacitance (F)*

*C_{OX} is calculated (with the result placed in the Analyze sheet) when the C-V test is run. The value for this parameter must be input into the Formulator for the `gni-w-wf` test.

One of the perplexing parts of the Zerbst method is to determine how to space the capacitance measurements. Capacitance measurement spacing almost entirely depends on how fast minority carriers can be generated. The interval time for the measurements can be adjusted depending on the device.

gni-w-wf test procedure

1. Run the C-V test.
2. Get the calculation results for the C_{OX}, C_{MIN} and N_{AVG} formulas from the Analyze sheet.
3. Input the values for C_{OX}, C_{MIN}, and N_{AVG} into the Formulator for the `gni-w-wf` test (for example, C_{OX} = 145E-12).
4. Run the `gni-w-wf` test to generate the Zerbst plot.

NOTE

If the value for the N_{AVG} in the Formulator is known, it can be used instead of the one derived from the C-V test.

gni-w-wf Analyze sheet

Test data is displayed in the Analyze sheet:

- Time: Timestamp for each measurement.
- Cp_GB: Measured parallel capacitance.
- Gp_GB: Measured conductance.
- DCV_GB: Forced dc bias voltage.
- F_GB: Forced test frequency.
- CVU1S: Status code for each measurement. Rows highlighted in blue indicate a fault. For details, refer to "Measurement status" in the *Model 4200A-SCS Clarius User's Manual*.
- Formulas: Formulator calculation results.

NOTE
GB = Gate-to-bulk.

MOS Capacitor Mobile Ion Project (moscap-mobile-ion)

Mobile ions can present a severe reliability issue in metal-oxide semiconductor (MOS) structures. These mobile charges in MOS capacitors are mainly due to ionic impurities, such as Na+, which can drift across the oxide and affect the device performance. One technique for determining the amount of mobile charge in the oxide of a MOS capacitor is the bias temperature stress (BTS) method. Using this method, the flatband voltage (*Vfb)* is used to determine the amount of charge. The flatband voltage is measured both at room temperature and after the device has been at an elevated temperature for enough time for the charges to be mobile. The difference in the flatband voltage is related to the mobile charge as follows:

$$Q_m = -\Delta V_{fb} C_{ox}$$

Where:

- Q_m = mobile ion charge (C)
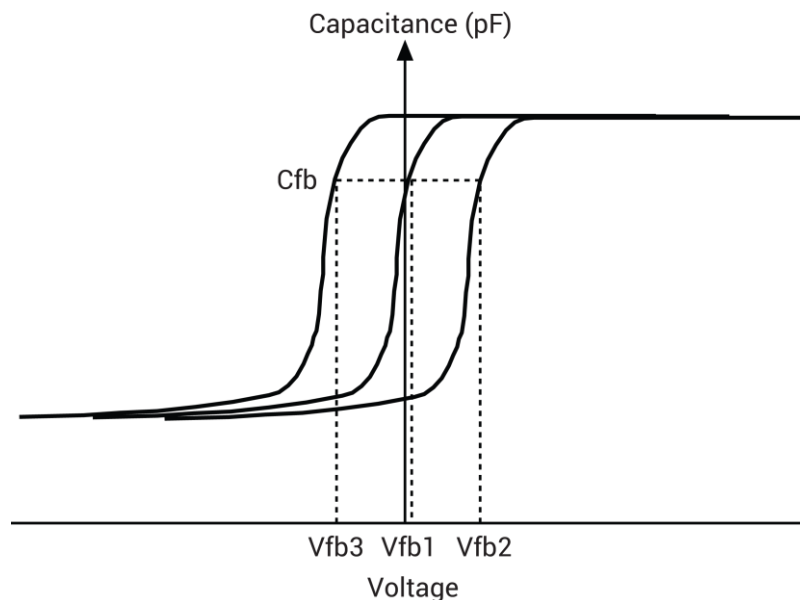- V_{fb} = flatband voltage (V)
- C_{OX} = oxide capacitance (F)

This semi-automatic project is executed from the subsite level. The oxide thickness and flatband voltage extracted from the data in the tests are sent to the subsite level Analyze sheet after the tests are executed. The calculated value of the mobile ion charge and concentration can be found in the Calc tab of the subsite Analyze sheet.

Before executing this test, you need to input the gate area of the device into the Constants area of the Formulator for the `CV-Vfb1`, `CV-Vfb2`, and `CV-Vfb3` test modules. Also, in the `CV-Vfb1` test, you must update the gate area in the formula area of the Formulator. The gate area formula to update is called `AREA_GATE` and is used in the calculation of the mobile ion charge in the subsite Calc sheet.

Basic testing involves the following steps:

1. **At room temperature, generate a C-V sweep on the MOS capacitance.** From the C-V data, extract the flatband capacitance (C_{fb}), flatband voltage ($V_{fb}1$), and the oxide capacitance (C_{OX}). The device should be measured on a hot chuck in a dark box. The dark box prevents static noise problems that can affect the C-V measurements.

2. **Apply dc bias voltage and temperature stress.** A gate voltage of approximately 1 MV/cm of dielectric thickness is applied across the device to drive the mobile ions to the interface. A thermal chuck is used to temperature-stress at a temperature in the range of 150 °C to 300 °C, depending on the type of ions. Typical temperature stress time is around five to 10 minutes. The device is cooled to room temperature with the bias voltage applied. Mobile charges will be trapped near the metal-oxide interface.

3. **Repeat the C-V sweep on a cooled sample and again extract the flatband voltage** ($V_{fb}2$)**.** If there are mobile charges in the oxide, the flatband voltage will be different from the first one.

4. **The sample is heated again, but the opposite polarity dc bias voltage is applied to the sample.** This causes the mobile charges to be driven toward the oxide-silicon interface. Again, the sample is cooled while the dc bias voltage is applied.

5. **Repeat the C-V sweep on the cooled sample and derive the flatband voltage** ($V_{fb}3$)**.** Since mobile charges are concentrated on the opposite interface, this flatband voltage will be different from the first and second measurements. This shift in the flatband voltage is illustrated in the following figure.

Figure 72: Flatband voltage shift caused by mobile charges in the oxide

6.   The mobile ion charge is calculated as follows:

$$Q_m = \frac{|V_{fb3} - V_{fb2}| C_{OX}}{A}$$

Where:

- Q_m = mobile ion charge (C)
- V_{fb2} = flatband voltage measured second time after temperature stress (V)
- V_{fb3} = flatband voltage measured third time with opposite bias polarity (V)
- C_{OX} = oxide capacitance (F)
- A = gate area (cm^2)

The mobile ion concentration is related to the mobile ion charge through the following equation:

$$N_{mi} = \frac{Q_m}{q}$$

Where:

- N_{mi} = mobile ion concentration
- Q_m = mobile ion charge (C)
- q = electron charge

moscap-mobile-ion connections

The following figure shows the basic test configuration. Refer to CVU connections (on page 2-1) for details on connections to a semiconductor wafer. Only use the supplied (red), same length 100 Ω SMA cables for connections to the 4210-CVU or 4215-CVU.

NOTE

After making or changing connections, be sure to use the CVU Confidence Check diagnostic tool and do connection compensation tests. Refer to Run an open check and short check (on page 2-17) and Connection compensation (on page 2-8) for details.

Figure 73: Basic configuration for mobile ion testing
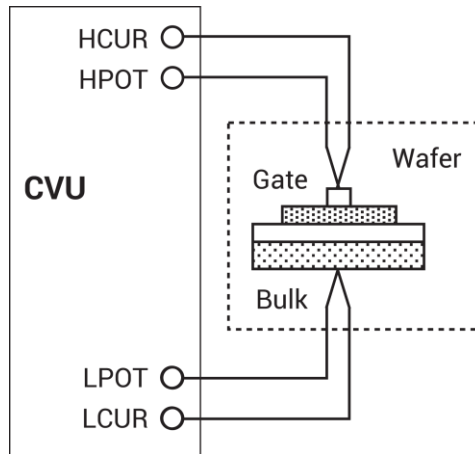
Formulas and constants

This project uses formulas and constants that are used by the `cvu-moscap` project. The formulas and constants are summarized in [cvu-moscap project formulas](#) (on page 4-26).

The `cv-vfb1` test also uses the following formula for gate area:

AREA_GATE = 2

Run the subsite

This semi-automatic test is executed from the `mobileion` subsite in the project. The test is run from this subsite because the oxide thickness and flatband voltage extracted from the data in the tests is sent to the subsite Analyze sheet after the tests are executed. The calculated value of the mobile ion charge and concentration is shown in the Calc tab of the Analyze sheet for the subsite.

Before executing this subsite, you need to input the gate area of the device into the Constants tab of the Formulator for the `cv-vfb1`, `cv-vfb2`, and `cv-vfb3` test modules. Also, for the `cv-vfb1` test, you must also update the `AREA_GATE` formula in the Formulator. This formula is used in the calculation of the mobile ion charge in the subsite Calc sheet.

This project must be run from the `mobileion` subsite level.

cv-vfb1 test

This test performs a C-V sweep on the MOS capacitor and extracts flatband capacitance, flatband voltage, and oxide capacitance. The oxide capacitance and the flatband voltage are sent to the Analyze sheet of the subsite. To view the values that are used in the mobile ion calculation, select the Calc tab in the subsite Analyze sheet.

cv-vfb1 Analyze sheet

The test data is displayed in the Analyze sheet:

- Time: Timestamp for each measurement (if Report Timestamps is selected).
- Cp_GB: Measured parallel capacitance.
- Gp_GB: Measured conductance.
- DCV_GB: Forced dc bias voltage.
- F_GB: Forced test frequency.
- Formulas: Formulator calculation results.

If rows are highlighted in blue, a fault occurred. For details, refer to "Measurement status" in the *Model 4200A-SCS Clarius User's Manual*.

NOTE

GB = Gate-to-bulk.

bias-pos test

This test applies a positive dc bias voltage to the MOS capacitor. The voltage continues to be applied as the device under test (DUT) is heated in the next action, `hotchuck`.

No graph is generated for this test.

Formulator formulas and constants

Formulas are not used for this test.

bias-pos Analyze sheet

The test data is displayed in the Analyze sheet:

- Time: Timestamp for each measurement.
- Cp_GB: Measured parallel capacitance.
- Gp_GB: Measured conductance.
- DCV_GB: Forced dc bias voltage.
- F_GB: Forced test frequency.
- CVU1S: Status code for each measurement. Rows highlighted in blue indicate a fault. For details, refer to "Measurement status" in the *Model 4200A-SCS Clarius User's Manual*.

NOTE

GB = Gate-to-bulk.

hotchuck action

This action prompts you to turn on the hot chuck to a specified temperature and then to cool down the sample. After the temperature stress, select **OK** to generate the C-V sweep in the following test. The bias voltage is output until you select **OK**.

cv-vfb2 test

This test performs a C-V sweep on the sample after it has been heated and then cooled. The oxide capacitance and the flatband voltage (V_{FB}) are sent to the Analyze sheet for the subsite. Select the Calc tab of the Analyze sheet to review the values that are used in the mobile ion calculation.

cv-vfb2 Analyze sheet

The test data is displayed in the Analyze sheet:

- Time: Timestamp for each measurement (if Report Timestamps is selected).
- Cp_GB: Measured parallel capacitance.
- Gp_GB: Measured conductance.
- DCV_GB: Forced dc bias voltage.
- F_GB: Forced test frequency.
- Formulas: Formulator calculation results.

If rows are highlighted in blue, a fault occurred. For details, refer to "Measurement status" in the *Model 4200A-SCS Clarius User's Manual*.

NOTE

GB = Gate-to-bulk.

bias-neg test

This test applies a negative dc bias voltage to the MOS capacitor. The voltage continues to be applied to the sample as the DUT is heated in the next test module, `hotchuck`.

Formulator formulas and constants

Formulas are not used for this test.

bias-neg Analyze sheet

The test data is displayed in the Analyze sheet:

- Time: Timestamp for each measurement.

- Cp_GB: Measured parallel capacitance.

- Gp_GB: Measured conductance.

- DCV_GB: Forced dc bias voltage.

- F_GB: Forced test frequency.

- CVU1S: Status code for each measurement. Rows highlighted in blue indicate a fault. For details, refer to "Measurement status" in the *Model 4200A-SCS Clarius User's Manual*.

NOTE
GB = Gate-to-bulk.

hotchuck action

This action prompts you to turn on the hot chuck to a specified temperature and then to cool down the sample. After the temperature stress, select **OK** to generate the C-V sweep in the following test. The bias voltage is output until you select **OK**.

cv-vfb3 test

This test performs a C-V sweep on the sample after it has been heated and then cooled. The oxide capacitance and the flatband voltage (V_{fb}) are sent to the Analyze sheet for the subsite. View the Calc tab in the Analyze sheet to review the values that are used in the mobile ion calculation.

To open the Calc sheet for the subsite:

1. In the project tree, select **mobileion**.
2. Select **Analyze**.
3. Select the **Calc** tab.

Figure 74: Calc sheet for the subsite level (Mobilelon)

cv-vfb3 Analyze sheet

The test data is displayed in the Analyze sheet:

- Time: Timestamp for each measurement (if Report Timestamps is selected).

- Cp_GB: Measured parallel capacitance.

- Gp_GB: Measured conductance.

- DCV_GB: Forced dc bias voltage.

- F_GB: Forced test frequency.

- Formulas: Formulator calculation results.

If rows are highlighted in blue, a fault occurred. For details, refer to "Measurement status" in the *Model 4200A-SCS Clarius User's Manual*.

NOTE
GB = Gate-to-bulk.

MOSFET 3-Terminal C-V Tests Using the 4200A-CVIV Bias Tees (mosfet-cviv-cv-bias-tees and mosfet-cviv-cv-bias-tees-400V)

This project contains test modules that perform high-voltage C-V measurements in the off-state on a 3-terminal, n-channel MOSFET. The mosfet-cviv-cv-bias-tees-400V test lets you make C-V measurements up to 400 V.

The tests in this project include:

- MOSFET Capacitance Gate-Source (`cgs`): Measures capacitance between the gate and source of a MOSFET while an SMU sweeps dc voltage at the drain. This test uses the CVIV bias tees.

- MOSFET Capacitance Drain-Source (`cds`): Measures capacitance between the drain and source of a MOSFET while an SMU sweeps dc voltage at the drain. This test uses the CVIV bias tees.

- MOSFET Reverse Transfer Capacitance (`crss`): Measures reverse transfer capacitance of a MOSFET while an SMU sweeps dc voltage at the drain. This test uses the CVIV bias tees.

- MOSFET Input Capacitance (`ciss`): Measures input capacitance of a MOSFET while an SMU sweeps dc voltage at the drain. This test uses the CVIV bias tees.

- MOSFET Output Capacitance (`coss`): Measures output capacitance of a MOSFET while an SMU sweeps dc voltage at the drain. This test uses the CVIV bias tees.

For additional information on high-voltage measurements, refer to *Application Note: Using the 4200A-CVIV Multi-Switch to Make High Voltage and High Current C-V Measurements.*

MOSFET I-V and C-V Tests Using 4200A-CVIV Multi-Switch Project (mosfet-cviv)

This project demonstrates how you can use a 4200A-CVIV Multi-Switch to automate I-V and C-V testing of a MOSFET. When the project is run, the 4200A-CVIV connects four SMUs to the MOSFET. The SMUs perform I-V tests on the MOSFET. The 4200A-CVIV then connects the CVU to the MOSFET. The CVU measures the gate to drain/source/bulk capacitance as a function of the dc voltage.

MOSFET Project (mosfet)

This project contains dc I-V, C-V, and pulse I-V tests for a MOSFET. It makes C-V measurements to explore the basic operation and parameters of the device. Since the high-frequency operation and switching speed of a MOSFET are dependent on the capacitance of the device, capacitance measurements are often made to various parts of the device. For example, the capacitance between the gate and channel (C_{GD} and C_{GS}) is important because it creates the charges necessary for

operating the devices. This gate-channel capacitance depends on the applied voltage and the operating region.

Capacitance measurements are made to various parts of the device, as shown in the following figure.

Figure 75: N-MOSFET with terminal capacitances
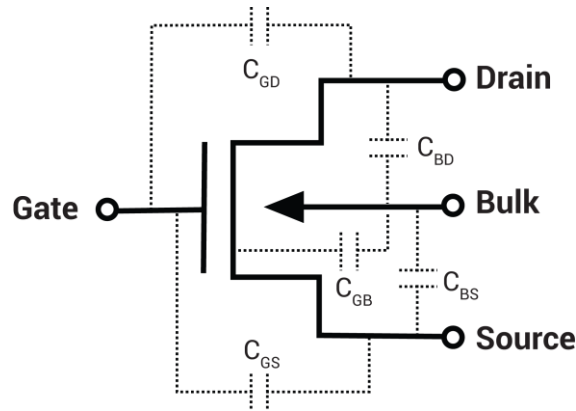
C-V measurements are often made on MOSFETs to extract particular device parameters, such as oxide capacitance (C_{OX}), flatband capacitance (C_{FB}), and oxide thickness (T_{OX}).

The `g-to-sdb` test generates a capacitance versus voltage graph. It plots the capacitance as a function of the gate voltage from the two-terminal measurement. A typical two-terminal C-V curve of an N-channel MOSFET is shown in the following figure.

Figure 76: N-channel MOSFET g-to-sdb graph
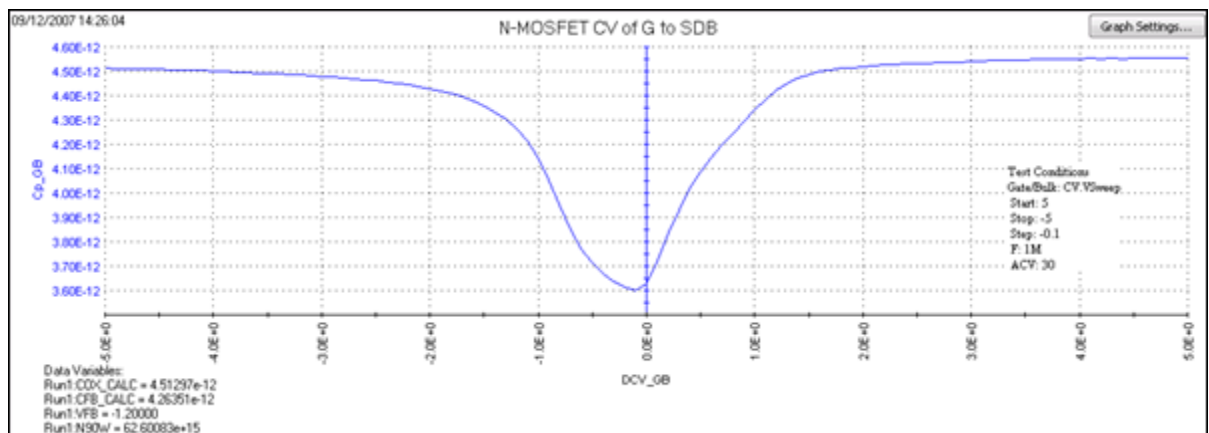
Notice from the high frequency curve that when the device is in the inversion region, the capacitance is high, unlike the MOS capacitor, which has low capacitance in inversion. This is because the MOSFET has a source and drain, which enables inversion charge to flow, unlike the MOS capacitor, which relies on generation and recombination in the bulk region.

The oxide capacitance (C_{OX}) is usually set to the maximum capacitance in accumulation, and is calculated by the C_{OX} formula in the Formulator.

Oxide thickness is calculated by the T_{OX} formula in the Formulator.

The `mosfet-dopingprofile` test performs a C-V sweep on the two-terminal MOSFET. It generates a doping concentration versus depletion depth graph. The doping concentration (*N*) is calculated and plotted as a function of depletion depth. Depletion depth is calculated by the DEPTHM formula in the Formulator.

Doping density is calculated from the measured capacitance and the voltage. It is calculated by the NDOPING formula in the Formulator.

mosfet connections

The following figure shows the basic test configuration for MOSFET testing (for details, see CVU connections (on page 2-1)). As shown, 2-wire sense connections are used with the source, drain, and bulk terminals tied together. Use only the supplied CA-446A or CA-447A red 100 Ω SMA cables for connections to the 4210-CVU or 4215-CVU. Use SMA cables that are the same length.

NOTE

After making or changing connections, be sure to use the CVU Confidence Check diagnostic tool and do connection compensation tests. Refer to Run an open check and short check (on page 2-17) and Connection compensation (on page 2-8) for details.

Figure 77: Two-terminal C-V test configuration for a MOSFET
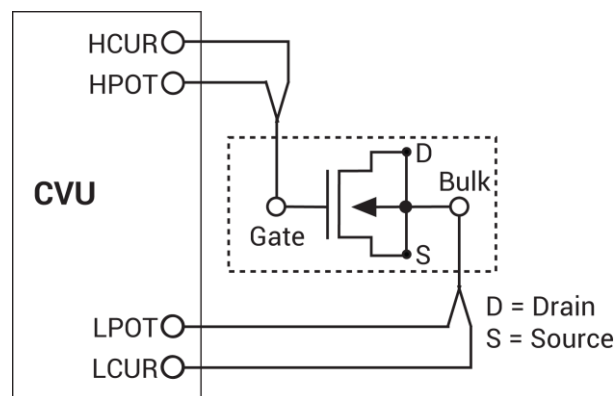
mosfet formulas and constants

Formulas and user-defined constants that are used for the application tests are summarized (in alphabetical order) in the next topics. The formulas and constants are set from the Formulator settings for the tests.

Formula: AR

Formula name: AR (*aR*)

Units: None

Description: Intermediate parameter for calculation of corrected capacitance.

Formulator entry:

AR = GP_GB-(GP_GB^2 + (2*PI*F_GB*CP_GB)^2)*RS

Simplified equation:

$$a_R = G - \left(G^2 + (2\pi f C)^2 R_s\right)$$

Formula: CADJ

Formula name: CADJ (*CADJ*)

Units: F

Description: Corrected capacitance by compensating series resistance.

Formulator entry:

CADJ = ((GP_GB^2 + (2*PI*F_GB*CP_GB)^2)*CP_GB)/(AR^2 +(2*PI*F_GB*CP_GB)^2)

Simplified equation:

$$C_{ADJ} = \frac{(G^2 + (2\pi f C)^2)C}{a_R^2 + 2\pi f C^{\ 2}}$$

Formula: CFB_CALC

Formula name: CFB_CALC (*CFB*)

Units: F

Description: Flatband capacitance.

Formulator entry:

CFB_CALC = (COX_CALC*ES*AREA/(DEBYEM*1E2))/(COX_CALC+(ES*AREA/(DEBYEM*1E2)))

Simplified equation:

$$C_{FB} = \frac{C_{OX}\left(\frac{\varepsilon_S A}{\lambda}\right)\left(1 \times E^2\right)}{C_{OX} + \left(\frac{\varepsilon_S A}{\lambda}\right)\left(1 \times E^2\right)}$$

Formula: DEBYEM

Formula name: DEBYEM (λ)

Units: m

Description: Debye length (in meters).

Formulator entry:

DEBYEM = SQRT(ES*K*TEMP/(ABS(N90W)*Q^2))*1E-2

Simplified equation:

$$\lambda = \left(\frac{\varepsilon_S kT}{q^2 N_X}\right)^{1/2} (1 \times E^{-2})$$

Formula: DEPTHM

Formula name: DEPTHM (*W*)

Units: m

Description: Depletion depth (in meters).

Formulator entry:

DEPTHM = 1E-2*AREA*ES*(1/COND(POX,MINPOS(CADJ),SUBARRAY(CADJ, POX, MINPOS(CADJ)),SUBARRAY(CADJ, MINPOS(CADJ),POX))-1/COX_CALC))

Simplified equation:

$$W = A\varepsilon_S \left(\frac{1}{C} - \frac{1}{C_{OX}}\right) (1 \times E^{-2})$$

Where:

- W = depletion depth (m)
- A = gate area (cm^2)
- εs = permittivity of the substrate material (F/cm)
- C = measured capacitance (F)
- C_{OX} = oxide capacitance (F)
- $1 \times E^{-2}$ = units conversion from cm to m

Formula: INVCSQR

Formula name: INVCSQR

Units: $1/F^2$

Description: Inverse square of capacitance.

Formulator entry:

INVCSQR = 1/CADJ^2

Simplified equation:

$$INVCSQR = \frac{1}{C^2}$$

Formula: N90W

Formula name: N90W

Units: None

Description: Doping density at 90% of maximum depletion depth.

Formulator entry:

N90W = AT(NDOPING, FINDD(DEPTHM, 0.9*MAX(DEPTHM), 2))

Formula: NDOPING

Formula name: NDOPING (N)

Units: $1/cm^3$

Description: Doping density.

Formulator entry:

NDOPING = ABS((-2)/(AREA^2*Q*ES)/(DELTA(COND(POX,MAXPOS(INVCSQR), SUBARRAY(INVCSQR, POX, MINPOS(CADJ)),SUBARRAY(INVCSQR, MINPOS(CADJ),POX)))/DELTA(DCV_GB)))

Simplified equation:

$$N(W) = \frac{2}{q\varepsilon_S A^2 \left[\dfrac{d\left(\dfrac{1}{C^2}\right)}{dV} \right]}$$

Formula: PHIB

Formula name: PHIB (φ_B)

Units: V

Description: Bulk potential.

Formulator entry:

PHIB = (-1)*K*TEMP/Q*LN(ABS(N90W)/NI)*DOPETYPE

Simplified equation:

$$\phi_B = \frac{kT}{q} \, Ln\left(\frac{N_{BULK}}{N_i}\right) (DopeType)$$

Formula: RS

Formula name: RS (*RS*)

Units: Ω

Description: Series resistance calculated from capacitance.

Formulator entry:

RS = (AT(GP_GB/((2*PI*F_GB)*CP_GB),POX))^2/((1+(AT(GP_GB/ ((2*PI*F_GB)*
CP_GB),POX))^2)*(AT(GP_GB,POX)))

Simplified equation:

$$R_S = \frac{\left(\frac{G}{2\pi fC}\right)^2}{\left[1+\left(\frac{G}{2\pi fC}\right)^2\right] G}$$

Formula: TOXNM

Formula name: TOXNM (*TOX*)

Units: nm

Description: Calculated thickness of oxide.

Formulator entry:

TOXNM = (1E7*AREA*EOX)/COX_CALC

Simplified equation:

$$T_{OX} = \left(\frac{A\varepsilon_{OX}(1xE^7)}{C_{OX}} \right)$$

Where:

- T_{OX} = oxide thickness (nm)
- A = gate area (cm^2)
- ε_{OX} = permittivity of the oxide material (F/cm)
- C_{OX} = oxide capacitance (F)
- 1 x E^7 = units conversion from cm to nm

Formula: VFB

Formula name: VFB (*VFB*)

Units: V

Description: Flatband voltage. Once CFB (*CFB*) is derived, *VFB* is interpolated from the closest *VGS* values.

Formulator entry:

VFB = AT(DCV_GB,POSVFB)

Constants for the mosfet project

Constant	Default Value	Units	Description
AREA	0.00012	cm^2	Gate area of device
DOPETYPE	1	none	1 = P-type, -1 = N-type
EOX	3.4e-013	F/cm	ε_{OX} - Permittivity of oxide
ES	1.04e-12	F/cm	ε_S - Semiconductor permittivity
Q	1.60218e-019	C	Charge on an electron
TEMP	293	K	Test temperature

g-to-sdb and mosfet-dopingprofile Analyze sheet

The test data is displayed in the Analyze sheet:

- Cp_GB: Measured parallel capacitance.

- Gp_GB: Measured conductance.

- DCV_GB: Forced dc bias voltage.

- F_GB: Forced test frequency.

- Formulas: Formulator calculation results.

NOTE

GB = Gate to bulk.

Solar Cell Project (solarcell)

To determine the electrical characteristics of a photovoltaic (PV) cell, a 4200-SMU or 4201-SMU and 4210-CVU or 4215-CVU are used to perform I-V, C-V, and C-F sweeps. Graphs are generated from the collected current, capacitance, frequency, and voltage data.

Formulator calculations are made to determine the following electrical characteristics of the PV cell:

- **I-V testing:** The Formulator calculates power (P), current (CURR), maximum power (PMAX), maximum current (IMAX), maximum voltage (VMAX), short-circuit current (ISC), open-circuit voltage (VOC), and fill factor (FF).

- **C-V testing:** The Formulator calculates inverse capacitance (INV_C) and the doping density (N).

I-V testing generates the following graphs:

- Current versus voltage graph for a forward-biased PV cell. Formulator formulas calculate the electrical characteristics of the cell.

- Current versus voltage graph for a reversed-biased PV cell.

C-V testing generates the following graphs:

- Capacitance versus voltage graph for a reversed-biased PV cell.

- A $1/C^2$ (inverse capacitance) and capacitance versus voltage graph for a PV cell. $1/C^2$ and doping density are calculated by the Formulator.

- Capacitance versus frequency graph.

The testing process is typically repeated using different light intensities and temperature conditions.

solarcell connections

The next figures show the basic test configurations for this project:

- **I-V testing**: The basic configuration shows four-wire sensing using a 4200-SMU, 4201-SMU, 4210-SMU, or 4211-SMU. Four-wire sensing is needed to achieve optimum performance. See *Model 4200A-SCS Source-Measure Unit (SMU) User's Manual* for details on SMU connections.

- **C-V Testing**: See CVU connections (on page 2-1) for details on connections. Use only the supplied (red) 100 Ω SMA cables for connections to the 4210-CVU or 4215-CVU. Use SMA cables that are the same length.

NOTE

After making or changing connections, be sure to use the CVU Confidence Check diagnostic tool and do connection compensation tests. Refer to Run an open check and short check (on page 2-17) and Connection compensation (on page 2-8) for details.

Figure 78: Basic configurations to test PV cells for I-V testing
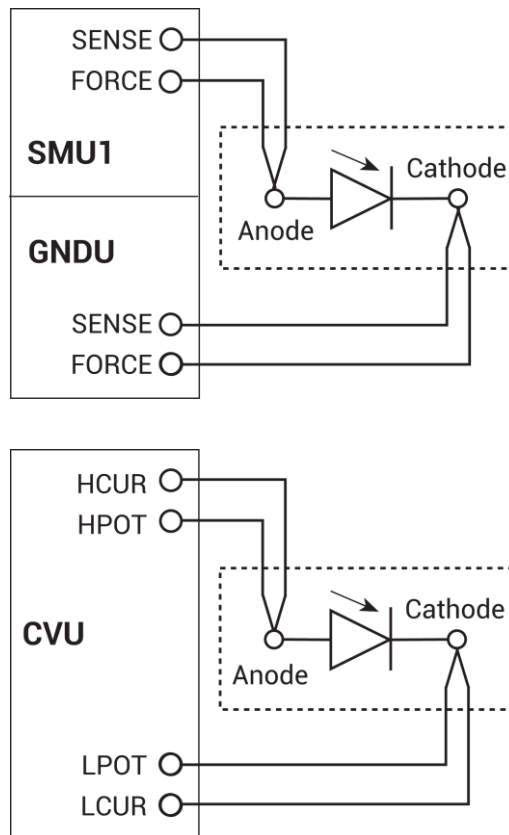
solarcell formulas and constants

Formulas and user-defined constants that are used for the tests are listed in alphabetical order in the next topics. The formulas and constants are set from the Formulator for the tests.

Formula: CURR

Formula name: CURR

Units: A

Description: PV cell current. The absolute value of the current output.

Formulator entry:

CURR = ABS(ANODEI)

Formula: FF

Formula name: FF

Units: None

Description: Fill factor.

Formulator entry:

FF = (IMAX*VMAX)/(ISC*VOC)

Simplified equation:

$$FF = \frac{I_{MAX}V_{MAX}}{I_{SC}V_{OC}}$$

Formula: IMAX

Formula name: IMAX

Units: A

Description: Cell current where the power output of the cell is greatest (PMAX).

Formulator entry:

IMAX = ABS(AT(ANODEI, MAXPOS(P)))

Formula: INV_C2

Formula name: INV_C2 (C)

Units: 1/F2

Description: Inverse capacitance.

Formulator entry:

INV_C2 = 1/CP_AC^2

Simplified equation:

$$C = \frac{1}{C^2}$$

Formula: ISC

Formula name: ISC (I_{SC})

Units: A

Description: Short circuit current. ISC is the point in I-V data where V = 0.

Formulator entry:

ISC = ABS(AT(ANODEI, FINDD(ANODEV, 0, FIRSTPOS(ANODEV))))

Formula: N

Formula name: N ($N_{(a)}$)

Units: 1/cm^3

Description: Doping density.

Formulator entry:

N = ABS(2/Q/ES/AREA^2/DIFF(INV_C2, DCV_AC))

Simplified equation:

$$N(a) = \cfrac{2}{\left| q\varepsilon_S A^2 \; \cfrac{d\left(\cfrac{1}{C^2}\right)}{dV} \right|}$$

Where:

- $N_{(a)}$ = doping density

- q = electron charge (C)

- E_s = semiconductor permittivity for silicon (F/cm)

- A = area (cm^2)

- C = measured capacitance (F)

- V = applied voltage (V)

Formula: P

Formula name: P

Units: W

Description: Power.

Formulator entry:

P = CURR*ANODEV

Simplified equation:

P = I x V

Where:

- I = Cell current

- V = Cell voltage

Formula: PMAX

Formula name: PMAX (P_{MAX})

Units: W

Description: Maximum power point.

Formulator entry:

PMAX = MAX(P)

Simplified equation:

$P_{MAX} = I_{MAX}$ x V_{MAX}

Formula: VMAX

Formula name: VMAX

Units: V

Description: Cell voltage where the power output of the cell is greatest (PMAX).

Formulator entry:

VMAX = AT(ANODEV, MAXPOS(P))

Formula: VOC

Formula name: VOC (V_{OC})

Units: V

Description: Open circuit voltage. VOC is the point in I-V data where I = 0.

Formulator entry:

VOC = AT(ANODEV, FINDU(ANODEI, 0, LASTPOS(ANODEI)))

Constants for the solarcell project

	Default value	Units	Description
AREA	8	cm^2	Gate area of device
ES	1.034e-12	F/cm	Semiconductor permittivity (ε_S)

fwd-ivsweep test

NOTE

Make sure the PV cell is connected to the SMU (see solarcell connections (on page 4-70)).

This test uses a 4200-SMU or 4201-SMU to perform a forward-biased voltage sweep on a PV cell. Current is measured on each step of the sweep. An I versus V graph is generated from the collected data. It also makes Formulator calculations to determine the electrical characteristics of the cell.

When the test is started, the SMU sweeps from −50 mV to 250 mV in 2 mV steps. A total of 151 current measurements are made.

fwd-ivsweep Analyze sheet

The test data is displayed in the Analyze sheet:

- AnodeI: Measured current.
- AnodeV: Forced voltage.
- Formulas: Formulator calculation results.

rev-ivsweep test

NOTE

Make sure the solar cell is connected to the 4200-SMU or 4201-SMU (see solarcell connections (on page 4-70)).

This test uses a SMU to perform a reversed-bias voltage sweep. Current is measured on each step of the sweep. An I (absolute value) versus V graph is generated from the collected data.

When the test is started, the SMU sweeps from 0 V to −600 mV in −5 mV steps. A total of 121 current measurements are made.

rev-ivsweep Analyze sheet

The test data is displayed in the Analyze sheet:

- AnodeI: Measured current.
- AnodeV: Forced voltage.

solarcell-cvsweep test

NOTE

Make sure the solar cell is connected to the 4210-CVU or 4215-CVU (see CVU connections (on page 2-1)).

This test uses a CVU to perform a capacitance voltage sweep on a solar cell. Capacitance is measured on each step of the sweep. A C versus V graph is generated from the collected data.

solarcell-cvsweep Analyze sheet

The test data is displayed in the Analyze sheet:

- Cp_AC: Measured parallel capacitance.
- Cp_AC: Measured conductance.
- DCV_AC: Forced dc bias voltage.
- F_AC: Forced test frequency.
- CVU1S: Status code for each measurement. Rows highlighted in blue indicate a fault. For details, refer to "Measurement status" in the *Model 4200A-SCS Clarius User's Manual*.

NOTE

AC = Anode to cathode.

solarcell-c-2vsv test

NOTE

Make sure the solar cell is connected to the 4210-CVU or 4215-CVU (see CVU connections (on page 2-1)).

This test uses a CVU to perform a capacitance-voltage sweep on a solar cell. Capacitance is measured on each step of the sweep. A graph ($1/C^2$ and C versus V) is generated from the collected data. The Formulator calculates $1/C^2$ and the doping density.

solarcell-c-2vsv Analyze sheet

The test data is displayed in the Analyze sheet:

- Cp_AC: Measured parallel capacitance.

- Gp_AC: Measured conductance.

- DCV_AC: Forced dc bias voltage.

- F_AC: Forced test frequency.

- CVU1S: Status code for each measurement. Rows highlighted in blue indicate a fault. For details, refer to "Measurement status" in the *Model 4200A-SCS Clarius User's Manual.*

- Formulas: Formulator calculation results.

NOTE

AC = Anode to cathode.

cfsweep test

NOTE

Make sure the PV cell is connected to the CVU (see CVU connections (on page 2-1)).

This test performs a frequency sweep, measuring capacitance at each frequency point, and then generates a C versus F graph.

cfsweep Analyze sheet

The test data is displayed in the Analyze sheet:

- Cp_AC: Measured parallel capacitance.

- Gp_AC: Measured conductance.

- DCV_AC: Forced dc bias voltage.

- F_AC: Forced test frequency.

- CVU1S: Status code for each measurement. Rows highlighted in blue indicate a fault. For details, refer to "Measurement status" in the *Model 4200A-SCS Clarius User's Manual.*

Interconnect Capacitance C-V Sweep test (cv-sweep)

Because the interconnect capacitance directly affects the speed and noise of an integrated circuit, making accurate capacitance measurements is very important. These measurements are usually measured between two metal pads on the wafer. The magnitude of capacitance is usually very small (<1 pF).

This test uses a voltage sweep to measure capacitance at every step of the sweep and generates a capacitance versus voltage graph. It also calculates noise.

This test module makes a C-V sweep. The measurements are set to Quiet mode because the measurements are very sensitive.

cv-sweep connections

The test configuration in the following figure shows the schematic representation of interconnect capacitance on a wafer. For details on connections to the wafer, see CVU connections (on page 2-1). Use only the supplied (red) 100 Ω SMA cables for connections to the 4210-CVU or 4215-CVU. Use SMA cables that are the same length.

NOTE

After making or changing connections, be sure to use the CVU Confidence Check diagnostic tool and do connection compensation tests. Refer to Run an open check and short check (on page 2-17) and Connection compensation (on page 2-8) for details.

Figure 79: Basic configuration to test interconnect capacitance
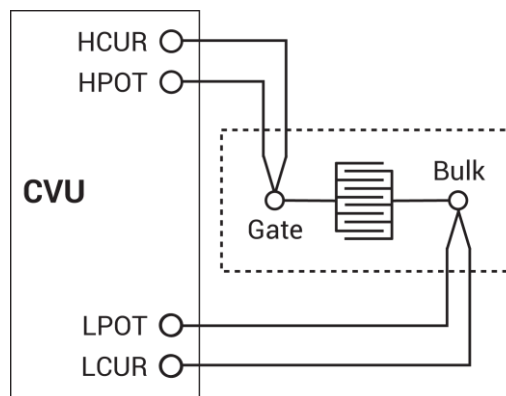
Formulas and constants

This project uses one formula (no constants):

- NOISE: Calculates the standard deviation of the capacitance measurements.
  NOISE = STDEV(CP_GB)

Analyze sheet

Test data is displayed in the Analyze sheet:

- Cp_GB: Measured parallel capacitance.

- Gp_GB: Measured conductance.

- DCV_GB: Forced dc bias voltage.

- F_GB: Forced test frequency.

- CVU1S: Status code for each measurement. Rows highlighted in blue indicate a fault. For details, refer to "Measurement status" in the *Model 4200A-SCS Clarius User's Manual.*

- NOISE: Formulator calculation result.

NOTE

GB stands for gate-to-bulk.

Nanowire tests

You can use C-V measurements on semiconductor nanowires and nanowire-based devices to derive important characteristics about the device, including mobility, carrier density, and device speed. Sometimes the capacitance is plotted as a function of channel length or gate length. These capacitance measurements can often be quite small, <1 pF. As a result, using proper techniques to reduce parasitic capacitance from affecting measurement accuracy is important.

These tests perform C-V sweeps on a two-terminal nanowire device. The tests are similar but use different drive frequencies. The tests generate capacitance versus voltage graphs.

cvu-nanowire connections

The following figure shows the basic test configuration. Refer to [CVU connections](#) (on page 2-1) for details. The `cv-gd` test is used to test a nanowire on a wafer. The `cv-sd` test can be used to test a nanowire on a wafer or a discrete nanowire device.

Use only the supplied (red) 100 Ω SMA cables for connections to the 4210-CVU or 4215-CVU. Be sure that all SMA cables used for the project are the same length.

NOTE

After making or changing connections, be sure to use the CVU Confidence Check diagnostic tool and do connection compensation tests. Refer to [Run an open check and short check](#) (on page 2-17) and [Connection compensation](#) (on page 2-8) for details.

Figure 80: Basic configuration to test a nanowire device
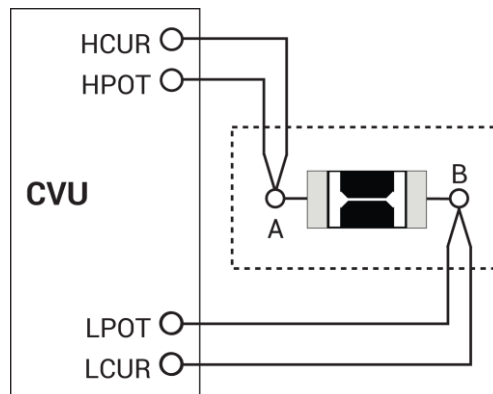
Formulas and constants

This project uses two formulas, described in the following topics. There are no constants.

Formula: CAVG

Formula name: CAVG

Units: F

Description: Calculates the average capacitance.

Formulator entry:

CAVG = AVG(CP_AB)

Formula: STD_DEV

Formula name: STD_DEV

Units: None

Description: Calculates the standard deviation of the capacitance measurements.

Formulator entry:

STD_DEV = STDEV(CP_AB)

cv-gd and cv-sd tests

`cv-gd` test: This test measures C-V (gate to drain at 1 MHz) on a nanowire device on a wafer or a discrete nanowire device. It generates a C versus V graph.

`cv-sd` test: This test measures C-V (source to drain at 100 kHz) on a nanowire device on a wafer or a discreet nanowire device. This test generates a C versus V graph and calculates average capacitance and standard deviation.

NOTE

Both tests are configured the same except for the drive frequency.

cv-gd and cv-sd Analyze sheet

The test data is displayed in the Analyze sheet:

- Cp_AB: Measured parallel capacitance.

- Gp_AB: Measured conductance.

- DCV_AB: Forced dc bias voltage.

- F_AB: Forced test frequency.

- CVU1S: Status code for each measurement. Rows highlighted in blue indicate a fault. For details, refer to "Measurement status" in the *Model 4200A-SCS Clarius User's Manual.*

- Formulas: Formulator calculation results (`cv-sd` test only).

NOTE

AB = Terminal A to Terminal B.

Make C-V measurements on a MOSCAP

In this section:

Introduction

Capacitance-voltage (C-V) measurements are commonly used to study gate-oxide quality in detail. These measurements are made on two-terminal devices called MOS capacitors, which are MOSFETs without a source and drain. C-V test results offer device and process information, including bulk and interface charges. Many MOS device parameters, such as oxide thickness, flat band voltage, and threshold voltage, can also be extracted from the C-V test data.

This section provides an example of how to use the 4210-CVU or 4215-CVU C-V Analyzer to make a C-V sweep on a MOS capacitor and derive common parameter extractions from the C-V data using the Formulator.

Equipment required

One 4200A-SCS with the following instruments and accessories:

- One 4210-CVU or 4215-CVU

- Four CA-447A SMA cables

- Four CS-1247 SMA female to BNC male adapters

- Two CS-701 BNC tee adapters

Device connections

Using the supplied cables, make connections from the output terminals of the CVU to the MOS capacitor.

⚠ WARNING

Hazardous voltages may be present on all output and guard terminals. To prevent electrical shock that could cause injury or death, never connect or disconnect from the 4200A-SCS while the output is on.

⚠ WARNING

To prevent electric shock, test connections must be configured such that the user cannot come in contact with test leads, conductors, or any device under test (DUT) that is in contact with the conductors. It is good practice to disconnect DUTs from the instrument before powering up the instrument. Safe installation requires proper shields, barriers, and grounding to prevent contact with test lead and conductors.


Connect the 4200A-SCS to the DUT

The hardware connections from the output terminals of the CVU to the MOS capacitor are shown in the following figure. Connect one cable to each of the CVU terminals, then connect one SMA female to BNC male adapter to the end of each cable.

The cables from the HCUR and HPOT terminals are coupled with the BNC tee adapter and are then connected to the gate of the MOS capacitor. The cables from the LCUR and LPOT terminals are also connected together with the BNC tee adapter and then are connected to the bulk of the MOS capacitor.

In the Clarius application, you will configure HCUR to be the high terminal of the ac ammeter and HPOT to be the high of the dc voltage source.

Figure 81: Connections from the 4210-CVU to the MOS capacitor
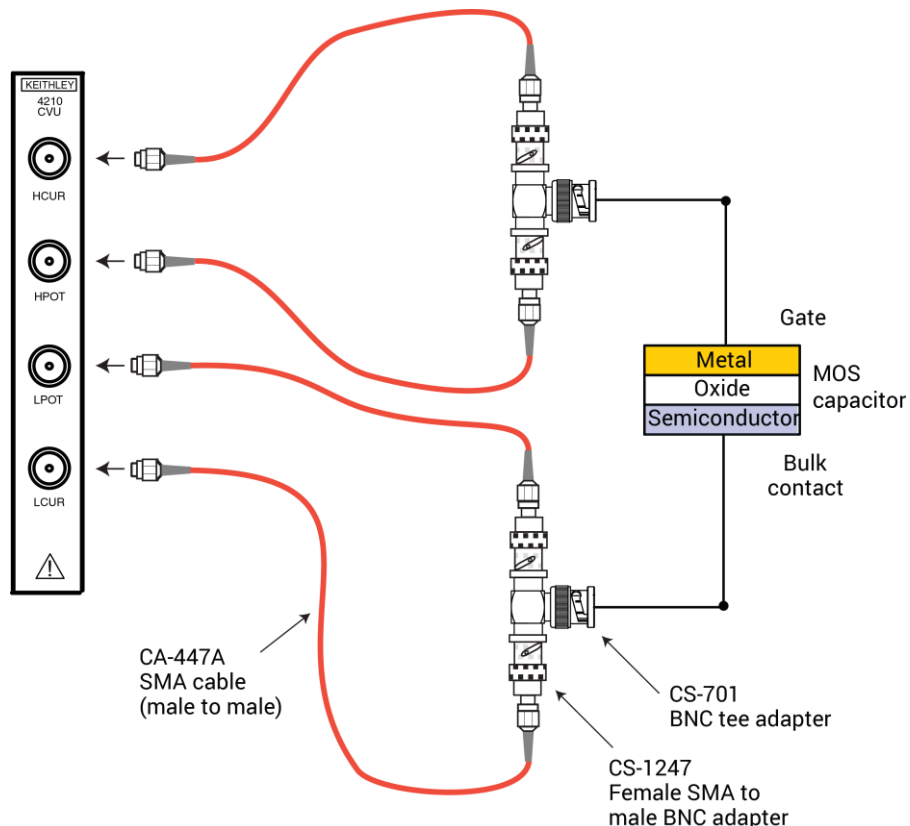
Set up the measurements in Clarius

This section describes how to set up the Clarius application to make a C-V sweep on a MOS capacitor. You select an existing project from the project library and configure a C-V sweep test.

For this example, you use Clarius to:

- Search for and select a project in the Project Library

- Configure the test

- Perform offset compensation

- Run the test

- View and analyze the test results

Search for and select a project

1. Choose **Select**.

Figure 82: Select highlighted
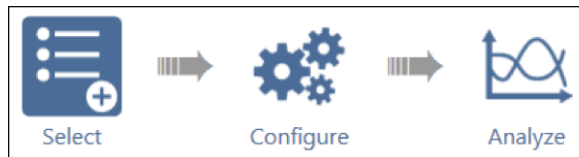
2. Select **Projects**.
3. Type **MOScap** into the search bar.
4. Select **Search**.
5. Select **MOS Capacitor C-V Project** (`cvu-moscap`).
6. Select **Create**.
7. Select **Yes** when prompted to replace the existing project.

The project is displayed. This project has the C-V tests for a MOS capacitor shown in the following figure.

Figure 83: MOS capacitor C-V project tree with three tests
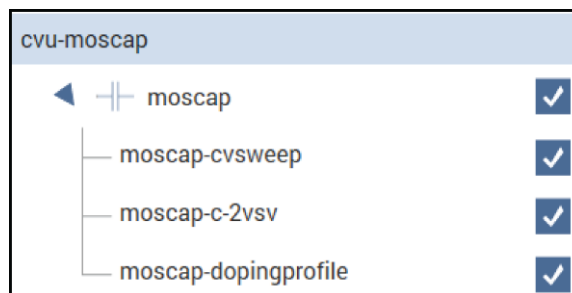
Configure the test

To configure the C-V sweep test, you set the source and measure parameters, define the timing parameters, and adjust the constants and formulas for extracting parameters from the C-V data.

This test makes a capacitance measurement at each step of a user-configured voltage sweep. A C-V graph is generated from the acquired data and several device parameters are calculated in the Formulator.
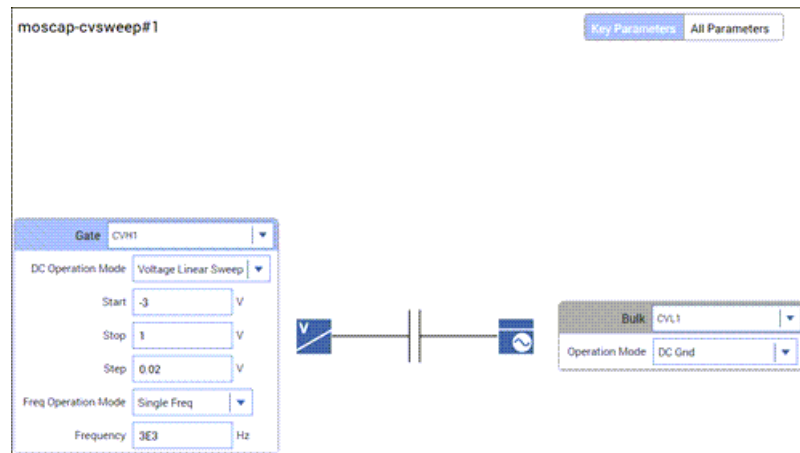
To configure the test:

1. Select **Configure**.

Figure 84: Configure highlighted
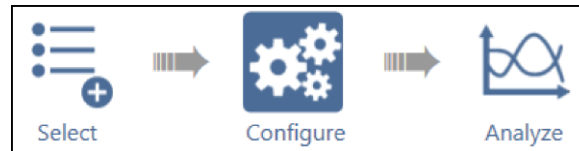
2. In the project tree, select the **moscap-cvsweep** test.
3. In the Key Parameters pane, adjust the voltage sweep and test frequency values as needed.

Figure 85: Key parameters for the C-V sweep of a MOS capacitor

4. In the Test Settings pane, set the Speed to **Quiet** for sensitive capacitance measurements.
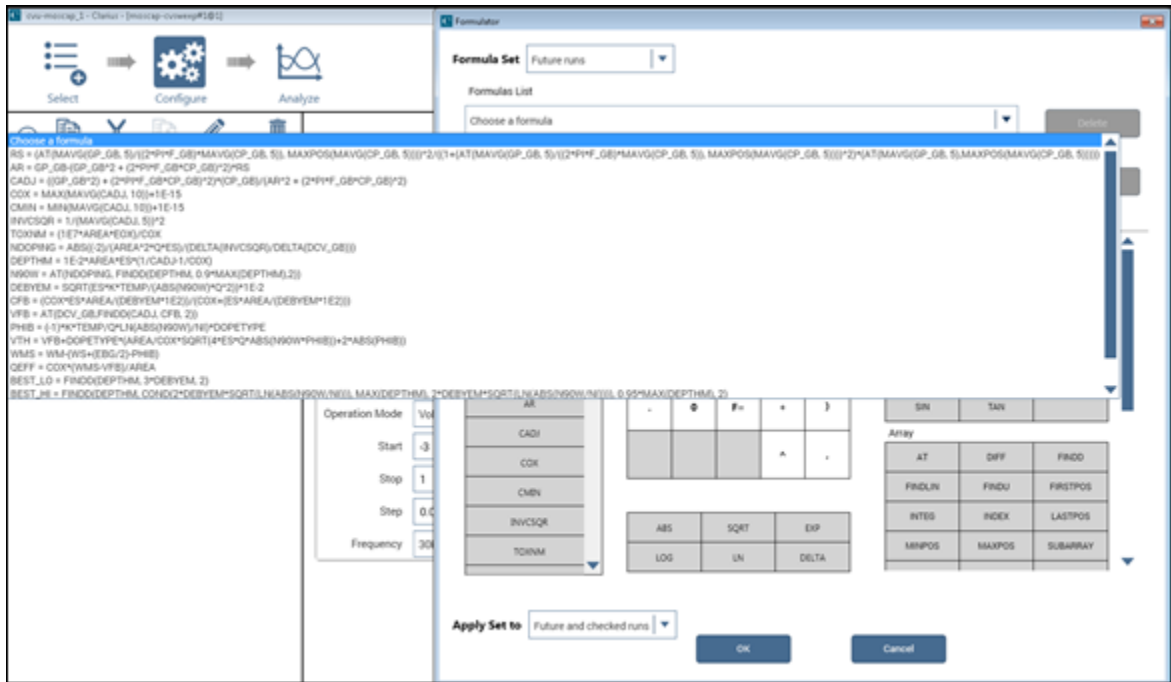
Figure 86: Test Settings pane

5. Adjust the **Sweep Delay** as needed.

6. Select **Formulator**. In this test, the Formulator contains equations for deriving common MOS capacitor parameters from the C-V data. Examples of these parameters include the oxide capacitance, oxide thickness, flatband voltage, flatband capacitance, threshold voltage, and doping concentration. You can view, edit, and add equations in this dialog box.

**Figure 87: Formulator dialog box**
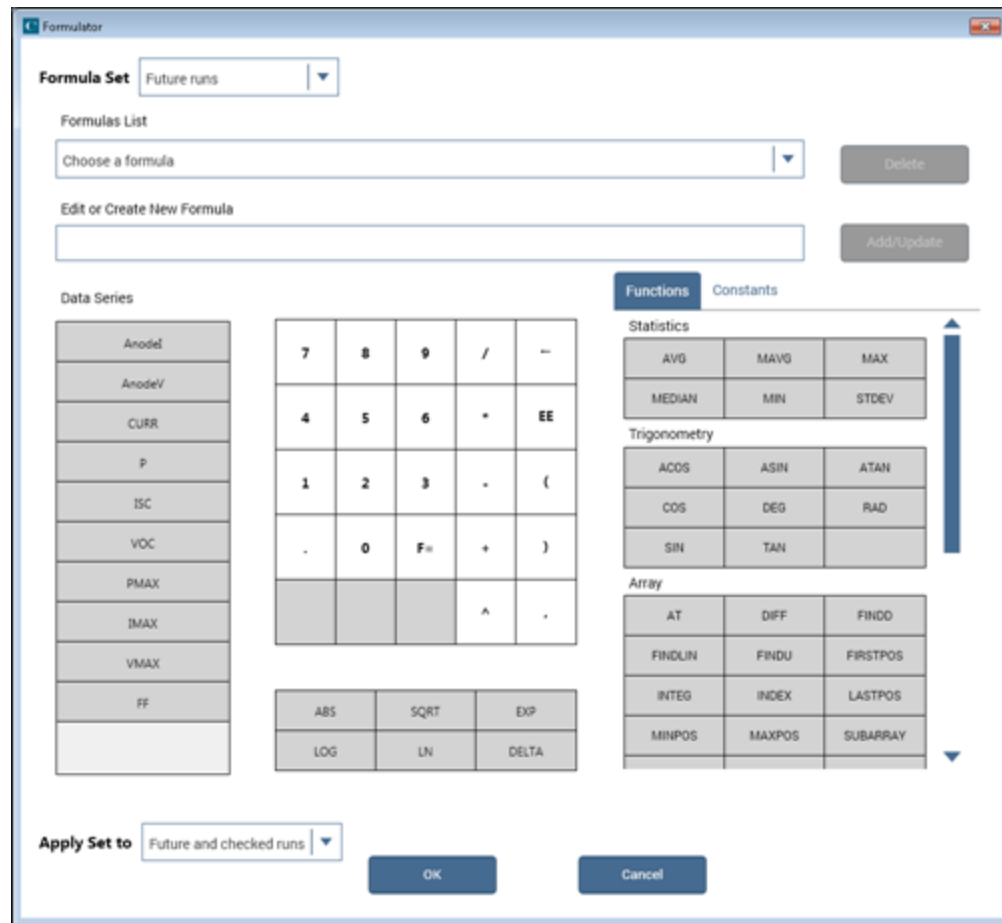
The following figure shows some of the equations that are included with this test. In the Constants area of the Formulator, you can change the constants that are used in the formulas, such as the gate area and temperature.

Figure 88: Formulas listed in the Formulator

7. Select **OK** to accept changes made in the Formulator.

8. Select **Terminal Settings**.

9. Select **Advanced**.

10. Adjust the parameters as needed.

Figure 89: Terminal Settings pane and Terminal Settings Advanced dialog box
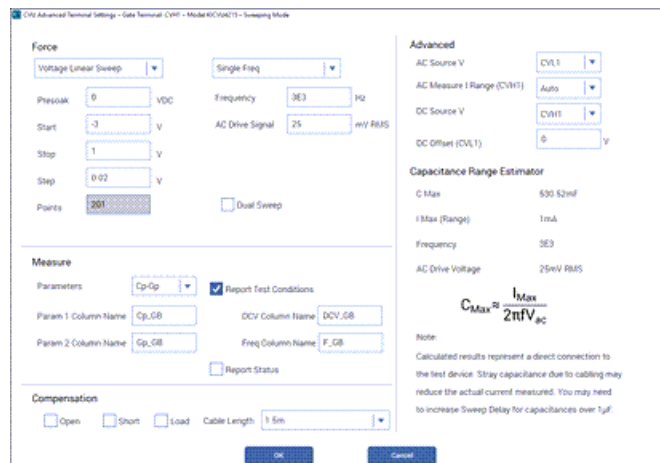
In this test, the CVH1 terminals are internally connected to the ac ammeter and the HI of the dc voltage source by default. The CVH1 terminals are externally connected to the gate of the MOS capacitor. The CVL1 terminals are internally connected to the ac voltage source and the LO of the dc voltage source and are externally connected to the bulk of the MOS capacitor or to the prober chuck.

Perform offset compensation

C-V measurements on a MOS capacitor are generally performed on a wafer using a prober. The 4210-CVU or 4215-CVU is connected to the MOS capacitor through cables, adapters, and a prober. Cabling adds stray capacitance to measurements.

To correct for the stray capacitance, Clarius has tools for offset correction. To set up offset correction, you perform the corrections for open in the Tools dialog box, and then you enable the corrections in the Terminal Settings pane.

Open compensation is generally used for high impedance measurements (<10 pF or >1 MΩ). A short compensation correction is generally used for low impedance measurements (>10 nF or <10 Ω). For a short compensation, you select Measure Short, and then short the probe to the chuck.

To perform the corrections:

1. Select **Tools**.
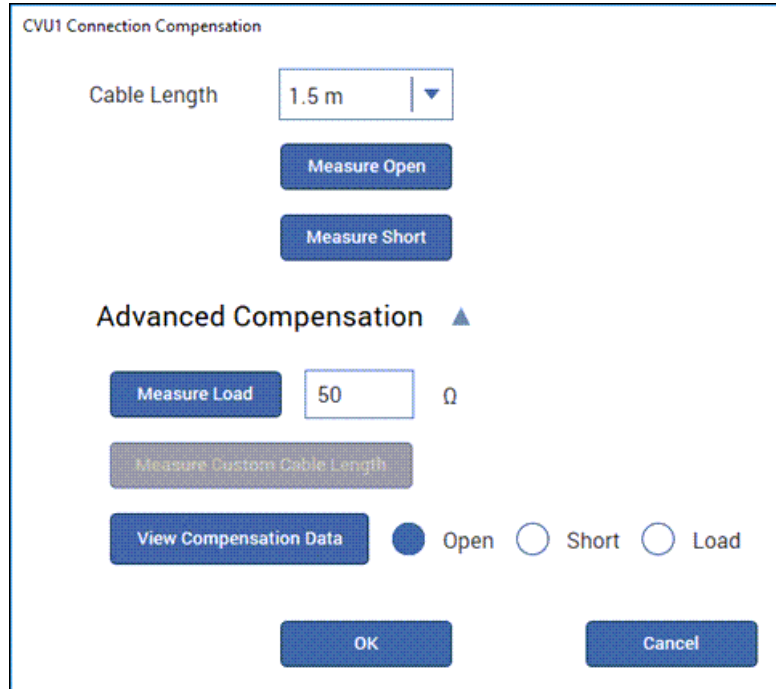
Figure 90: Tools icon in Clarius
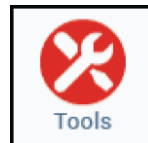
2. Select Instrument Tools from the left pane.
3. Select **CVU Connection Compensation**.

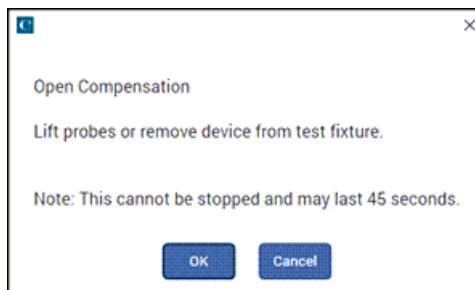**Figure 91: Clarius Tools dialog box**

4. Disconnect the probes from the DUT.
5. Select **Measure Open**.

Figure 92: CVU Connection Compensation dialog box

6. Select **OK**. You are prompted to verify that the probes have been disconnected from the DUT.

Figure 93: Prompt to remove probes from DUT

7. Make sure that the probes have been disconnected from the DUT, then select **OK**. The compensation runs, and a dialog box confirms that the compensation has run successfully.

8. Select **Exit** to close the Tools dialog box.

9. From the Terminal Settings pane, under Compensation, enable corrections by selecting **Open**.

Figure 94: Enabling CVU Compensation

Run the test

Select **Run** to execute the test.

Figure 95: Run
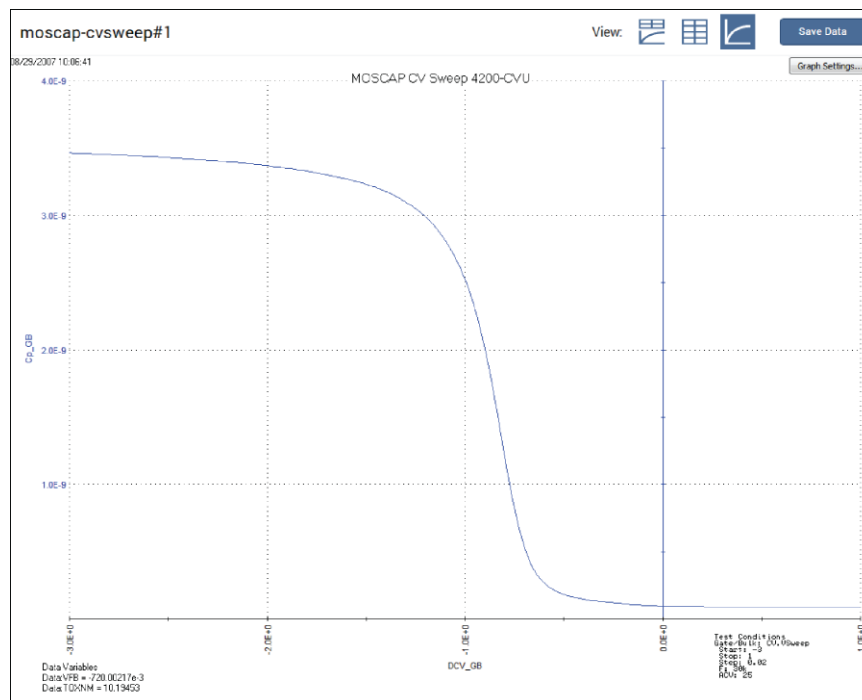

View and analyze the test results

Select **Analyze** while you run the project to view test results in real time.

Figure 96: Analyze highlighted

The C-V data is plotted on the graph as the `moscap-cvsweep` test executes.

Figure 97: Graph in the Analyze pane

You can also click the data only view of the Analyze sheet, as highlighted in the following figure, to display more data. For example, you can display a holistic view of the parameters for a device.

Figure 98: C-V data in the sheet

	Cp_GB	Gp_GB	DCV_GB	F_GB	RS	AR	CADJ	COX	CMIN	INVCSQR	TOX
1	3.4645E-9	36.4846E-6	-3.0000E+0	30.0000E+3	85.3264E+0	-19.4742E-9	3.4754E-9	3.4698E-9	90.0692E-12	#REF	
2	3.4633E-9	36.4740E-6	-2.9800E+0	30.0000E+3		-4.7268E-9	3.4741E-9			#REF	
3	3.4621E-9	36.4524E-6	-2.9600E+0	30.0000E+3		158.2666E-12	3.4729E-9			82.9086E+15	
4	3.4609E-9	36.4374E-6	-2.9400E+0	30.0000E+3		10.4458E-9	3.4717E-9			82.9667E+15	
5	3.4597E-9	36.4159E-6	-2.9200E+0	30.0000E+3		13.5522E-9	3.4705E-9			83.0257E+15	
6	3.4585E-9	36.3938E-6	-2.9000E+0	30.0000E+3		17.2661E-9	3.4693E-9			83.0848E+15	
7	3.4572E-9	36.3689E-6	-2.8800E+0	30.0000E+3		19.1980E-9	3.4680E-9			83.1443E+15	
8	3.4559E-9	36.3514E-6	-2.8600E+0	30.0000E+3		28.4679E-9	3.4667E-9			83.2056E+15	
9	3.4547E-9	36.3206E-6	-2.8400E+0	30.0000E+3		23.3835E-9	3.4655E-9			83.2676E+15	
10	3.4534E-9	36.3083E-6	-2.8200E+0	30.0000E+3		39.6584E-9	3.4641E-9			83.3307E+15	
11	3.4521E-9	36.2819E-6	-2.8000E+0	30.0000E+3		40.3526E-9	3.4628E-9			83.3955E+15	
12	3.4507E-9	36.2581E-6	-2.7800E+0	30.0000E+3		45.5286E-9	3.4614E-9			83.4610E+15	
13	3.4493E-9	36.2374E-6	-2.7600E+0	30.0000E+3		55.0267E-9	3.4600E-9			83.5275E+15	
14	3.4480E-9	36.2034E-6	-2.7400E+0	30.0000E+3		48.0724E-9	3.4587E-9			83.5952E+15	
15	3.4465E-9	36.1833E-6	-2.7200E+0	30.0000E+3		58.5557E-9	3.4572E-9			83.6643E+15	
16	3.4451E-9	36.1589E-6	-2.7000E+0	30.0000E+3		63.6099E-9	3.4558E-9			83.7338E+15	
17	3.4436E-9	36.1332E-6	-2.6800E+0	30.0000E+3		69.5090E-9	3.4543E-9			83.8057E+15	
18	3.4421E-9	36.1037E-6	-2.6600E+0	30.0000E+3		70.9472E-9	3.4528E-9			83.8791E+15	
19	3.4406E-9	36.0822E-6	-2.6400E+0	30.0000E+3		81.4972E-9	3.4513E-9			83.9541E+15	
20	3.4390E-9	36.0475E-6	-2.6200E+0	30.0000E+3		80.0865E-9	3.4497E-9			84.0308E+15	
21	3.4375E-9	36.0144E-6	-2.6000E+0	30.0000E+3		79.6444E-9	3.4481E-9			84.1090E+15	
22	3.4358E-9	35.9866E-6	-2.5800E+0	30.0000E+3		86.8085E-9	3.4464E-9			84.1885E+15	
23	3.4342E-9	35.9480E-6	-2.5600E+0	30.0000E+3		82.0969E-9	3.4448E-9			84.2691E+15	
24	3.4325E-9	35.9198E-6	-2.5400E+0	30.0000E+3		88.1696E-9	3.4431E-9			84.3510E+15	
25	3.4309E-9	35.8909E-6	-2.5200E+0	30.0000E+3		94.6727E-9	3.4414E-9			84.4342E+15	
26	3.4292E-9	35.8622E-6	-2.5000E+0	30.0000E+3		101.1837E-9	3.4397E-9			84.5191E+15	
27	3.4274E-9	35.8265E-6	-2.4800E+0	30.0000E+3		102.8557E-9	3.4379E-9			84.6060E+15	

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