Ge based Tunneling and Negative Capacitance FETs: Devices and Characterization

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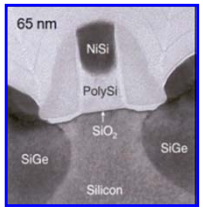
Outline

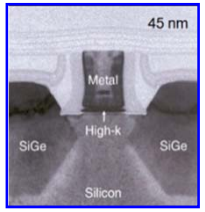
- Non-Si Microelectronics（非硅微电子学）
  - More Moore
  - More than Moore
- High Mobility Ge and GeSn MOSFETs
- Beyond CMOS
  - GeSn Tunneling FETs
  - Ge and GeSn Negative Capacitance FETs
  - Piezoelectric FETs
- Summary

Evolution of CMOS Devices

65 nm

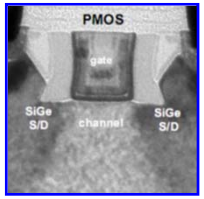


45 nm

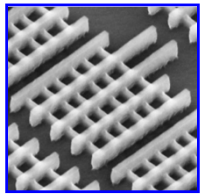


Intel

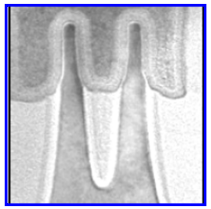
32 nm



22 nm



14 nm



10-7-5-3 nm

Si FinFET and GAA FET：
From Lab to Foundries

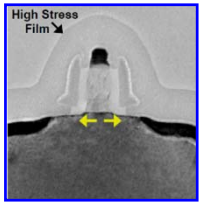
10 nm 以下 (By ITRS and IRDS)

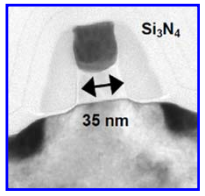
高迁移率非Si材料：
III-V、SiGe、Ge等

Beyond CMOS：
TFET、NC Tansistor、
Spinelectronics

Stained Si pFETs with SiGe S/D Stressor

Stained Si nFETs with Stress Liner





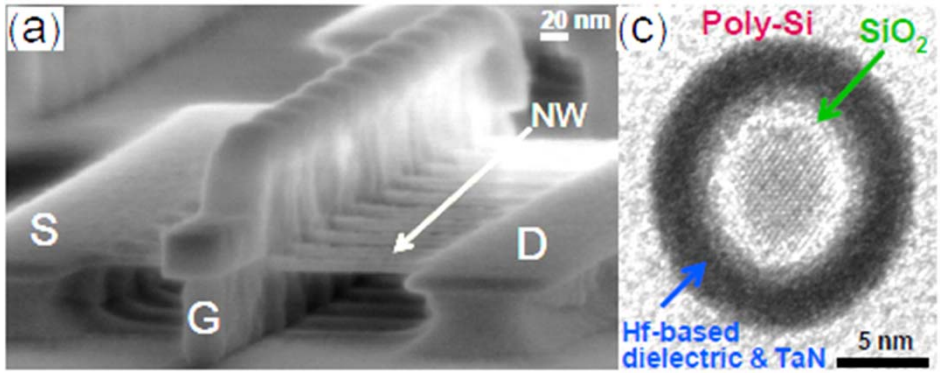
High-k
Metal Gate

3D Transistor
FinFET

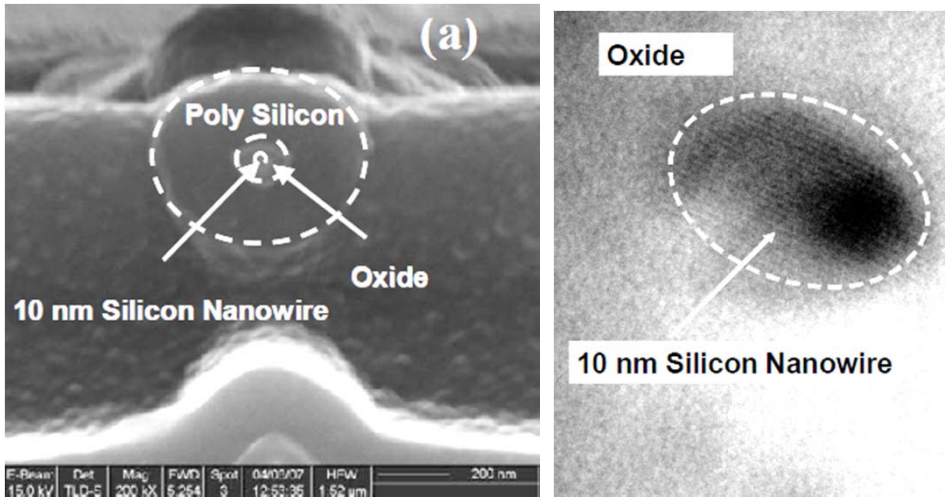
Strained Si

2005 2007 2009 2012 2015 2018 Year

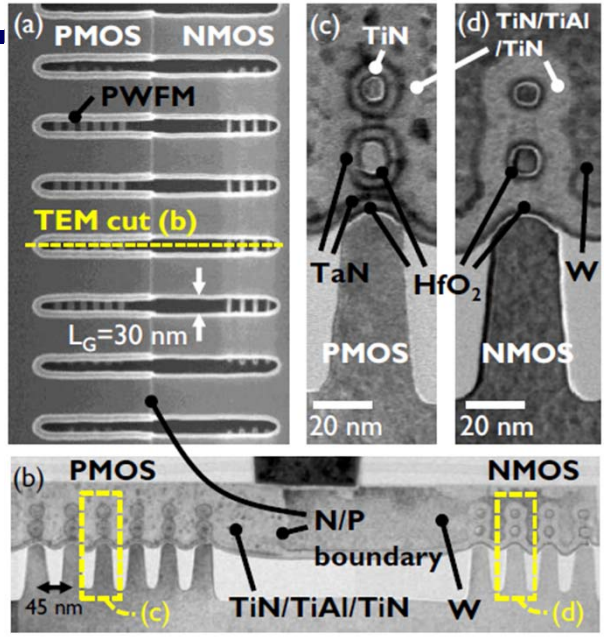
Nanowire/Nanosheet FETs



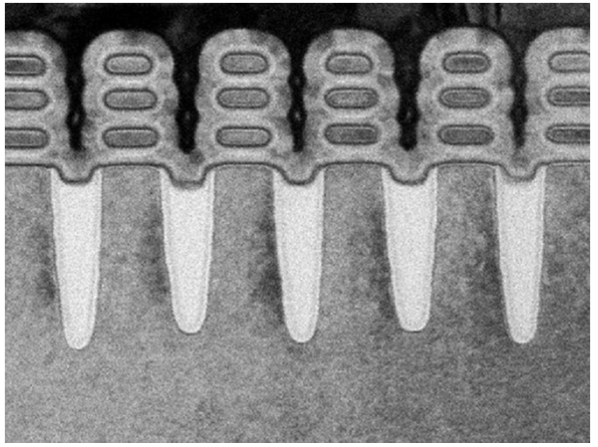
IEDM 2009, pp.297 (IBM)



IEDM 2007, pp.895 (北大，黄如院士)



IEDM 2016, pp.524 (IMEC)



VLSI 2017, pp.T230 (IBM)

Post-Moore Era

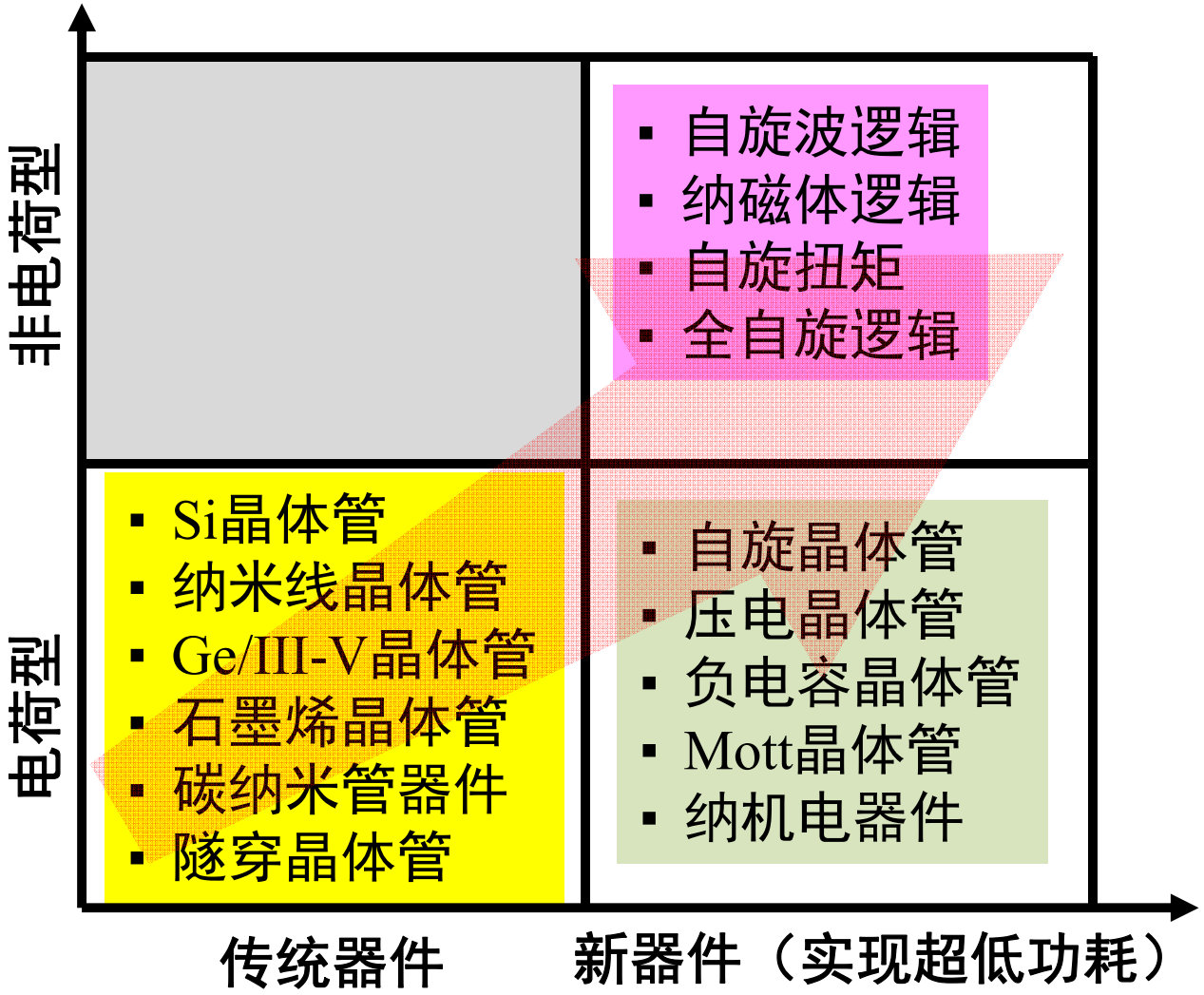
2016: International Roadmap for Devices and Systems (IRDS)

- ❑ More Moore
- ❑ Beyond CMOS
- ❑ Application Benchmarking
- ❑ Environment, Safety, and Health
- ❑ Factory Integration
- ❑ Metrology
- ❑ Outside System Connectivity
- ❑ System and Architecture
- ❑ Yield Enhancement

- 采用新材料、新结构实现低功耗集成电路
- 满足更多，更广泛的芯片需求

Beyond CMOS-功耗瓶颈

- 传统器件与新器件并重
- 突出新材料和新原理
- 基础研究推动新器件发展



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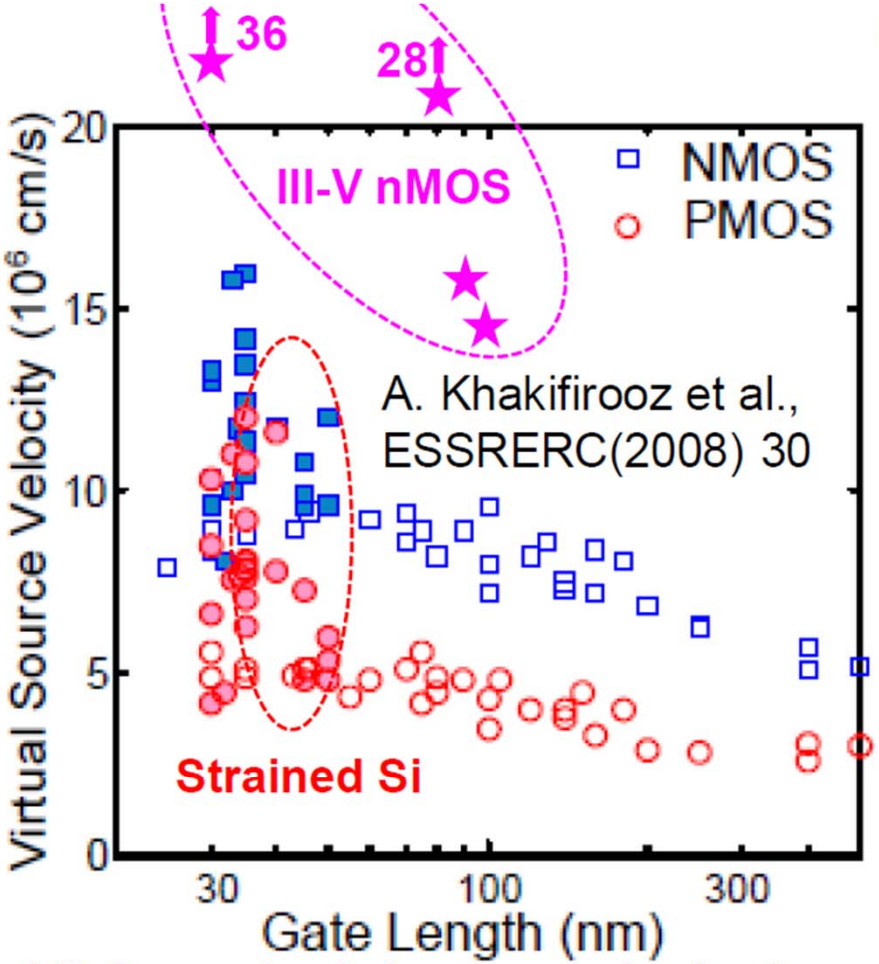
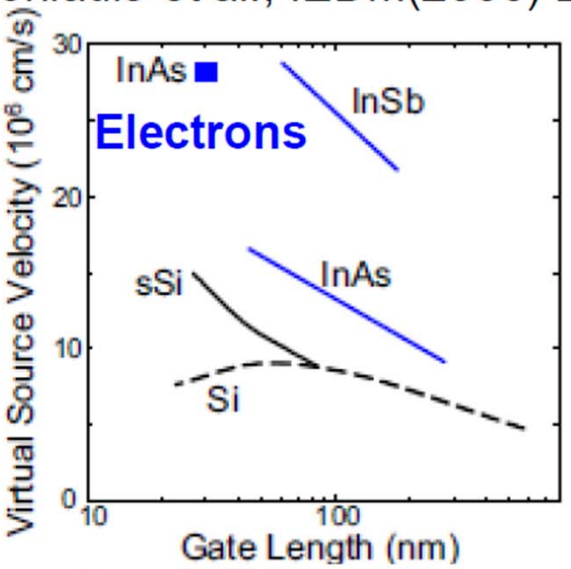
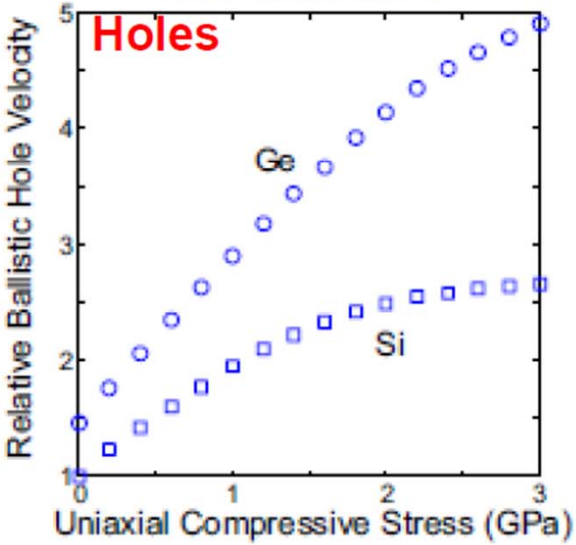
Motivation: Trend of Injection Velocity



D. Antoniadis et al., IEDM(2008) 253





- High carrier injection velocity is expected for low effective mass channel materials such as III-V and (strained) Ge

Motivation: Need for High Mobility Channels

	Si	Ge	GaAs	InP	InAs	InSb
electron mob. (cm^2/Vs)	1600	3900	9200	5400	40000	77000
electron effective mass ($/m_0$)	m_t: 0.19 m_l: 0. 916	m_t: 0.082 m_t: 1.467	0.067	0.08	0.026	0.0135
hole mob. (cm^2/Vs)	430	1900	400	200	500	850
hole effective mass ($/m_0$)	m_{HH}: 0.49 m_{LH}: 0.16	m_{HH}: 0.28 m_{LH}: 0.044	m_{HH}: 0.45 m_{LH}: 0.082	m_{HH}: 0.45 m_{LH}: 0.12	m_{HH}: 0.57 m_{LH}: 0.35	m_{HH}: 0.44 m_{LH}: 0.016
band gap (eV)	1.12	0.66	1.42	1.34	0.36	0.14
permittivity	11.8	16	12	12.6	14.8	17

- Ge ⇒ lightest hole m^* (light electron m^*) ⇒ pMOS (CMOS)
- III-V ⇒ light electron m^* ⇒ nMOS
- GaAs·InP ⇒ E_g higher than that in Si ⇒ low power

Motivation: Need for High Mobility Channels

	Si	Ge	GaAs	InAs	InSb	GeSn
电子迁移率	1600	3900	9200	40000	77000	高于Ge
空穴迁移率	430	1900	400	500	850	类Ge
禁带宽度 (eV)	1.12	0.66	1.424	0.36	0.17	小于Ge

$$I_D = W \times v \times Q_{inv}$$

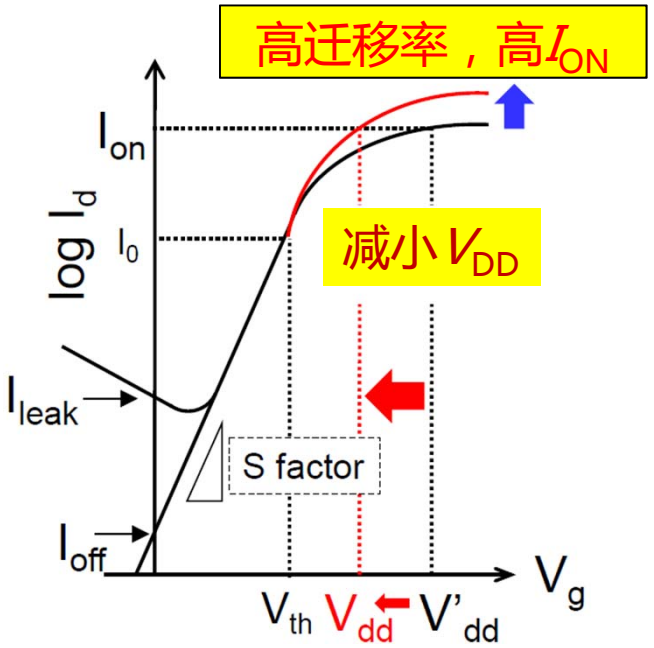
width, velocity, inversion charge density

$$v \propto \mu_{eff}$$

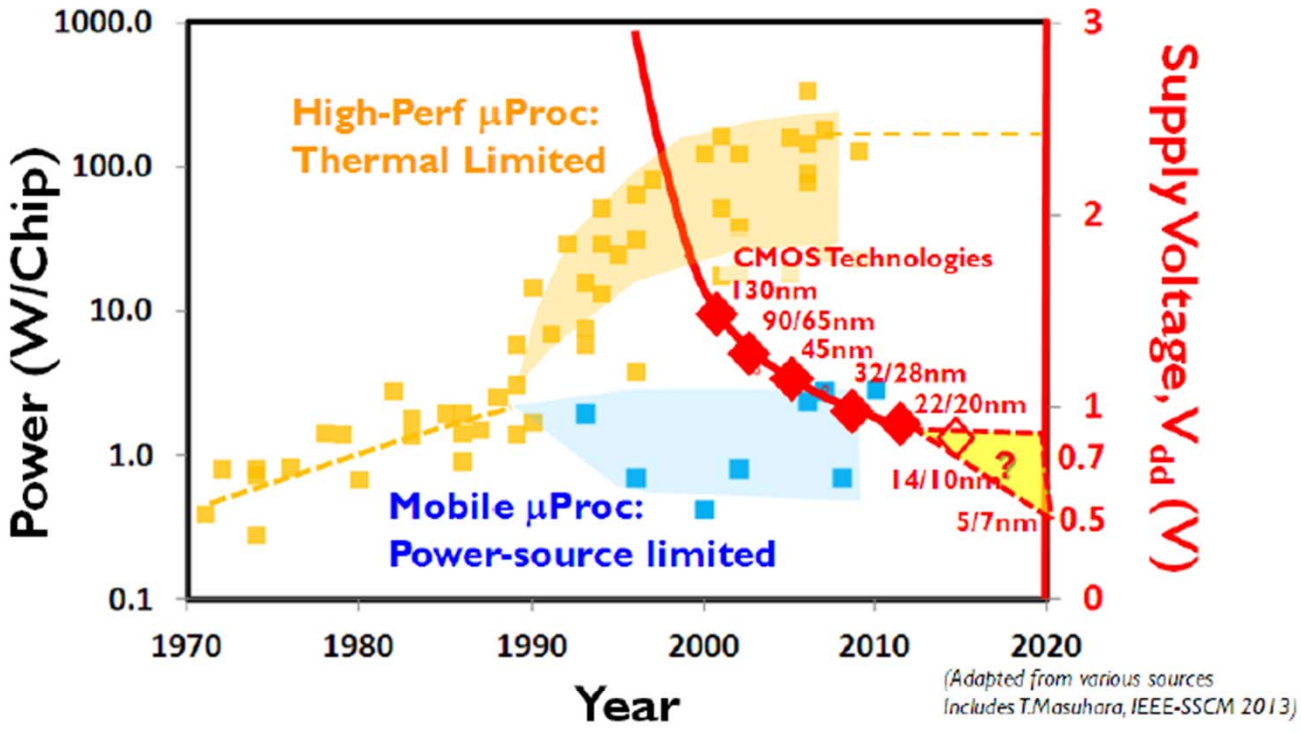
mobility

$$Q_{inv} \propto C_g(V_{gs} - V_{th})^{\eta}$$

gate capacitance; gate over-drive



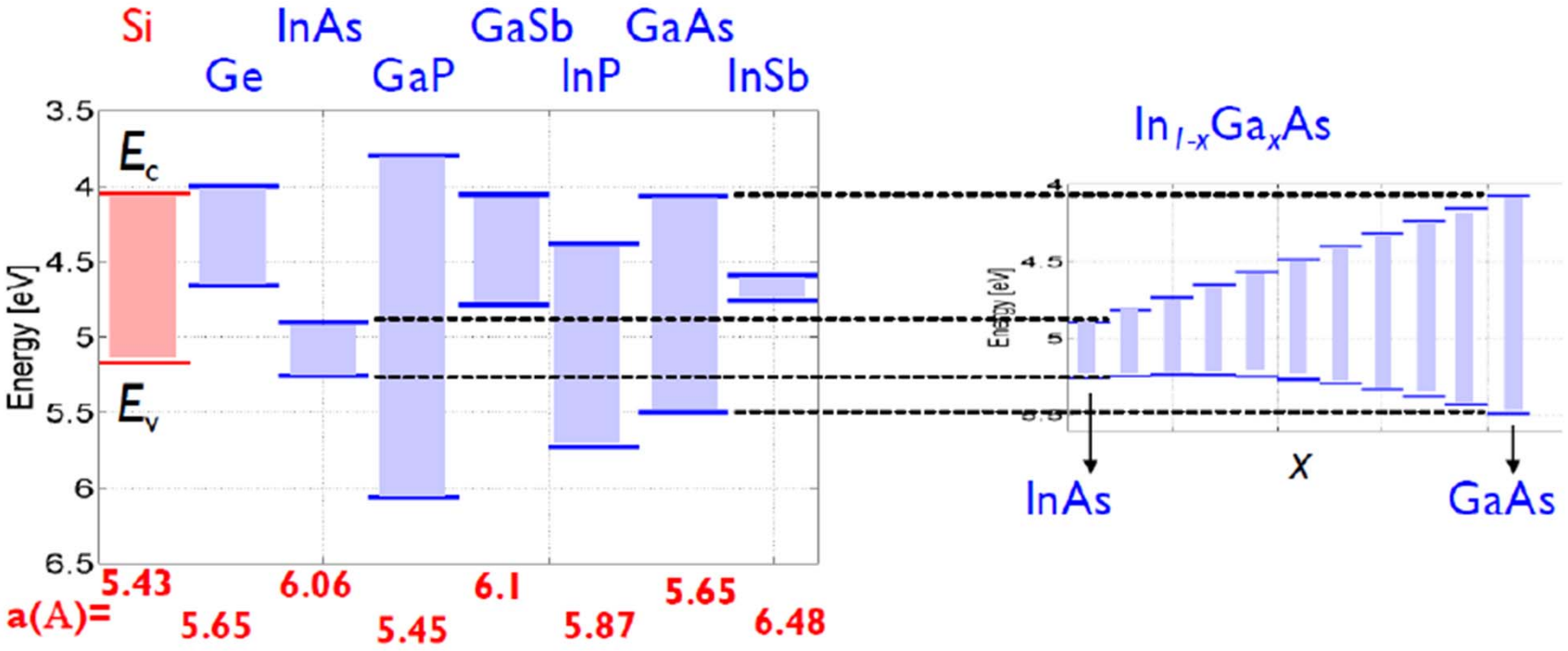
Motivation: Need for High Mobility Channels



$$P_{tot}=P_{dyn}+P_{stat}$$
$$P_{stat}=I_{OFF}\ V_{DD}$$
$$P_{dyn}=fCV^2_{DD}$$

Devices with low V_T & steep SS
Further increase in mobility to improve performance at reduced V_{DD}

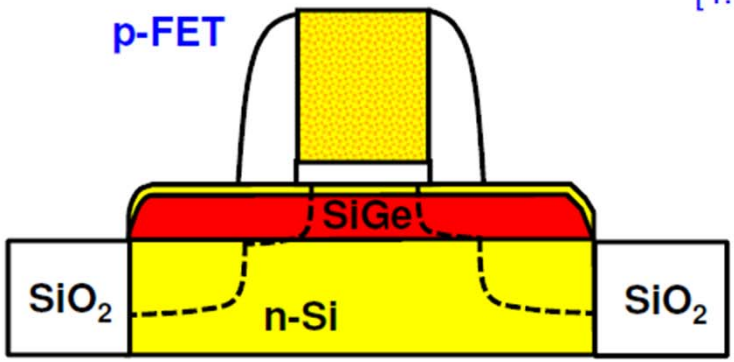
Motivation: Need for High Mobility Channels

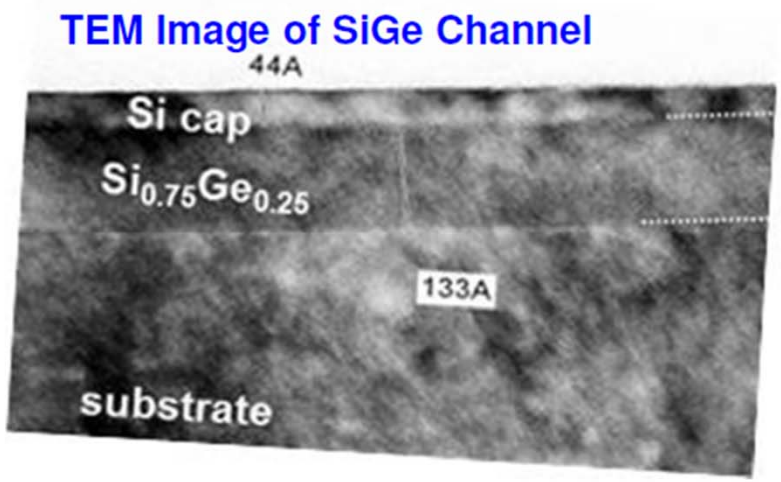


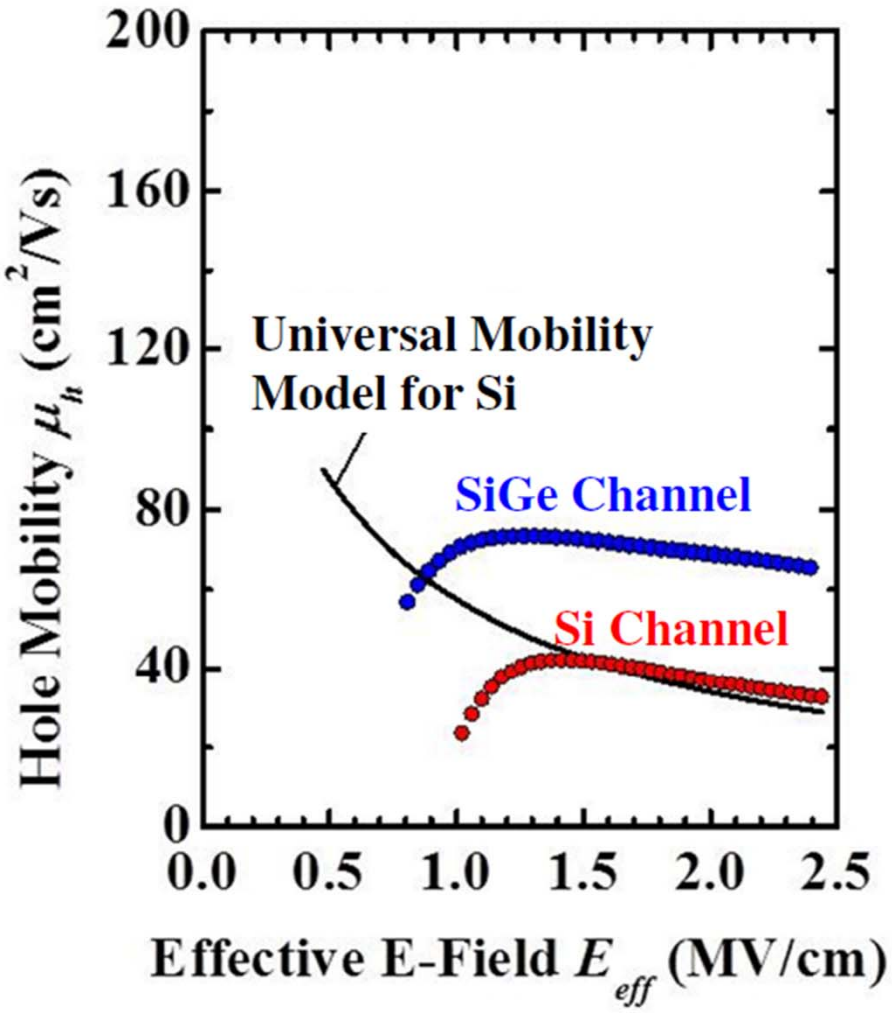
New Electrostatics with hetero-structure device possibilities

SiGe FETs: Strained SiGe Channel p-FET

[Y.-C. Yeo, Q. Lu, T.-J. King, C. Hu *et al.*, *IEDM 2000*, pp. 753]



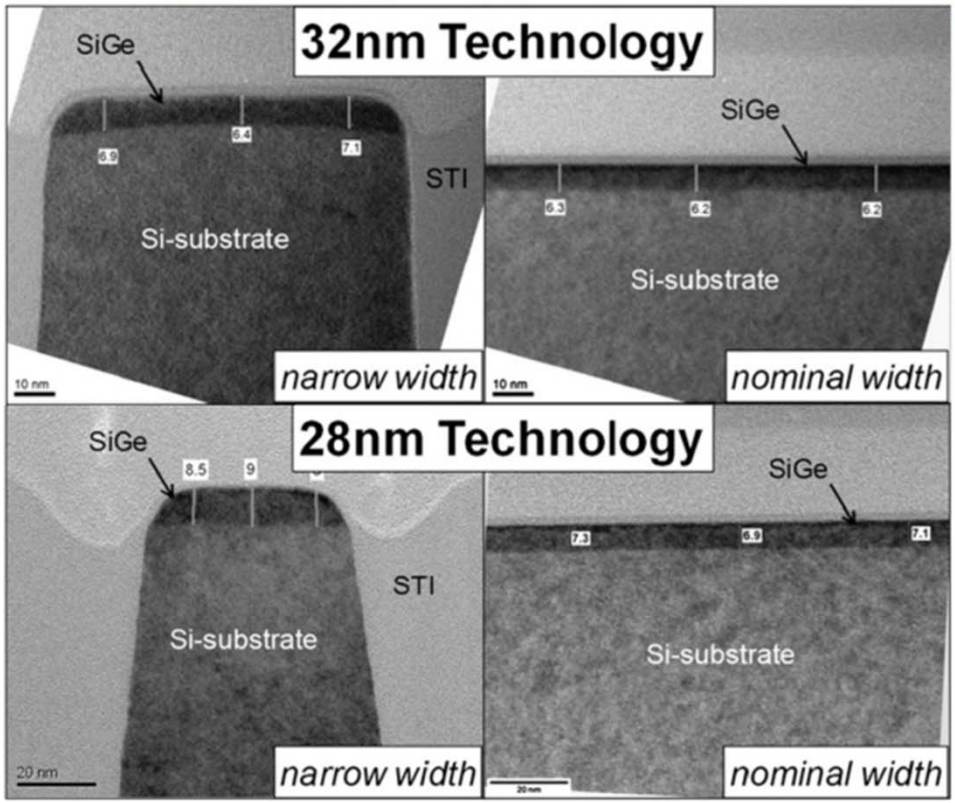




SiGe FETs: Strained SiGe Channel p-FET

Globalfoundries. SiGe Channel on Bulk Si.

[C. Reichel *et al.*, "SiGe channels for V_T control of high-k metal gate transistors for 32 nm CMOS technology and beyond", *Thin Solid Films 520*, pp. 3170, Feb. 2012]

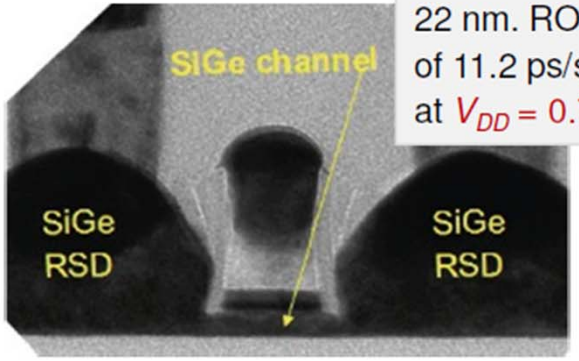


"GLOBALFOUNDRIES 32 nm high-k metal gate technology, with SiGe channel for V_{TH} control of p-FET, is in production. This epitaxial channel material is being introduced into high volume manufacturing in CMOS technology."

IBM, STM, Globalfoundries, Renesas, Soitec, CEA-LETI

SiGe Channel on UTSOI.

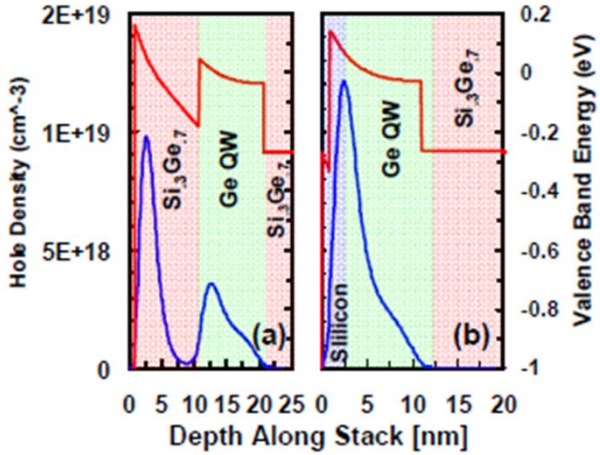
[K. Cheng *et al.*, *IEDM 2012*, 18.1]

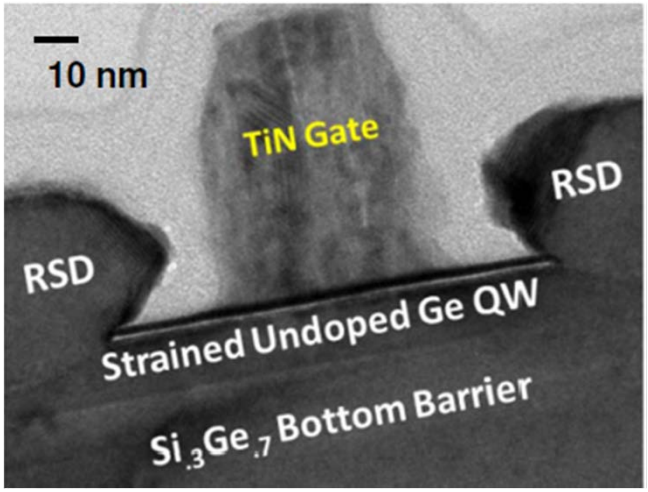


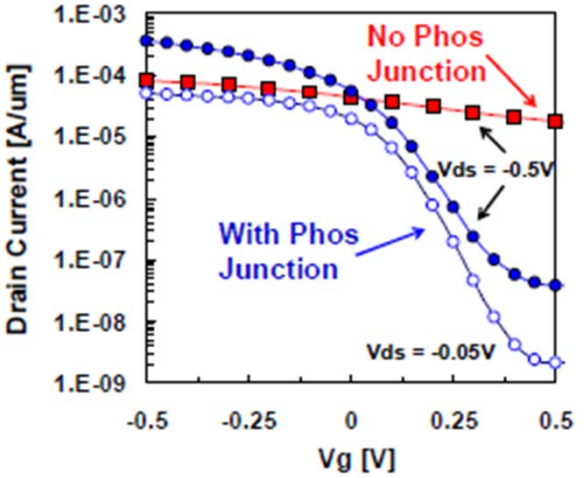
22 nm. RO delay of 11.2 ps/stage at V_{DD} = 0.7 V

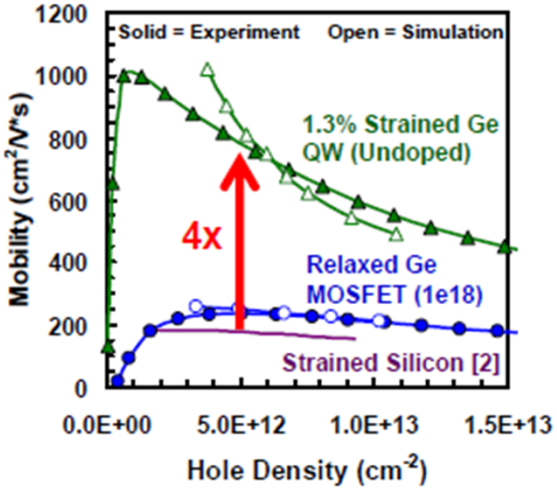
Ge pFET:
Device Architecture and Electrical Results

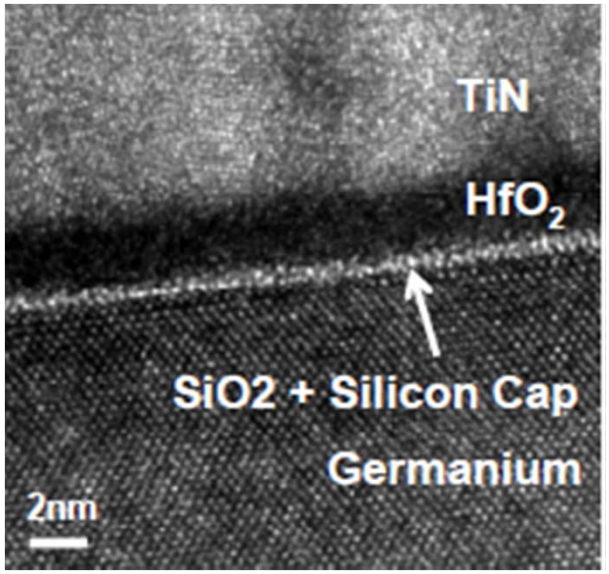
Intel.
Strained Ge
Quantum Well pFET
R. Pillarisetty *et al.*,
***IEDM*, 2010, p.150**



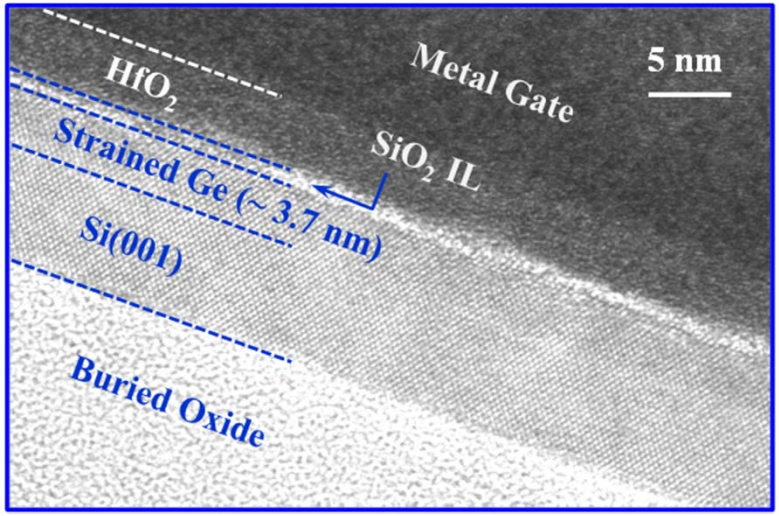


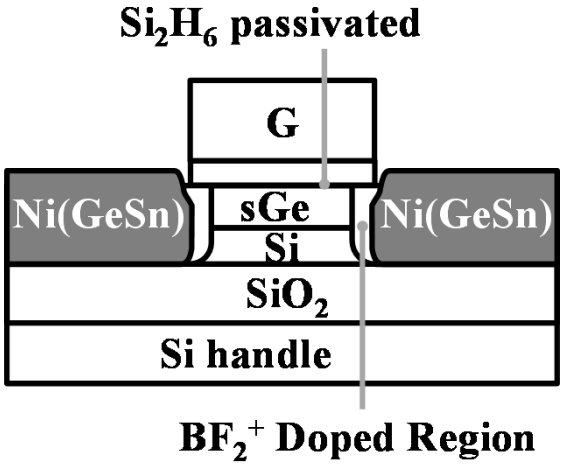






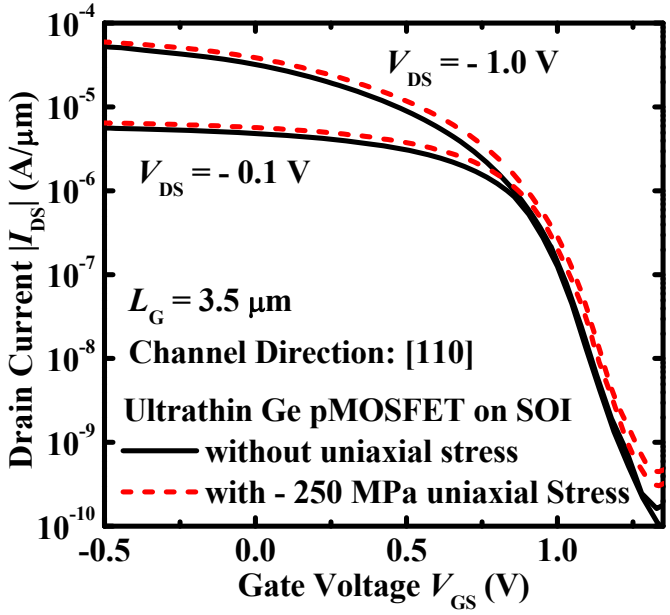
Strained Ge Quantum Well pMOSFET (西电)

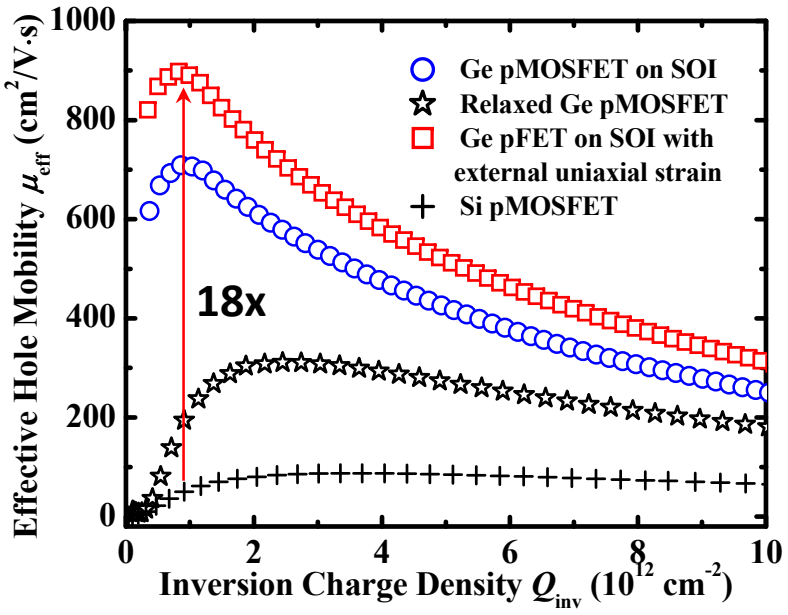




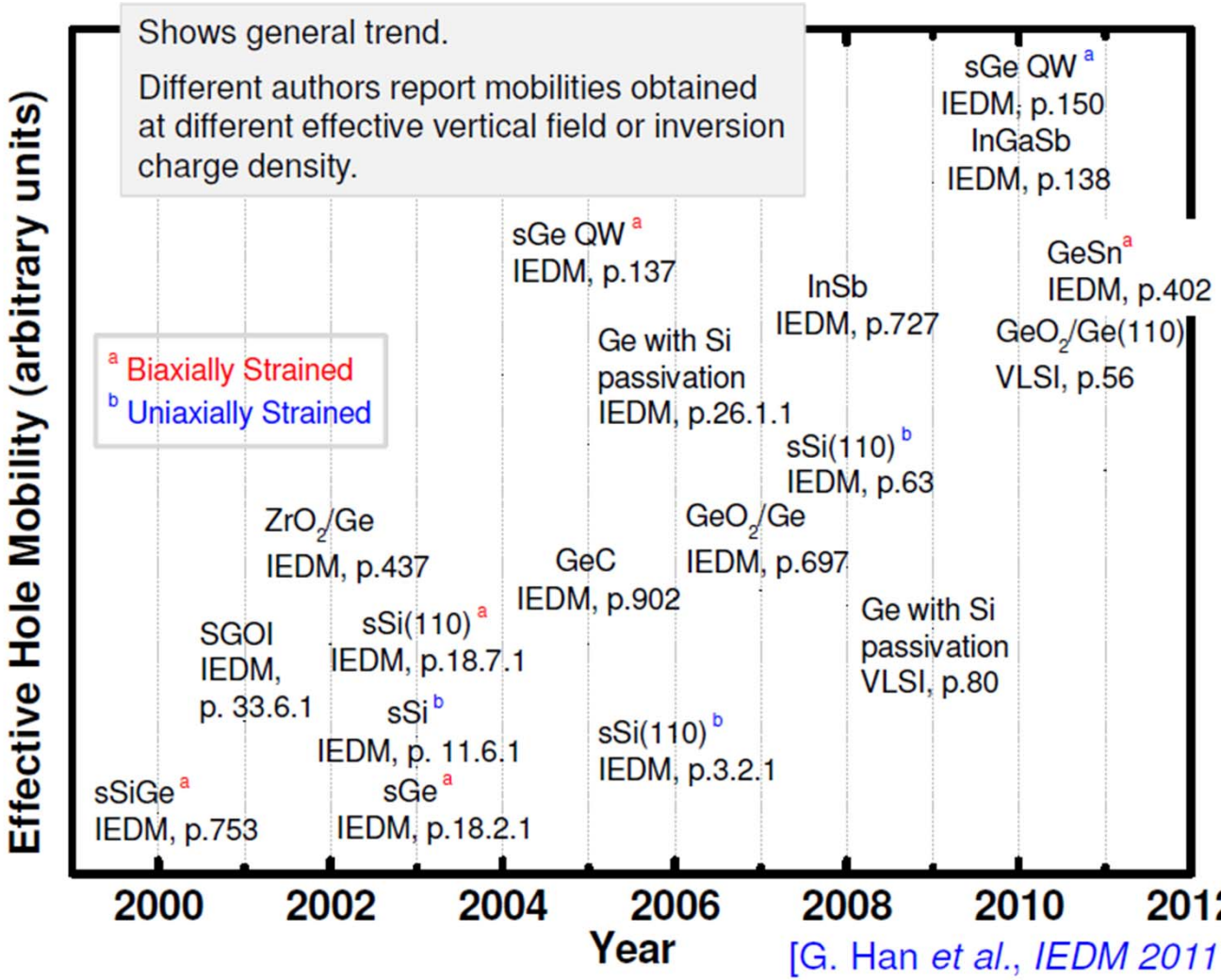
H. Wang et al., ICSICT 2016, (Excellent Student Paper Award);

Nanoscale Research Letters, v.12, pp.120, 2017.





World's First GeSn pFET (IEDM 2011 late news)

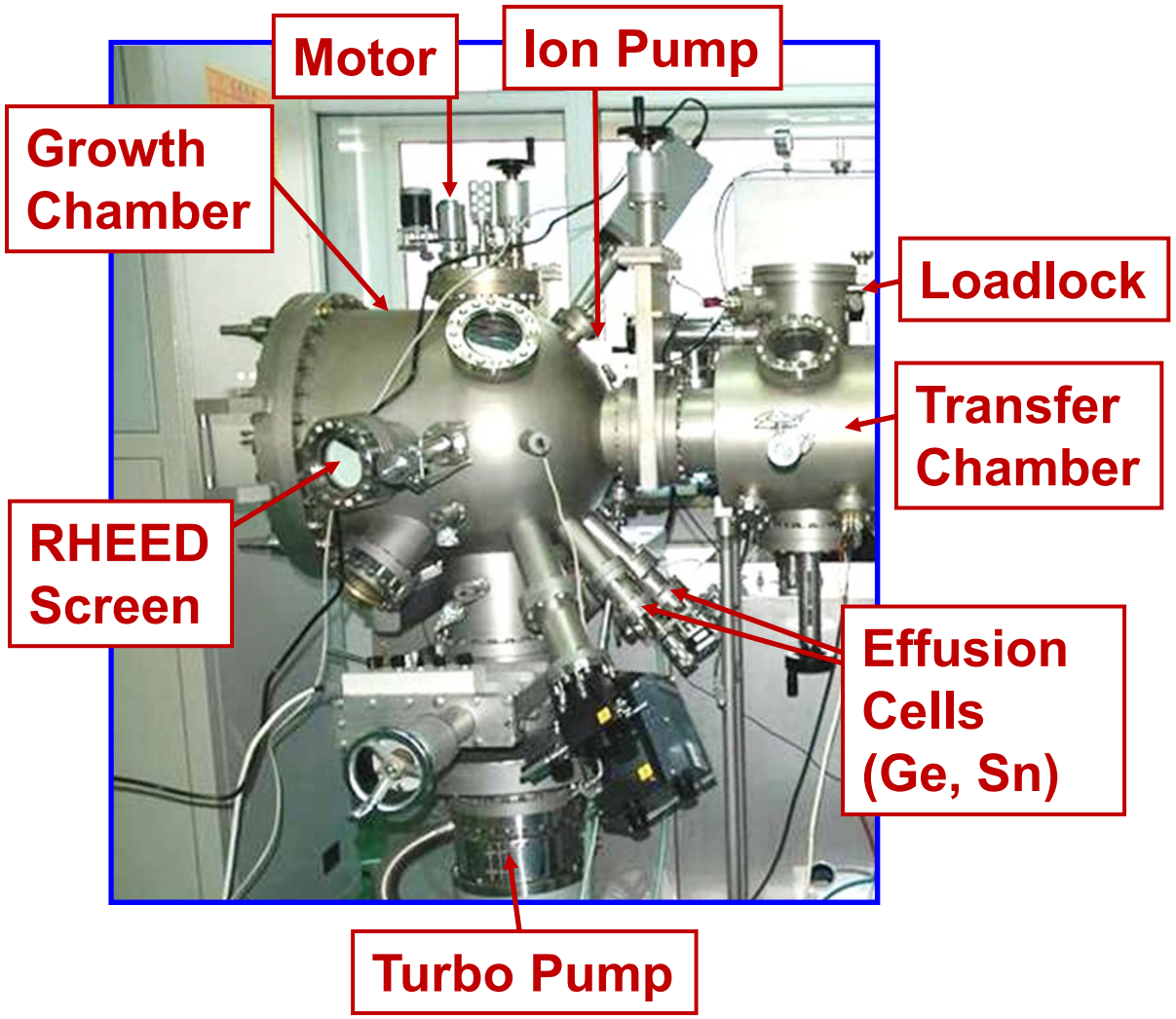


Material	Bulk Mobility for Holes (cm^2/Vs)
GaAs	400
Si	450
$In_{0.53}Ga_{0.47}As$	460
InAs	500
InSb	850
Ge	1900
GeSn	>1900

[G. Han *et al.*, *IEDM 2011 Late News*, pp. 402].

GeSn Materials: Epitaxial Growth Using Solid Source MBE

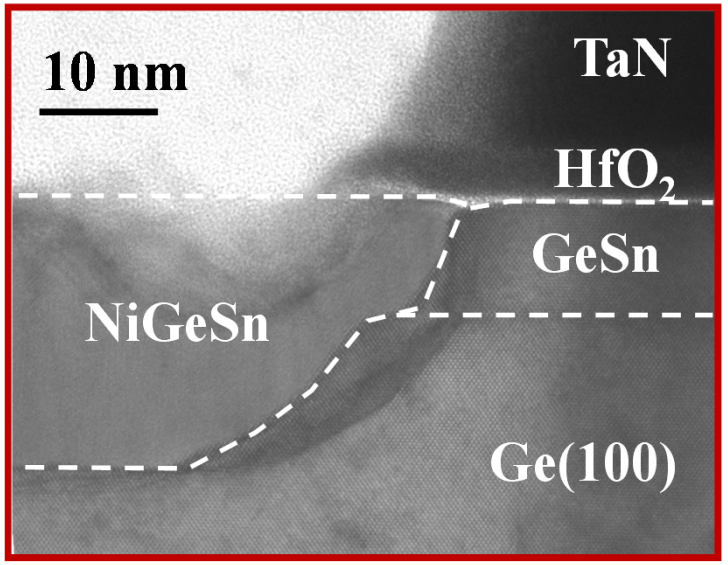
- Home-made MBE Tool.
- Base Pressure: 3×10^{-8} Pa
- *In situ* RHEED monitoring
- Compatible with 4-inch substrate



World's First GeSn pFET (IEDM 2011 late news)

Key Process Steps

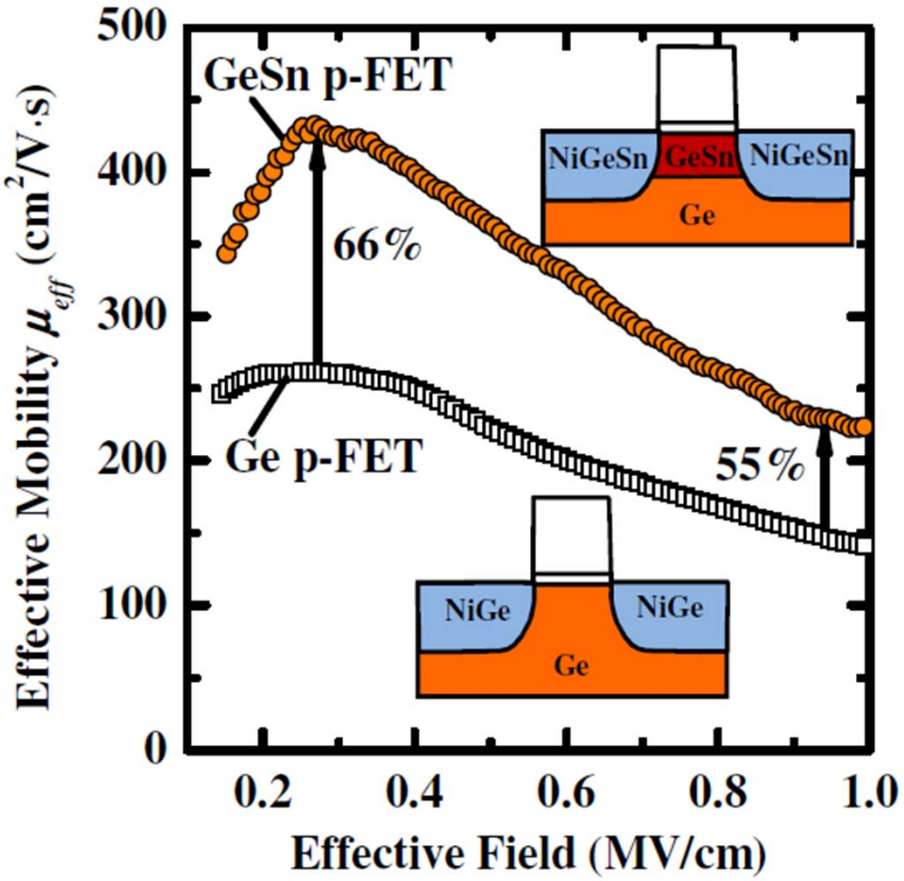
- Epitaxial Growth of 10 nm $Ge_{0.947}Sn_{0.053}$ by MBE (180 ˚C)
- Low Temperature Si Passivation using Si_2H_6 (370 ˚C)
- TaN/HfO_2 Gate Stack Formation
- Active Region Definition
- Ni Deposition (10 nm)
- Anneal for NiGeSn Metallic S/D Formation (350 ˚C)
- Selective Removal of Ni Using H_2SO_4

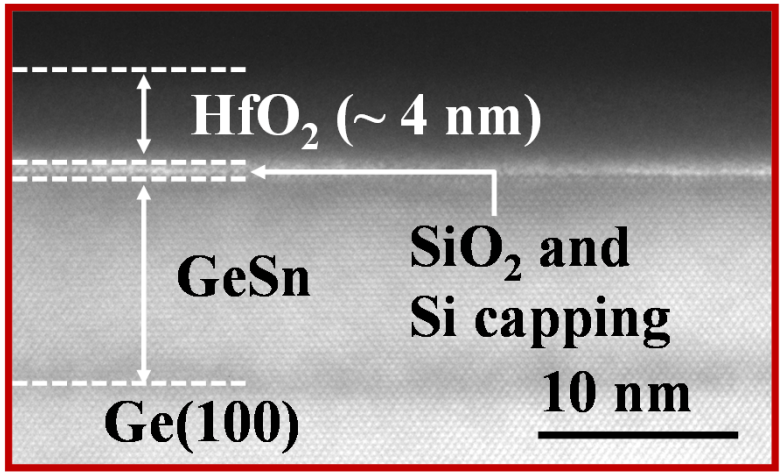


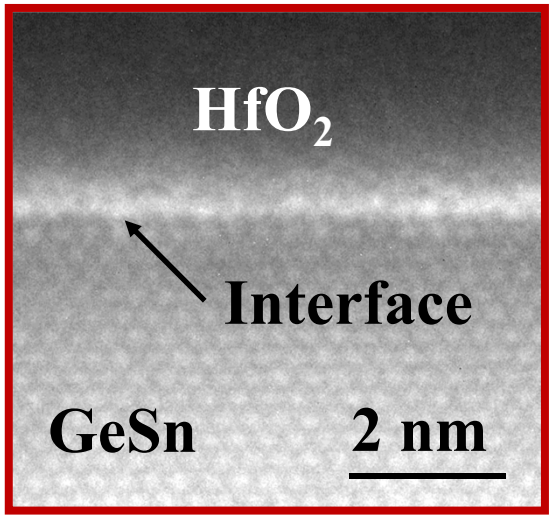
World's First GeSn pFET (IEDM 2011 late news)

$Ge_{0.947}Sn_{0.53}$ has ~55% higher hole mobility than relaxed Ge.

[G. Han *et al.*, *IEDM 2011 Late News*, pp. 402].



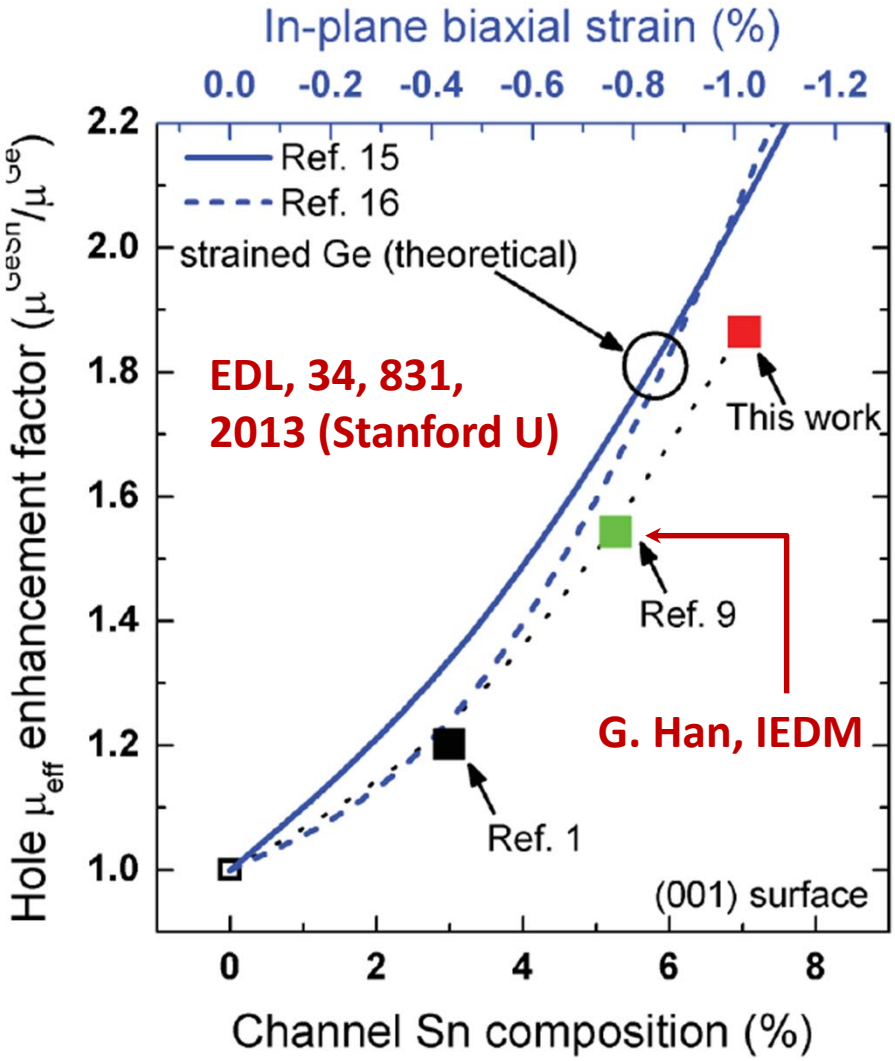




World's First GeSn pFET (IEDM 2011 late news)

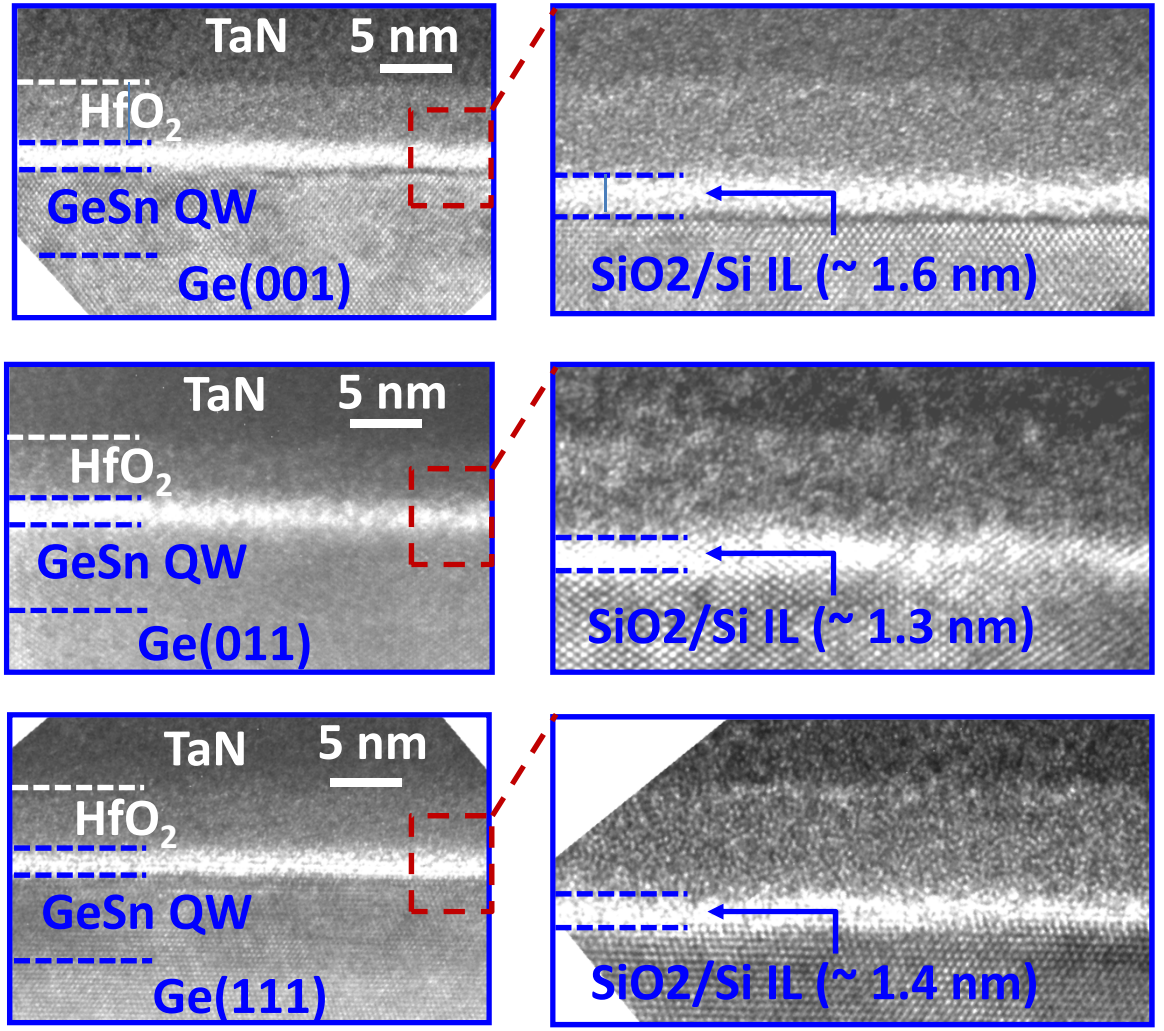
An increase in the Sn composition of GeSn on Ge buffer leads to

- **increase of channel compressive strain**
- **boosting hole mobility**



Strained GeSn Quantum Well pMOSFETs

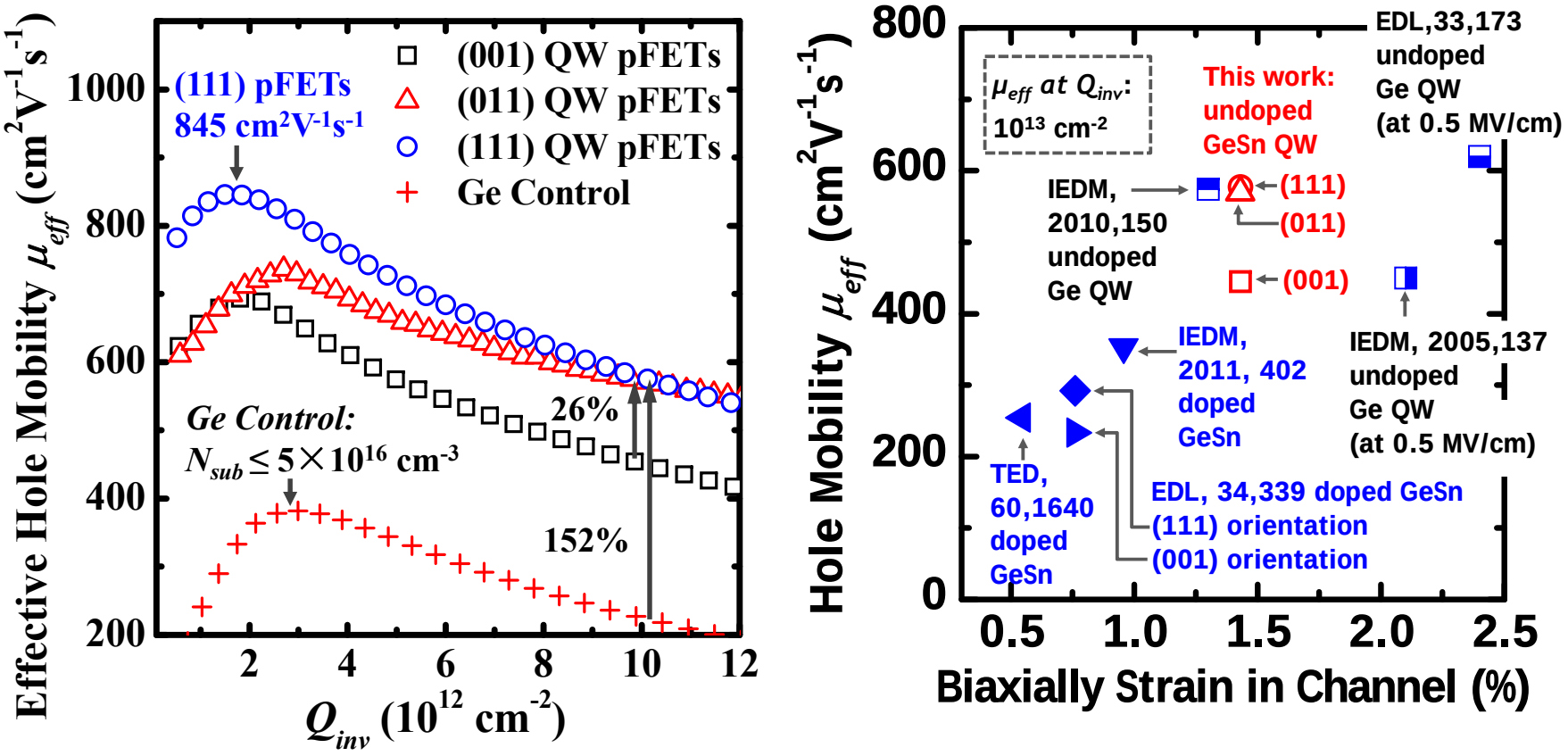
- High quality GeSn channel and Si_2H_6 passivated interface.
- Most of the Si cap was oxidized.



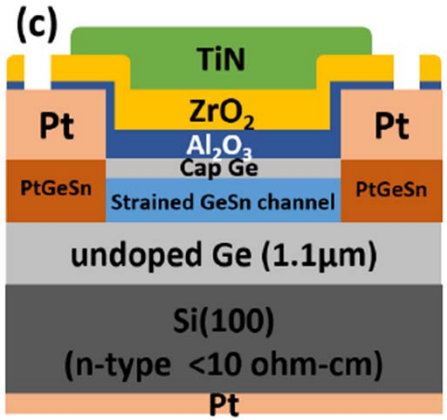
IEEE Symposium on VLSI Technology, 2014, pp. 100.
IEEE Electron Device Letters, v. 37, pp. 701, 2016.
IEEE Transactions on Electron Devices, v. 61, pp. 3639 - 3645, 2014.
Semiconductor Science and Technology, vol. 29, pp. 115027, Nov. 2014.

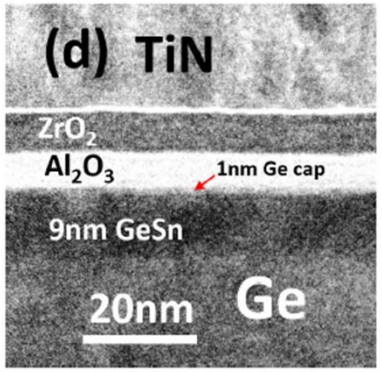
Strained GeSn Quantum Well pMOSFETs

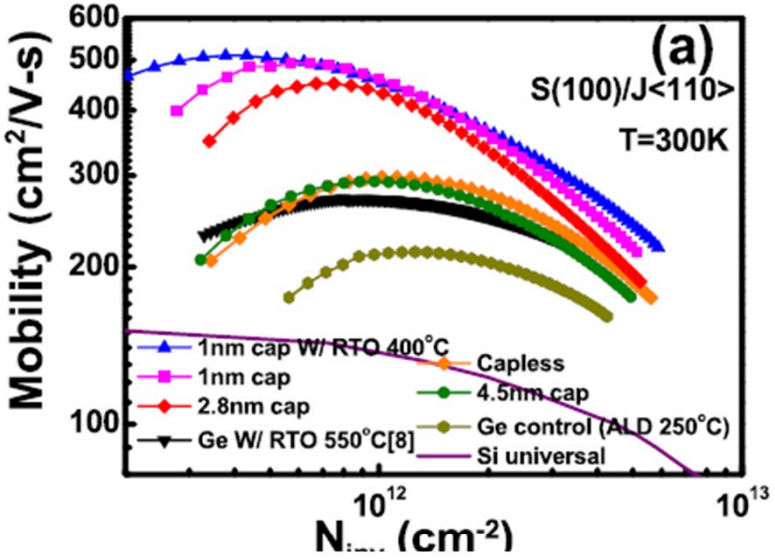
G. Han and Y. Hao *et al., IEEE Symposium on VLSI Technology, 2014, pp. 100.*



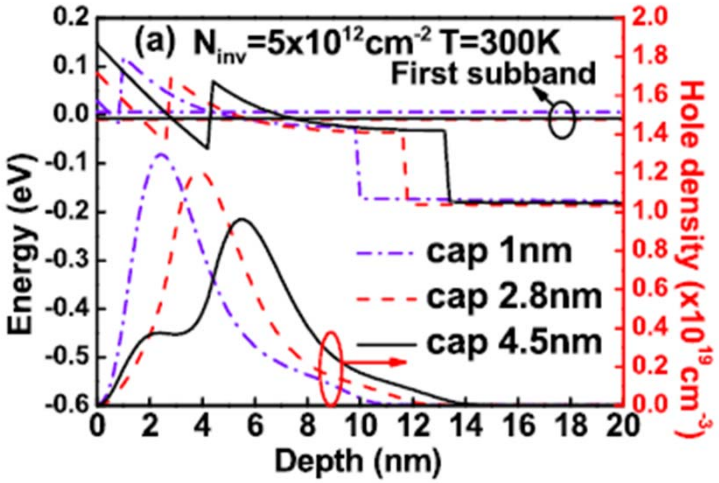
Strained GeSn Quantum Well pMOSFETs







- Y-S Huang *et al.*, High mobility CVD Grown Ge/Strained $Ge_{0.9}Sn_{0.1}$/Ge Quantum Well pMOSFETs on Si By Optimizing Ge Cap Thickness, IEEE TED, 2017.
- Y.-S Huang et al., IEDM 2016.



Outline

- Non-Si Microelectronics（非硅微电子学）
  - More Moore
  - More than Moore
- High Mobility Ge and GeSn MOSFETs
- Beyond CMOS
  - GeSn Tunneling FETs
  - Ge and GeSn Negative Capacitance FETs
  - Piezoelectric FETs
- Summary

Beyond CMOS实现超低功耗

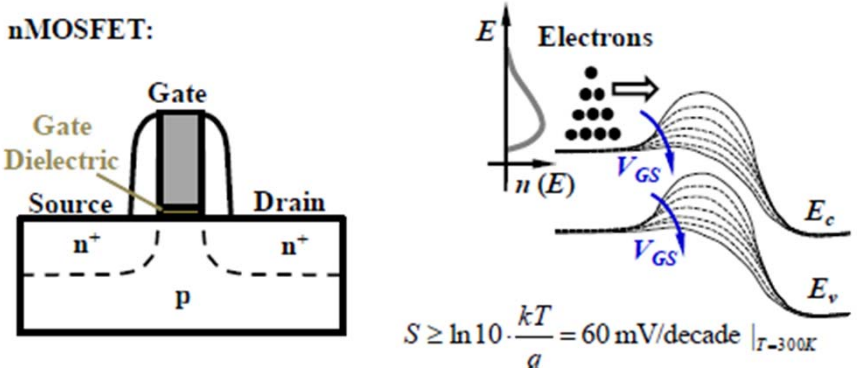
- Increased I_{off} causes increased static power consumption.

$$P_{static} = W \cdot I_{off} \cdot V_{DD}$$

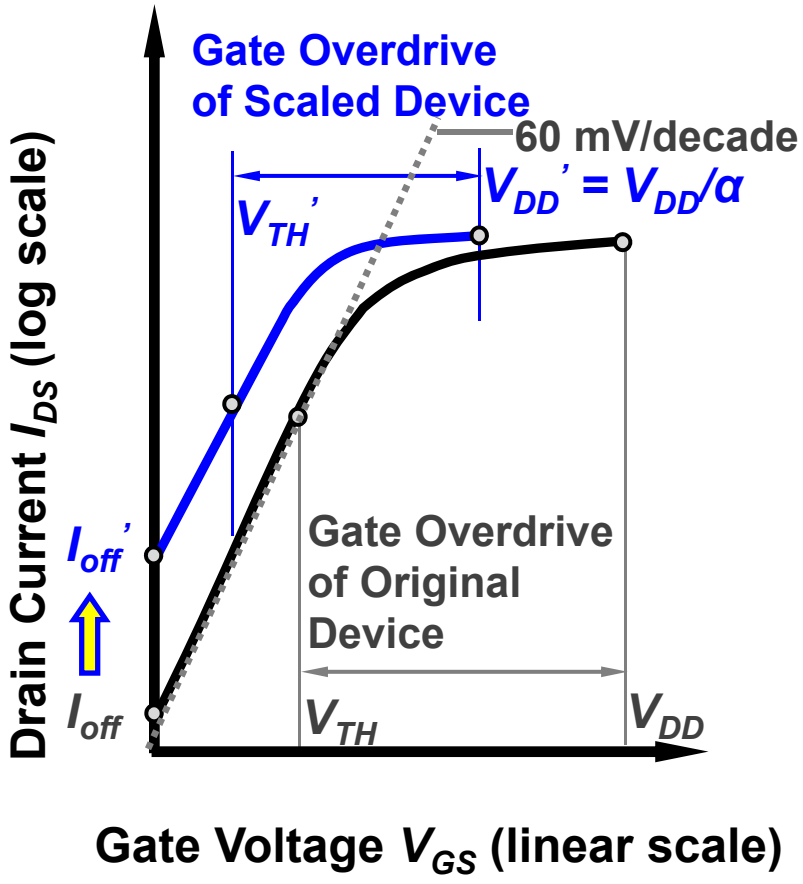
- Nonscalability of suthreshold swing (S).

$$S = \ln 10 \frac{kT}{q}\left(\frac{C_{ox} + C_D}{C_{ox}}\right)$$

$$\geq 60 \text{ mV/decade } (T = 300\,\text{K})$$



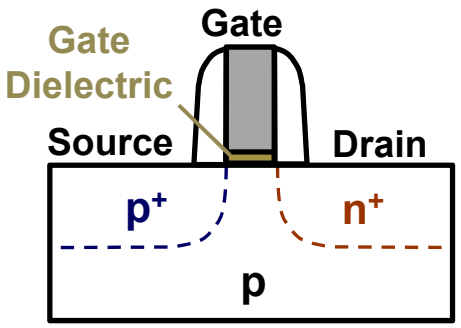
Fundamental Limit of Scaling



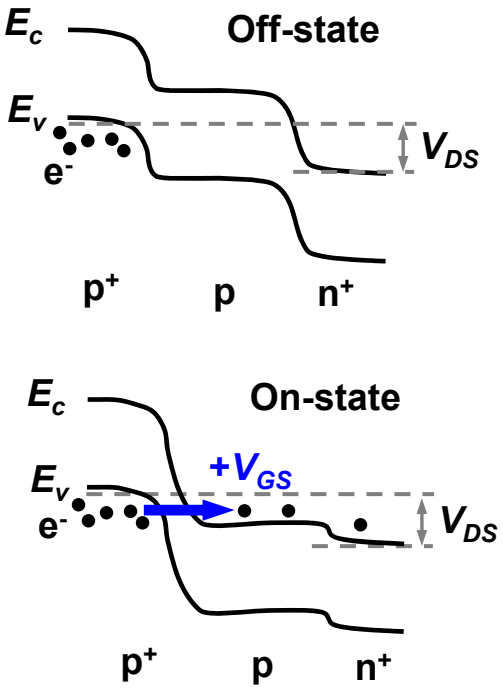
Beyond CMOS : Tunneling FET

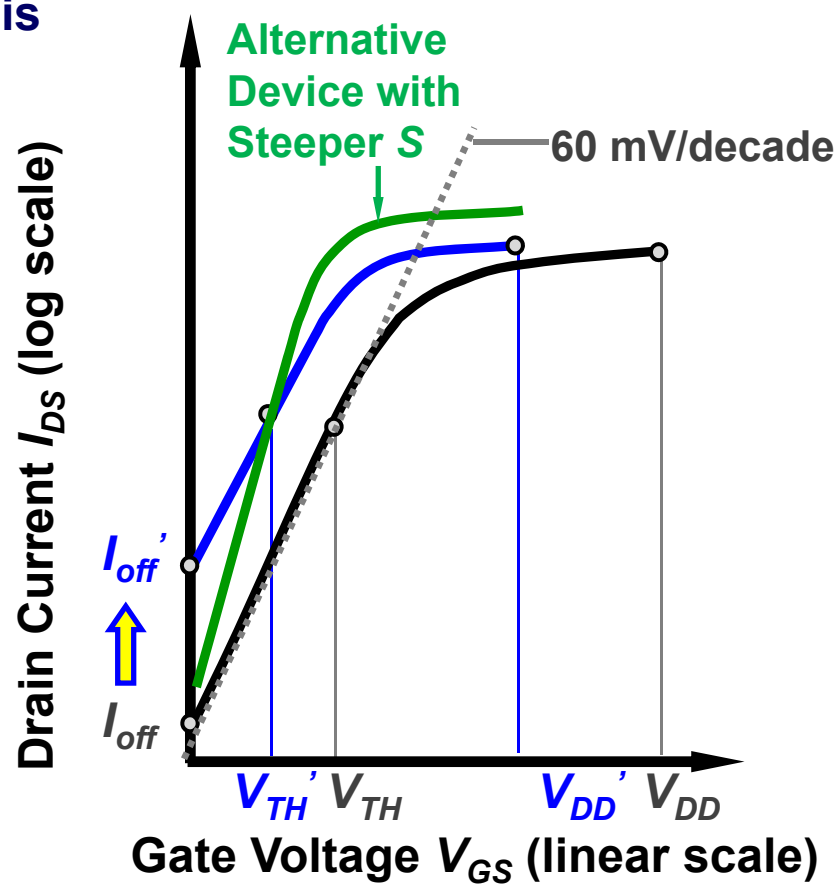
- Alternative device with steeper *S* is promising to overcome CMOS limitation.
- Tunneling Field-Effect Transistor (TFET) is one of the most promising candidates.

TFET:
gated p-i-n diode

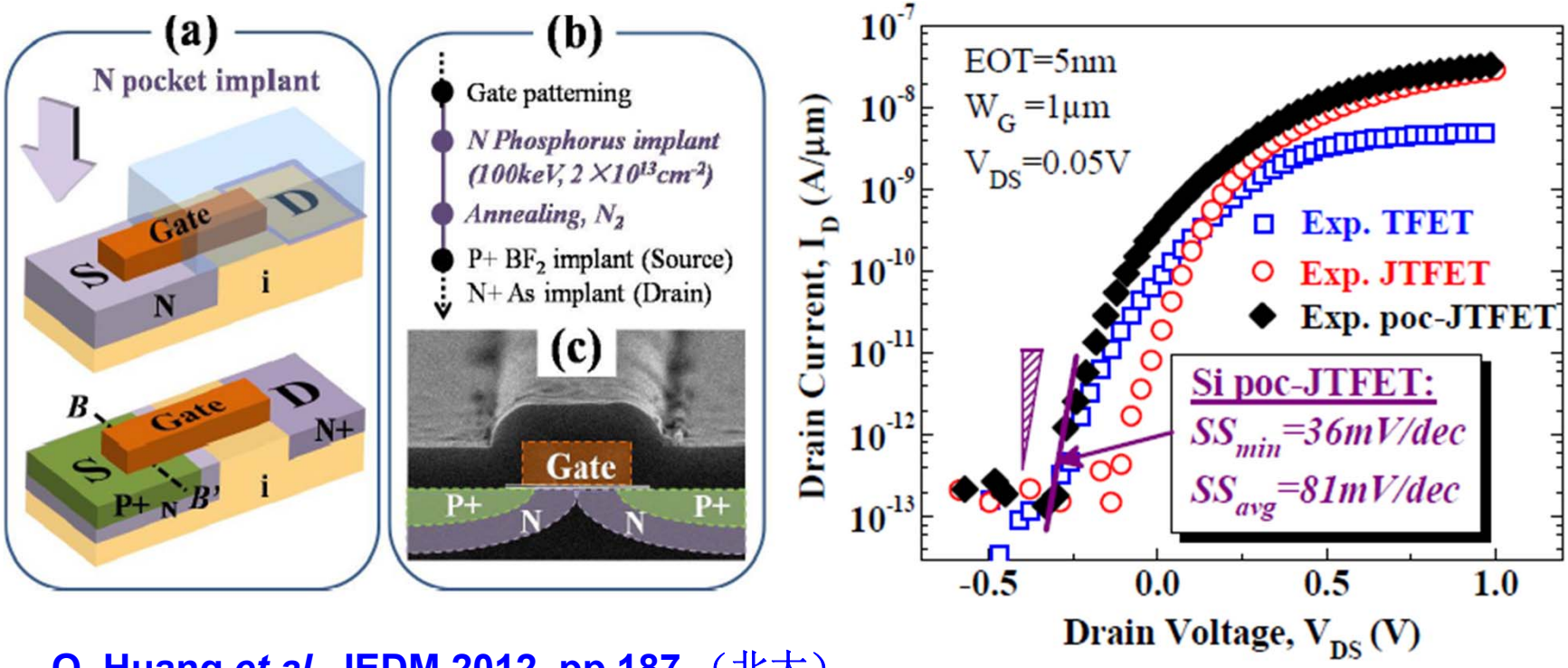


Quantum Band-to-band Tunneling (BTBT) of Electrons from E_v to E_c





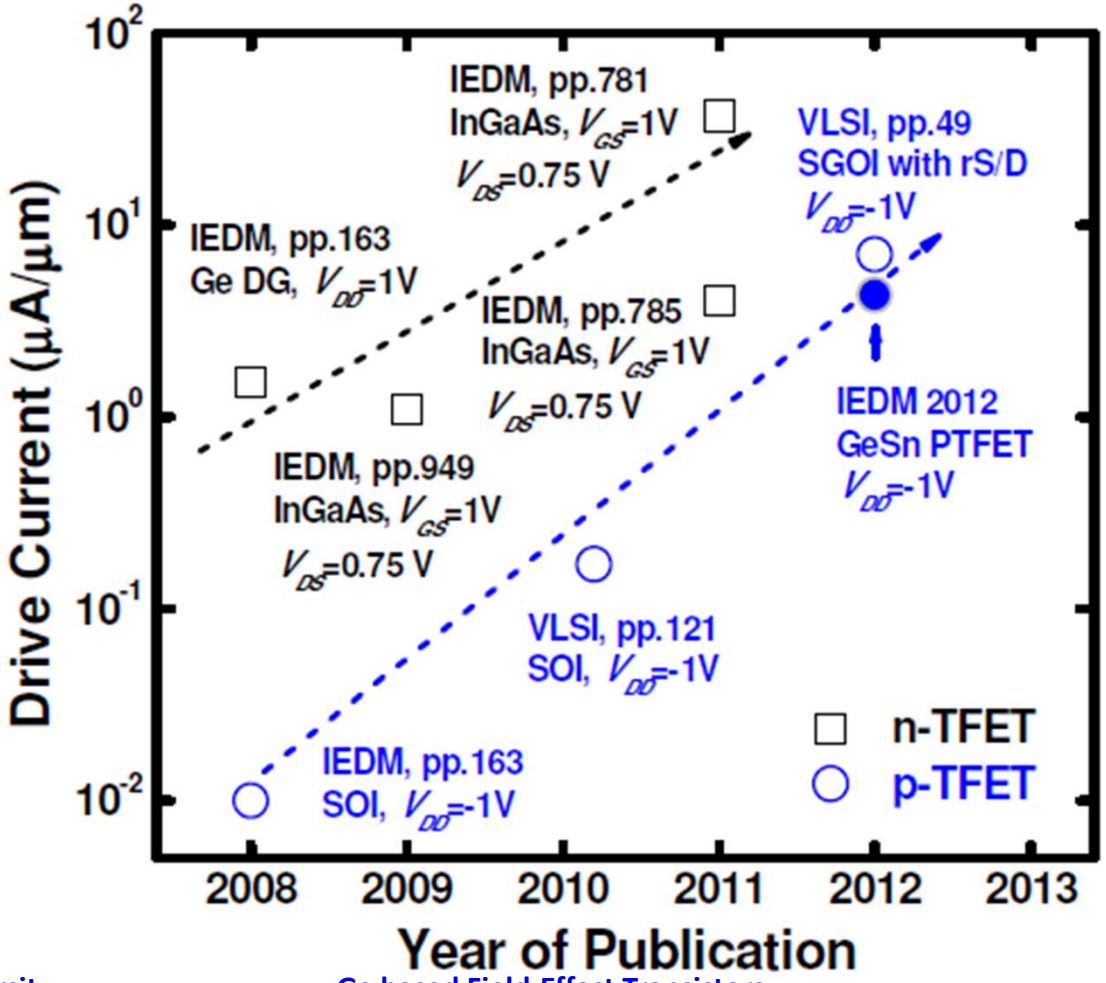
Beyond CMOS：Tunneling FET



Q. Huang *et al.*, IEDM 2012, pp.187 （北大）
Y. Zhao *et al., IEEE EDL, v.38, no. pp.540, 2017*
Q. Huang *et al.*, IEDM 2015, pp.22.2.1
Q. Huang *et al.*, IEDM 2011, pp.16.2.1 （北大）

First GeSn Tunneling FETs

G. Han *et al.*, "Towards Direct Band-to-Band Tunneling in P-Channel Tunneling Field Effect Transistor (TFET): Technology Enablement by Germanium-Tin (GeSn) " IEDM 2012, pp.379-382

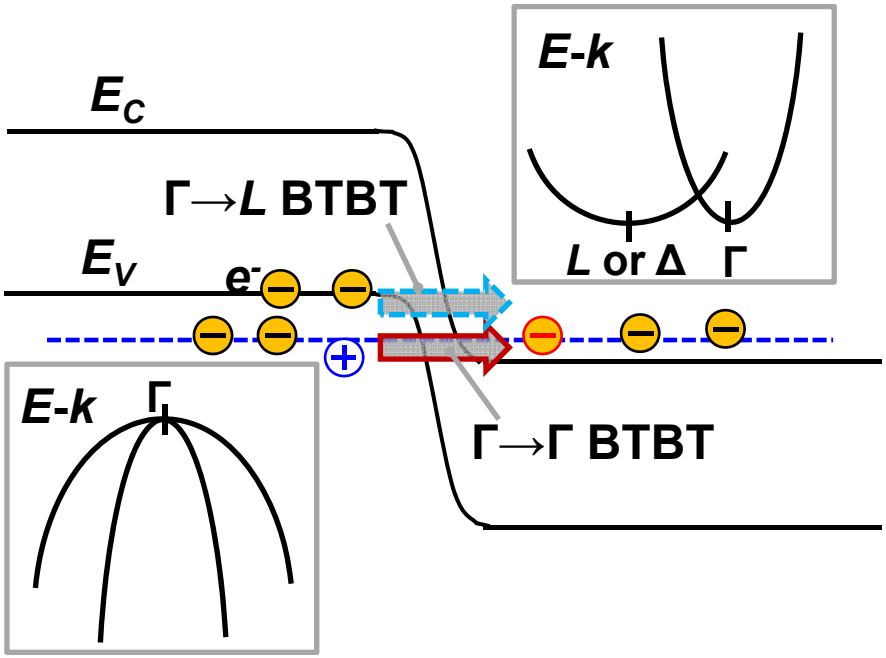


GeSn Tunneling FETs

Why Germanium-tin (GeSn) alloy?

Proper material for TFET application:

- Small band-gap (Ge, GeSn, InGaAs, InAs, graphene)
- Direct band-gap (InGaAs, InAs, GeSn alloy)



GeSn Tunneling FETs

Why Germanium-tin (GeSn) alloy?

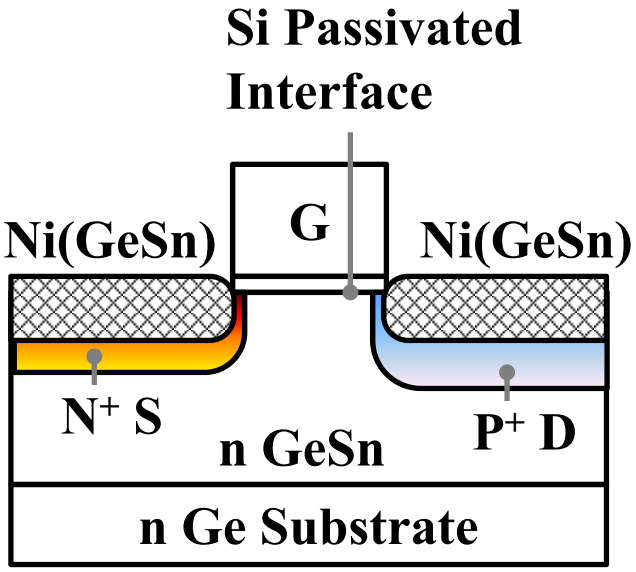
Proper material for TFET application:

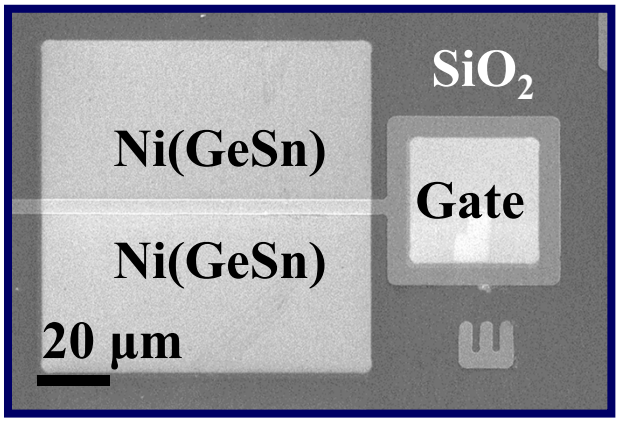
- Small band-gap (Ge, GeSn, InGaAs, InAs, graphene)
- Direct band-gap (InGaAs, InAs, GeSn alloy)
- Group IV material is preferred in CMOS compatible process

Comparison of III-V, SiGe, GeSn for TFET application

	III-V	SiGe	GeSn
Small E_G	√	×	√
Direct BTBT	√	×	√
High interface quality	×	√	√
Easy Integration on Si	×	√	√

GeSn Tunneling FETs (IEDM 2012)



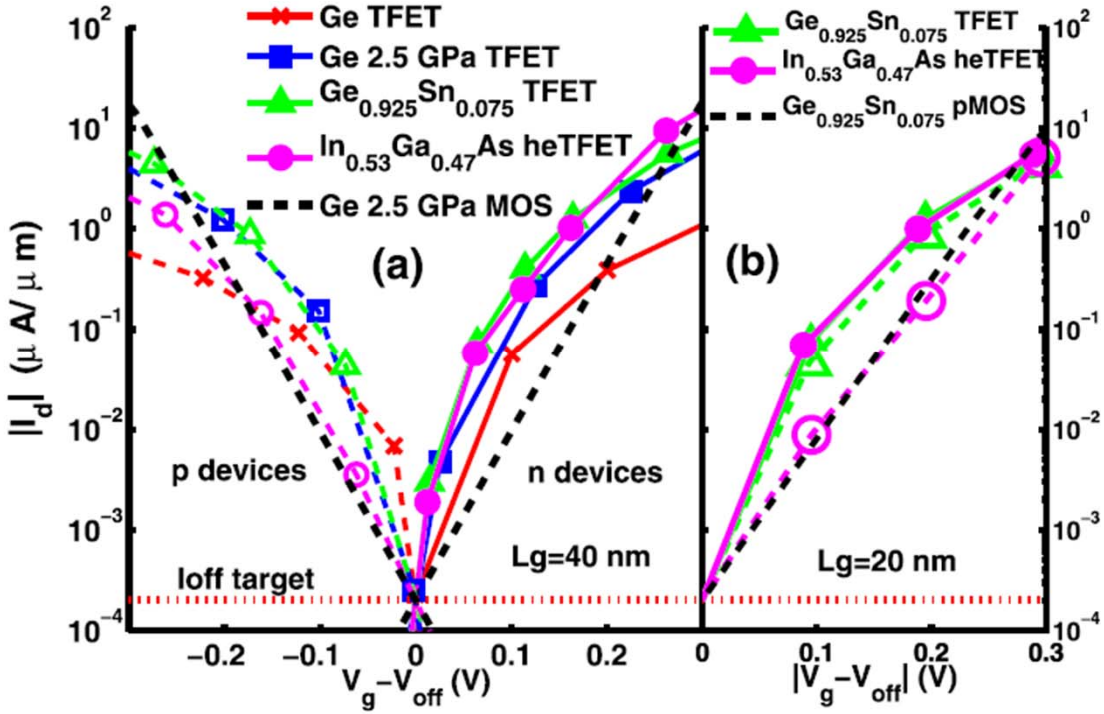


	Device Structure	*Gate Length* L_G	Supply Voltage V_{DD} (V)	I_{ON} (µA/µm)
Ref [7]	GOI TFET	100 nm	V_{DS} = - 0.8 V, V_{GS}-V_{BTBT} = -1V	1
Ref [8]	Si TFET	160 nm	- 1.0 V	0.15
Ref [9]	Si TFET	20 µm	- 1.0 V	0.17
Ref [10]	Strained Ge TFET	700 nm	V_{DS} = -1.5 V, V_{GS}-V_{BTBT} = -1V	0.006
Ref [11]	SiGe/SOI TFET with Raised S/D	200 nm	- 1.0 V	7
This Work	GeSn TFET	3 µm	- 1.0 V	4.34

G. Han *et al.*, the world's first GeSn TFET, IEDM 2012, pp.379-382

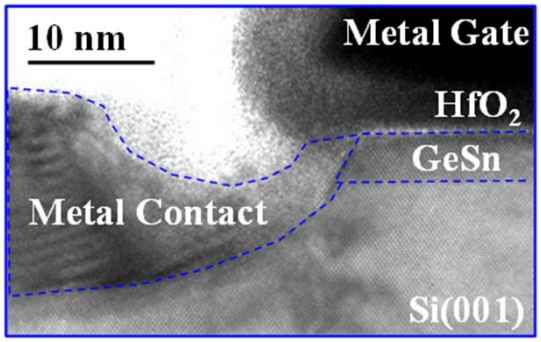
GeSn Tunneling FETs (IEDM 2012)

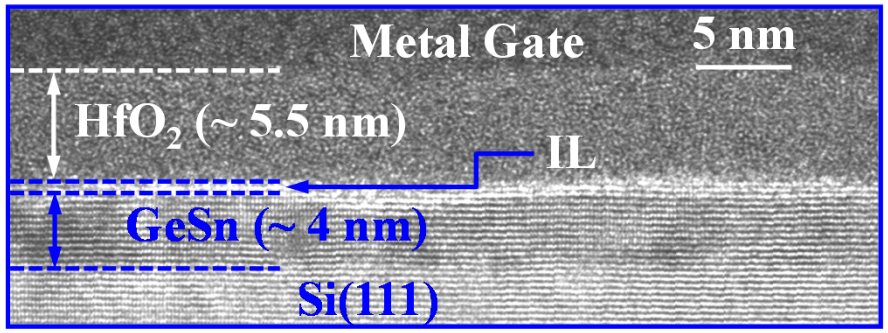
Highlighted by Intel! R. Kotlyar et al., *Applied Physics Letters*, 102, 113106 (2013).

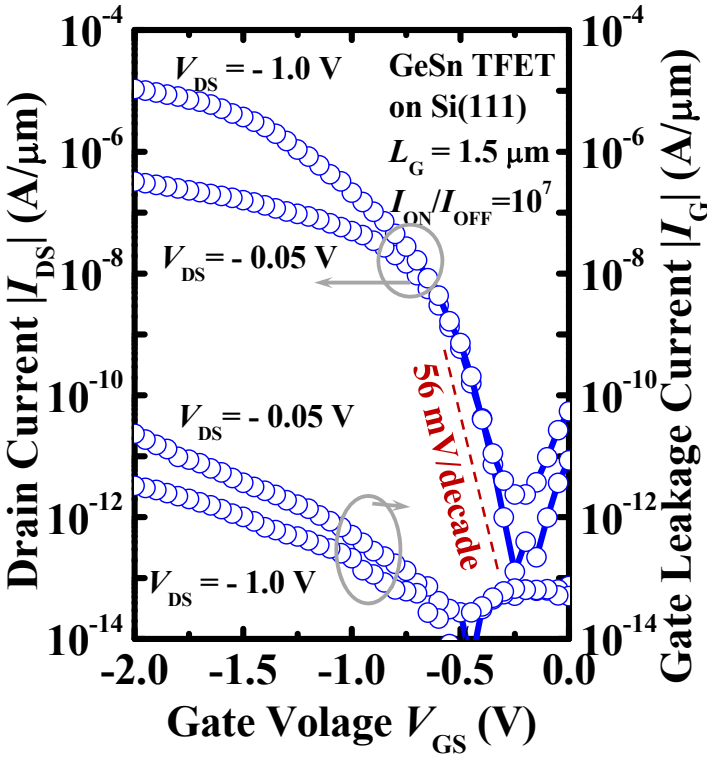


The group IV devices with the engineered direct band gap are promising candidates to realize the complementary TFET scaled logic for low power applications.

GeSn Tunneling FETs on Silicon (西电)







- H. Wang *et al.*, *SSDM*, 2017.
- H. Wang *et al.*, *IEEE TED*, v.64, no.7, pp.2804, 2017.
- Y. Wang *et al.*, *IEEE TED*, v.64, no.4, pp.1541, 2017.
- H. Wang *et al.*, *JJAP*, v. 56, no.4s, pp. 04CD07, 2017.
- H. Wang *et al.*, *JJAP*, vol. 55, pp. 04ED13, 2016.
- H. Wang *et al.*, *IEEE TED*, v.63, pp.303, 2016.
- G. Han *et al.*, *IEEE EDL*, vol. 37, pp. 701, 2016.
- H. Wang *et al.*, *SSDM*, 2016 pp. 47 - 48.
- M. Liu *et al.*, *IEEE TED*, vol.62, pp. 1262, 2015.
- H. Wang *et al.*, *SSDM*, 2015, pp. K-15.
- Y. Yang *et al.*, *IEEE TED*, v. 60, pp. 4048, 2013.
- Y. Yang *et al.*, *JAP*, vol. 113, pp. 194507, 2013.
- Y. Yang *et al.*, *IEEE IEDM* 2012, pp. 379.
- G. Han *et al.*, *APL*, v. 98, pp. 153502, 2011.
- P. Guo *et al.*, *IEEE EDL*, v. 30, pp. 981, 2009.
- M. Liu *et al.*, *IEEE VLSI-TSA* 2015, pp. TR33.
- H. Wang *et al.*, *IEEE VLSI-TSA* 2015, pp. TR32.
- G. Han *et al.*, *IEEE VLSI-TSA* 2012.

Outline

- Non-Si Microelectronics（非硅微电子学）
  - More Moore
  - More than Moore
- High Mobility Ge and GeSn MOSFETs
- Beyond CMOS
  - GeSn Tunneling FETs
  - Ge and GeSn Negative Capacitance FETs
  - Piezoelectric FETs
- Summary

Negative Capacitance (NC) in Ferroelectric (FE) Gate Dielectric

S. Salahuddin *et al.*, Use of negative capacitance to provide voltage amplification for low power nanoscale devices, *Nano Letters*, v.8, pp. 405, 2008.

Subthreshold Swing

$$SS = \frac{\partial V_{GS}}{\partial (\log_{10} I_{DS})} = \frac{\partial V_{GS}}{\partial \psi_s} \frac{\partial \psi_s}{\partial (\log_{10} I_{DS})}$$

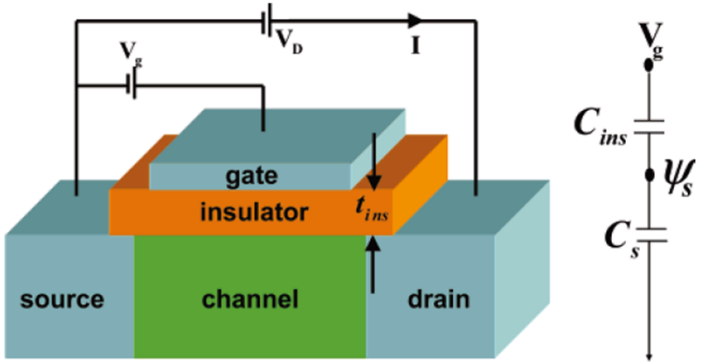
$$= \left(1 + \frac{C_s}{C_{ins}}\right) \times 60 mV / dec.$$

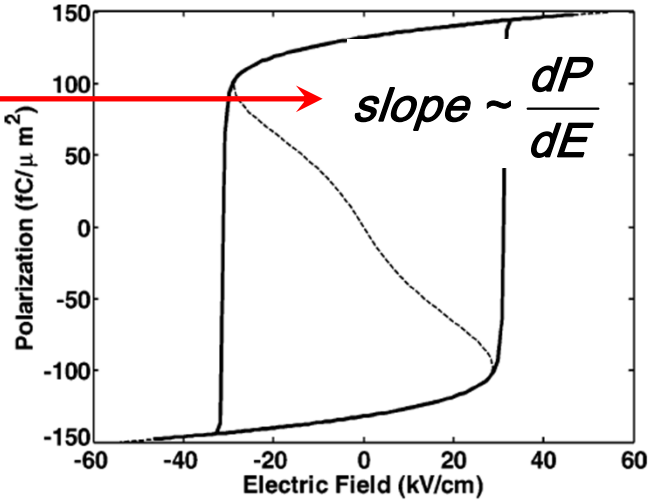
Internal Gate Gain

$$\frac{\partial \psi_s}{\partial V_{GS}} > 1$$

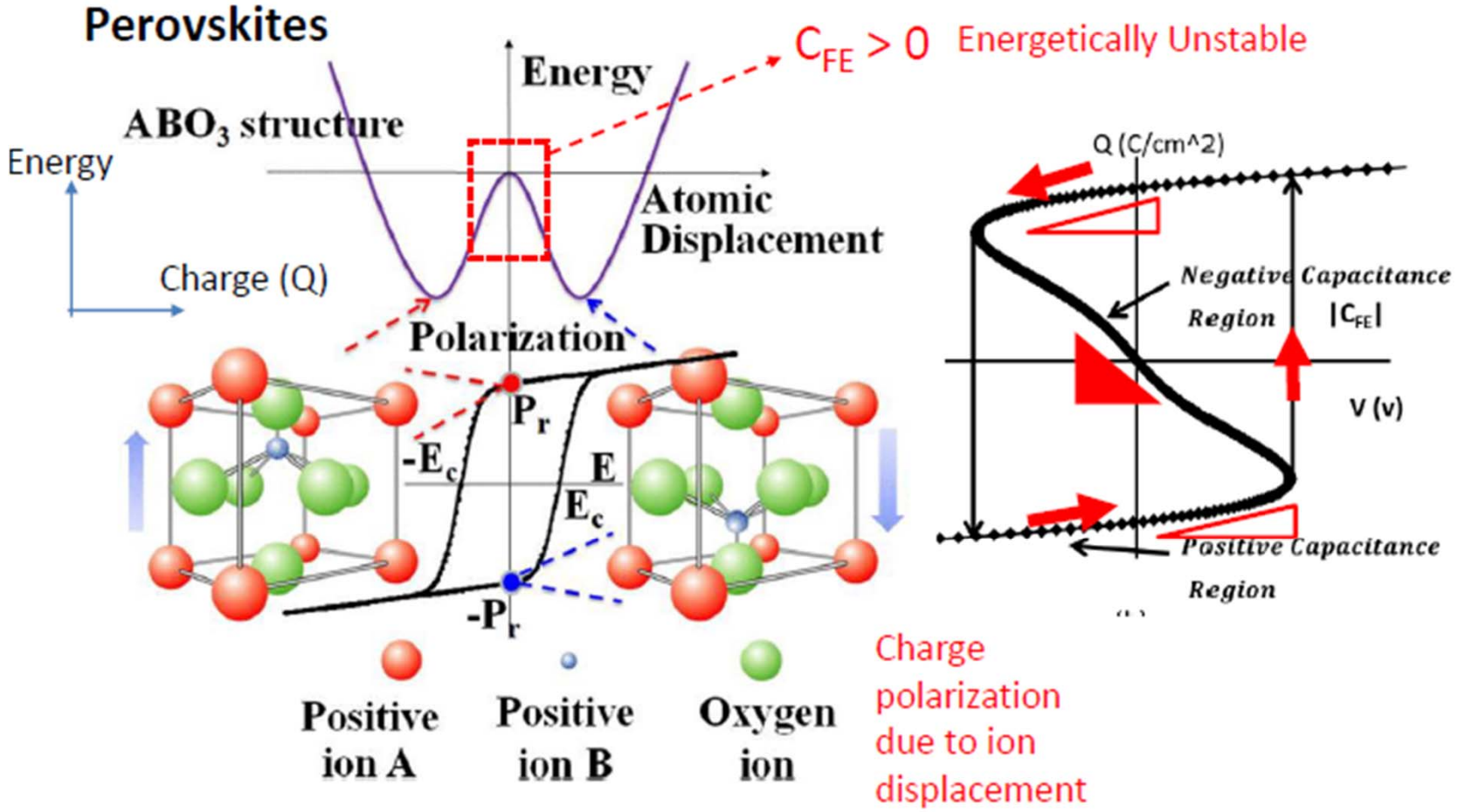
$C_{ins} < 0$

SS < 60 mV/decade



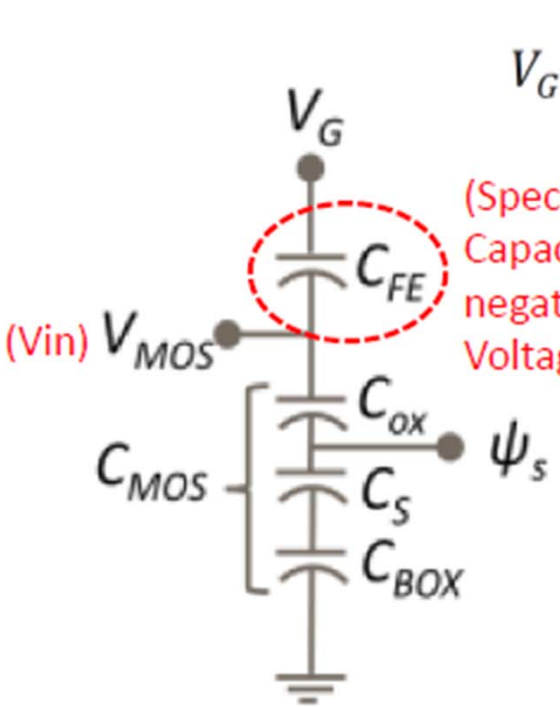


Negative Capacitance by Ferroelectrics



- Ferroelectric states determined by field-induced ion displacement
- Negative capacitance state is between stable ferroelectric states
- Needs special material & operation design to stabilize

Theoretical Studies on Negative Capacitance Transisotrs



(Special Internal Capacitor that turns negative to provide Voltage gain)

$$V_G\ Amplification = Av = \frac{\partial V_{MOS}}{\partial V_G} = \frac{|C_{FE}|}{|C_{FE}| - C_{MOS}}$$

$C_{FE} \sim C_{MOS} \rightarrow$ Max. Av

$$C_G = \frac{C_{FE}C_{MOS}}{C_{FE}+C_{MOS}} = \frac{-|C_{FE}|C_{MOS}}{|C_{FE}|-C_{MOS}}$$

$$NCFET\ SS = MOSFET\ SS * \frac{1}{Av} = 60mV/dec * \left(1+\frac{C_{dep}}{C_{ox}}\right) * \frac{1}{Av}$$

$$= 60mV/dec * \left(1 + \frac{C_{dep}}{C_{ox}} - \frac{C_{dep}}{|C_{FE}|}\right)$$

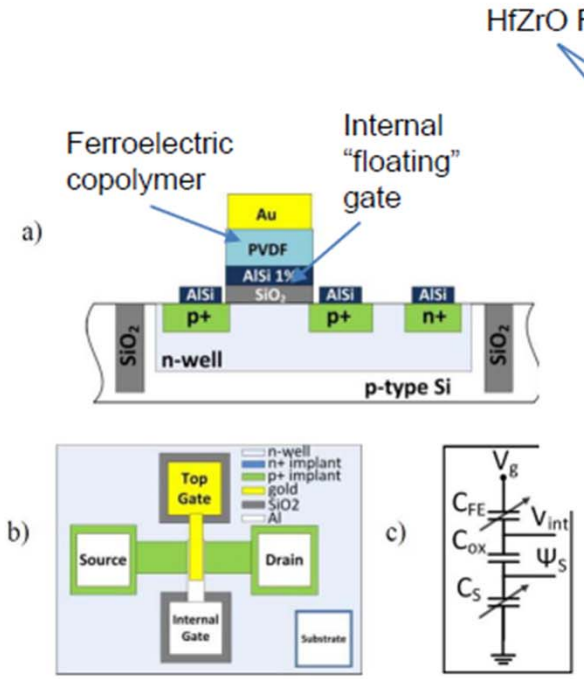
-ve cap effect

S < 60mV/dec
$C_{dep}/|C_{FE}| > C_{dep}/|C_{ox}| \Rightarrow |C_{FE}| > C_{ox}$

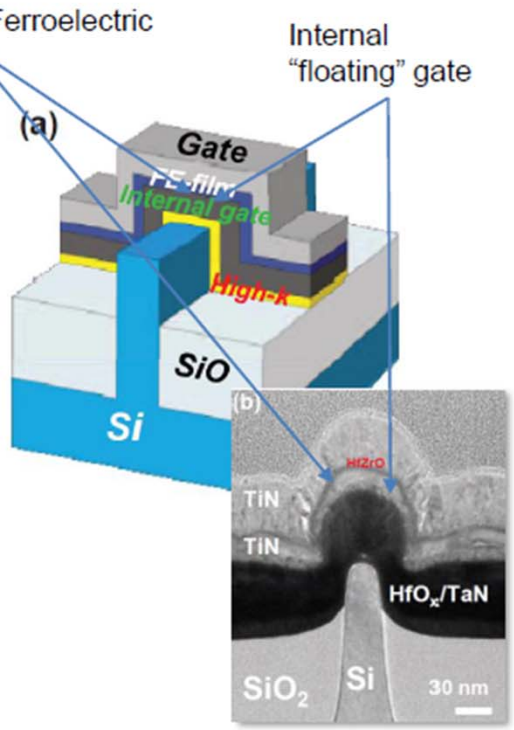
S < 0 (Unstable)
$C_{dep}/|C_{FE}| < C_{dep}/|C_{ox}| + 1$

Chun Wing Yeung; et. al. "Device design considerations for ultra-thin body non-hysteretic negative capacitance FETs," Symp. Energy Efficient Electronic Systems (E3S), 2013 Third Berkeley Year: 2013, Pages: 1 - 2

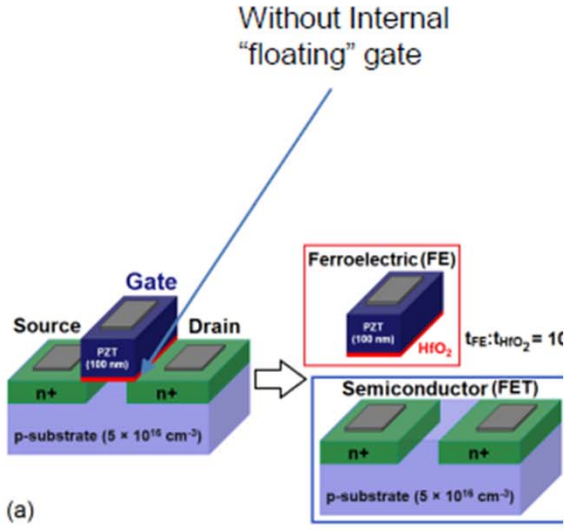
Some Device Structures



A. Rusu et al. *IEDM 2010* pp. 16.3.1–16.3.4. (Adrian Ionescu EPFL)



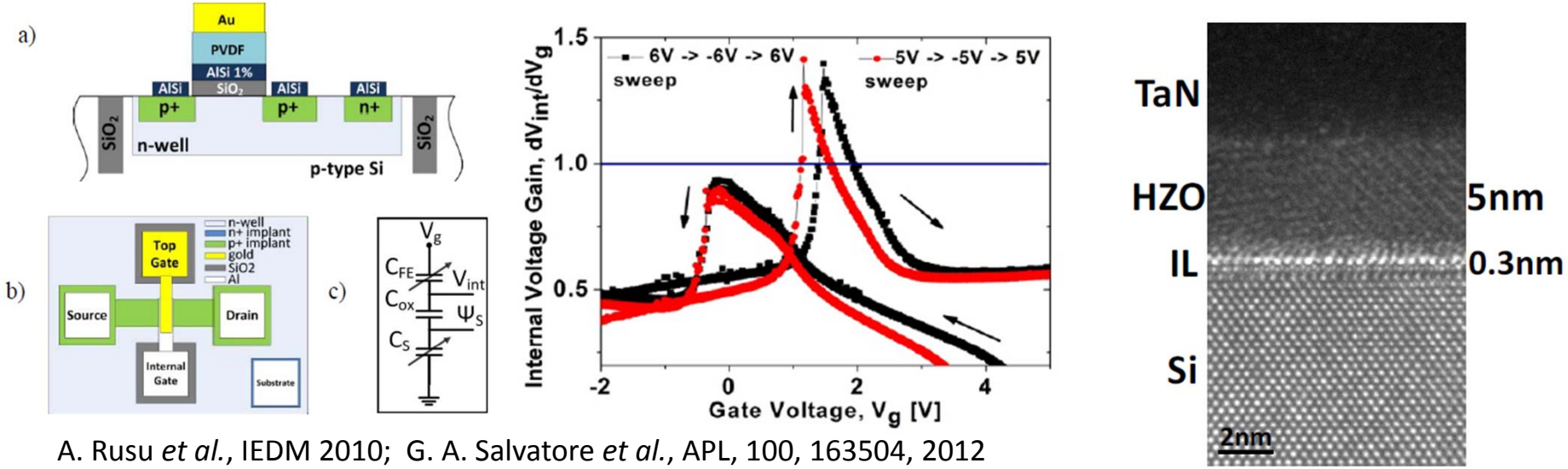
Li et al. *IEDM 2015* pp. 22.6.1–22.6.4. (C.Hu & S. Salahudin Berkeley)



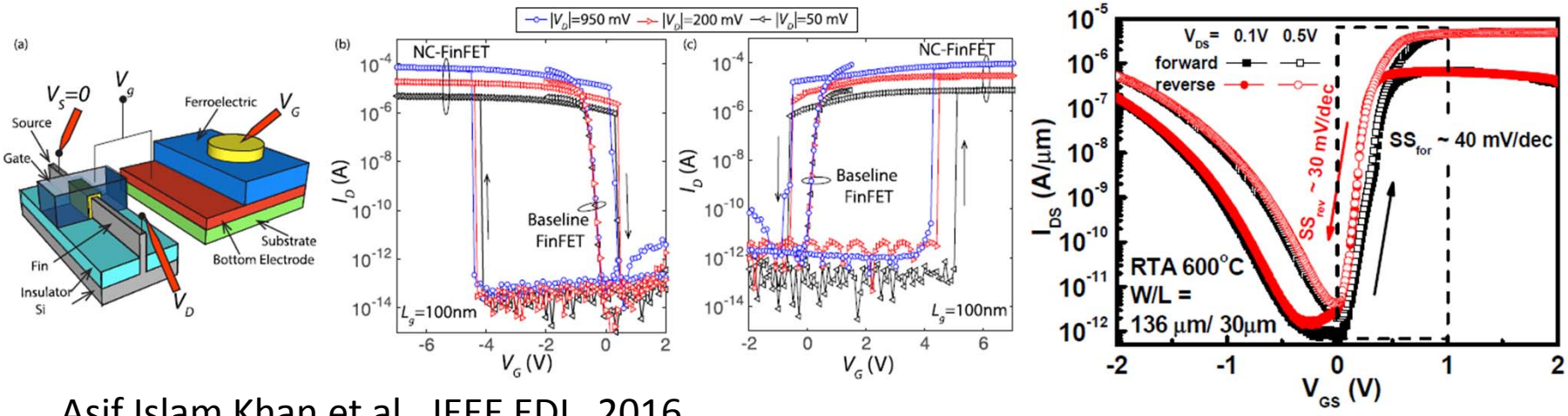
S. Dasgupta et. al. EEE Journal on Exploratory Solid-State Computational Devices and Circuits
Year: 2015, Volume: 1
Pages: 43 – 48 (S. Datta Penn State)

- Essentially a Ferroelectric Capacitor in series with metal-gate capacitor
- Internal gate introduced to (a) probe internal Fe-Cap (b) Equipotential interface to mitigate depolarization from transistor channel/SD regions, to achieve uniform field despite FE domain formation? Floating voltage node sensitive to leakage.
- No internal gate: Sensitive to FE-gate-Oxide trap density

Some Device Structures



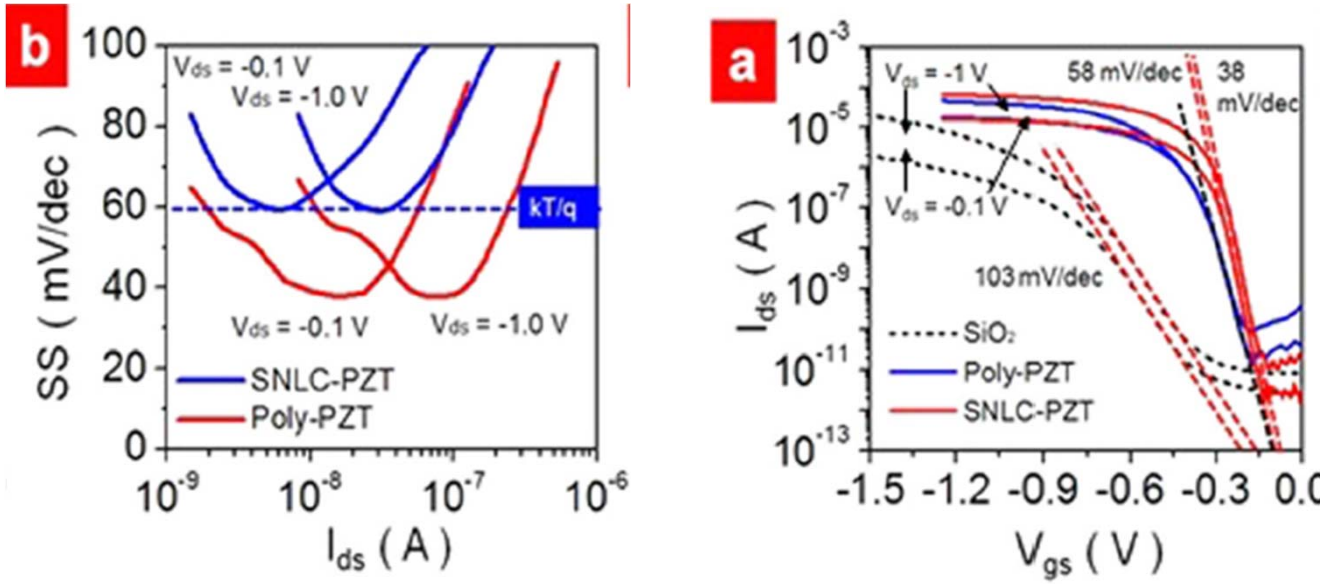
A. Rusu *et al.*, IEDM 2010; G. A. Salvatore *et al.*, APL, 100, 163504, 2012



Asif Islam Khan et al., IEEE EDL, 2016

M. H. Lee, IEDM 2015

Some Device Structures（造假）



Retraction: "Sub-kT/q subthreshold slope p-metal-oxide-semiconductor field-effect transistors with single-grained $Pb(Zr,Ti)O_3$ featuring a highly reliable negative capacitance" [Appl. Phys. Lett. 108, 103504 (2016)]

Jae Hyo Park[1,2] and Seung Ki Joo[1,2]
[1]*Department of Material Science and Engineering, Seoul National University, Seoul 151-742, South Korea*
[2]*Eui-San Research Center, Research Institute of Advanced Materials (RIAM), Seoul National University, Seoul 151-742, South Korea*

(Received 20 January 2017; accepted 24 January 2017; published online 17 February 2017)

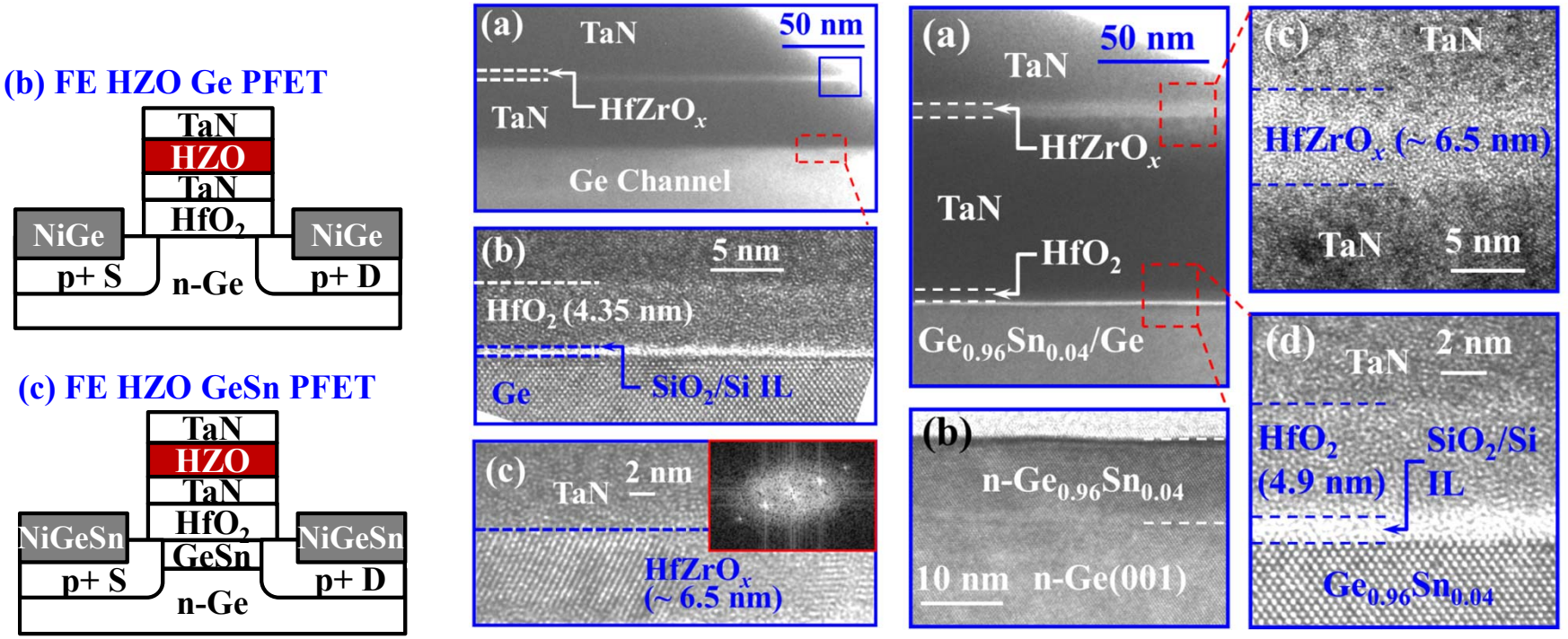
[http://dx.doi.org/10.1063/1.4975639]

The authors wish to retract the referenced article due to duplication of figures and significant overlap with other publications by the authors[1–3] and because of concerns about the accuracy of the description of the devices and materials from which the reported results were obtained.[4] The authors recognize that these represent serious errors and sincerely apologize for any inconvenience they may have caused.

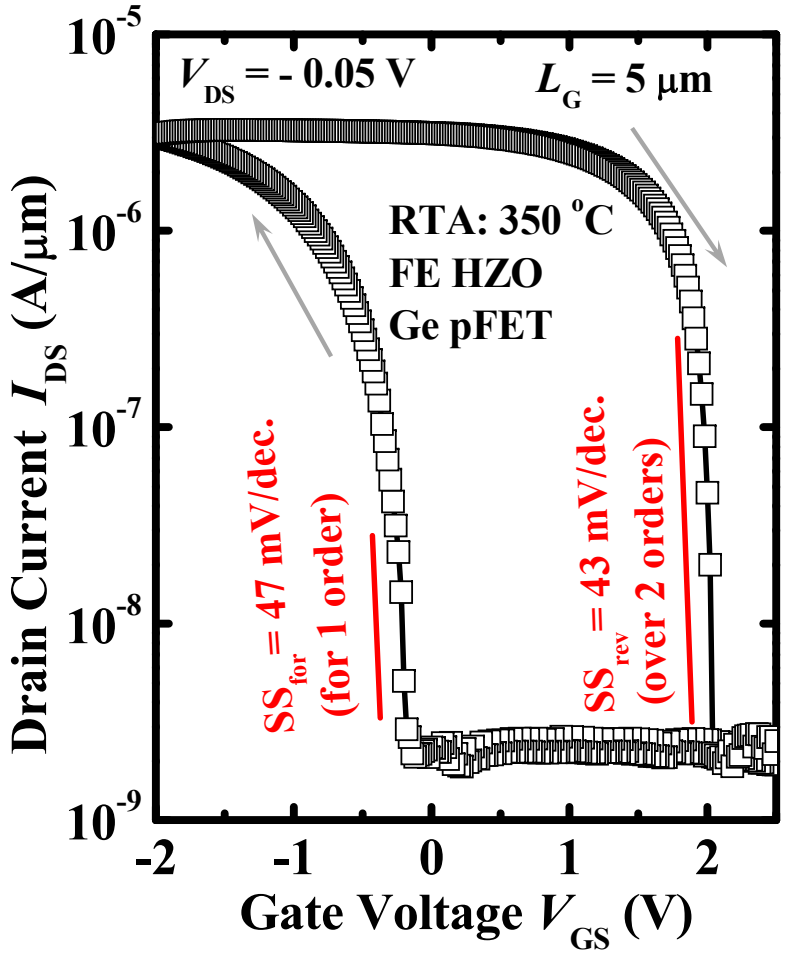
[1]J. H. Park and S. K. Joo, IEEE Electron Device Lett. **36**, 1033 (2015).
[2]J. H. Park, H. Y. Kim, G. S. Jang, D. Ahn, and S. K. Joo, J. Phys. D: Appl. Phys. **49**, 075106 (2016).
[3]J. H. Park, H. Y. Kim, G. S. Jang, K. H. Seok, H. J. Chae, S. K. Lee, Z. Kiaee, and S. K. Joo, Sci. Rep. **6**, 23189 (2016).
[4]J. H. Park and S. K. Joo, Appl. Phys. Lett. **108**, 103504 (2016).

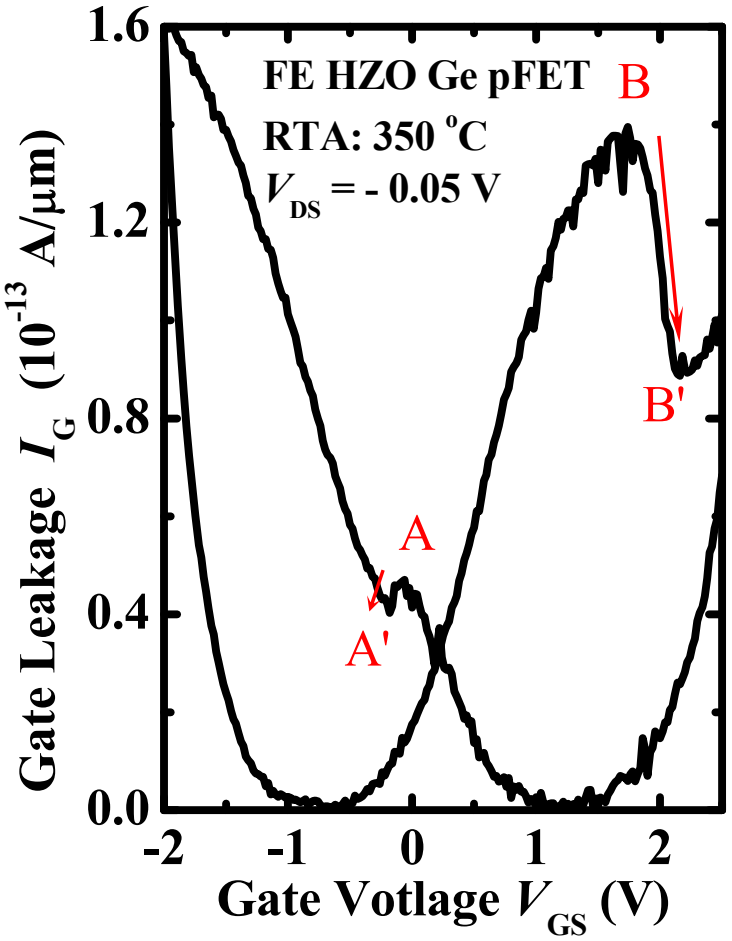
Negative Capacitance Ge PMOSFET

Jiuren Zhou *et al.*, "Ferroelectric $HfZrO_x$ Ge and GeSn PMOSFETs with Sub-60 mV/decade Subthreshold Swing, Negligible Hysteresis, and Improved I_{DS}," ***IEEE International Electron Devices Meeting***, San Francisco, CA, USA, Dec. 2016, pp.310-313, 2016.



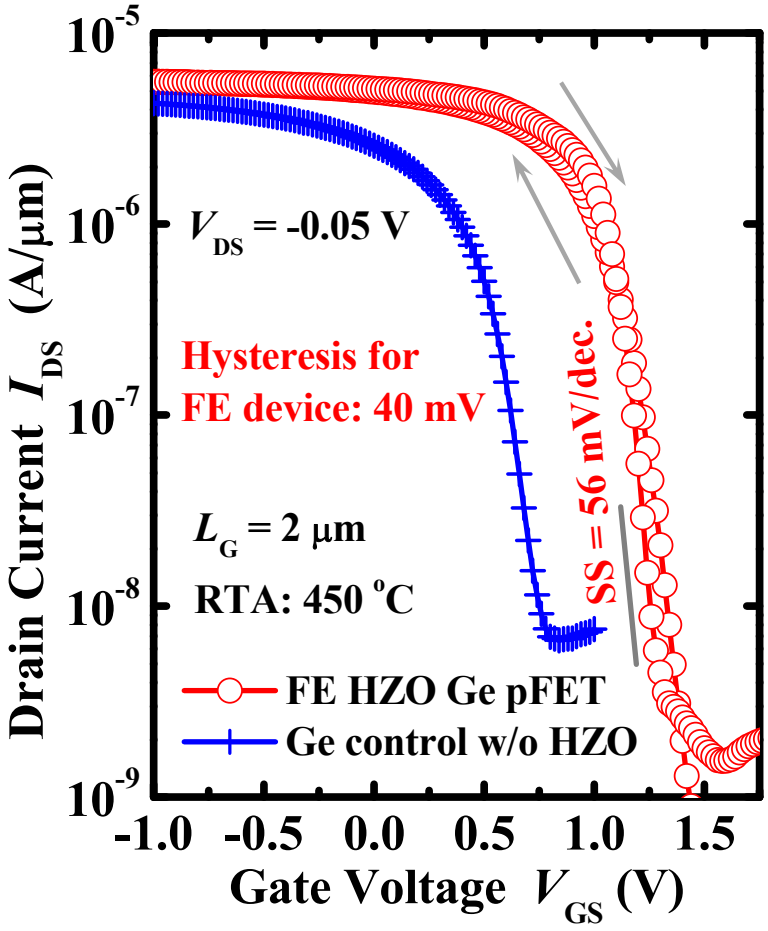
Negative Capacitance Ge PMOSFETs: I_{DS}-V_{GS} at 350 °C RTA

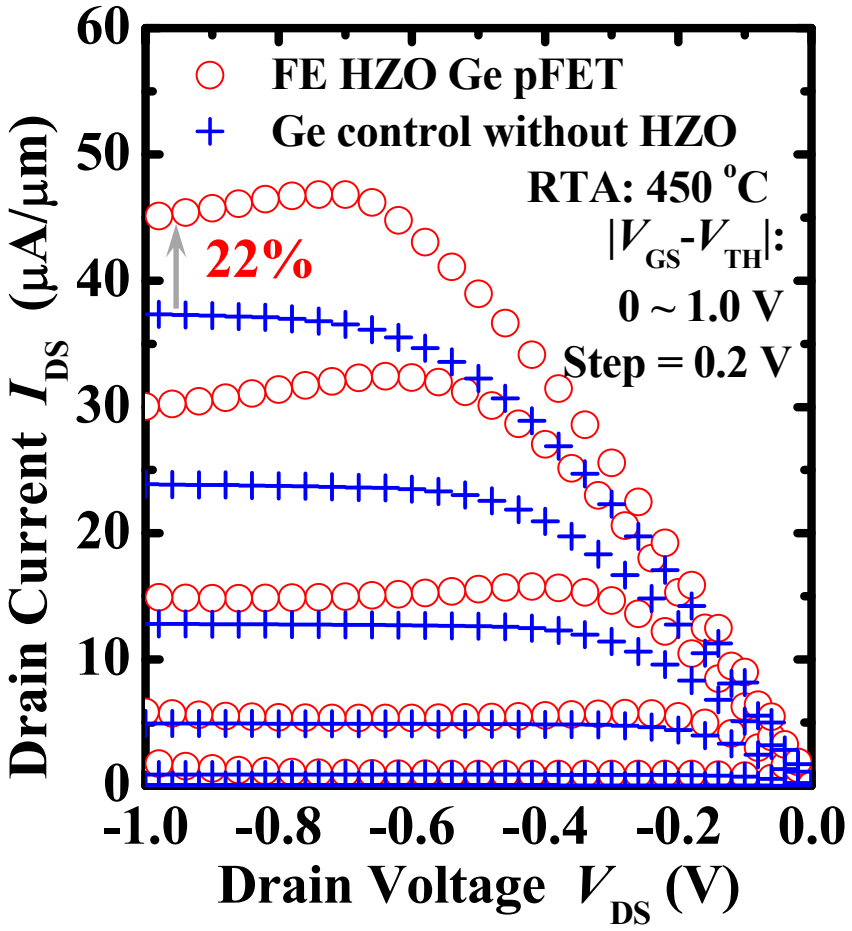




J. Zhou *et al.*, IEDM 2016, p.310

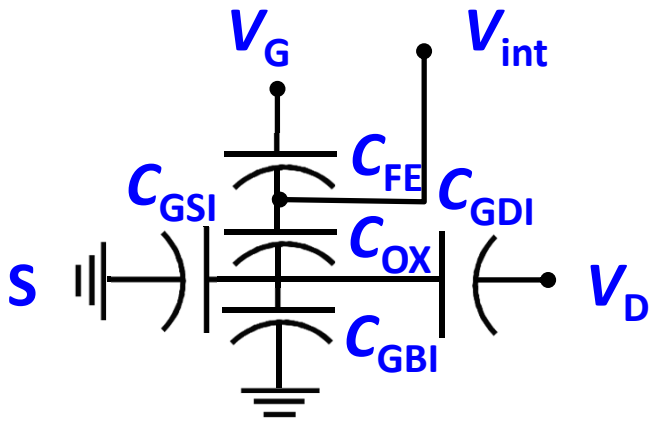
Negative Capacitance Ge PMOSFETs: I_{DS}-V_{GS} at 450 °C RTA



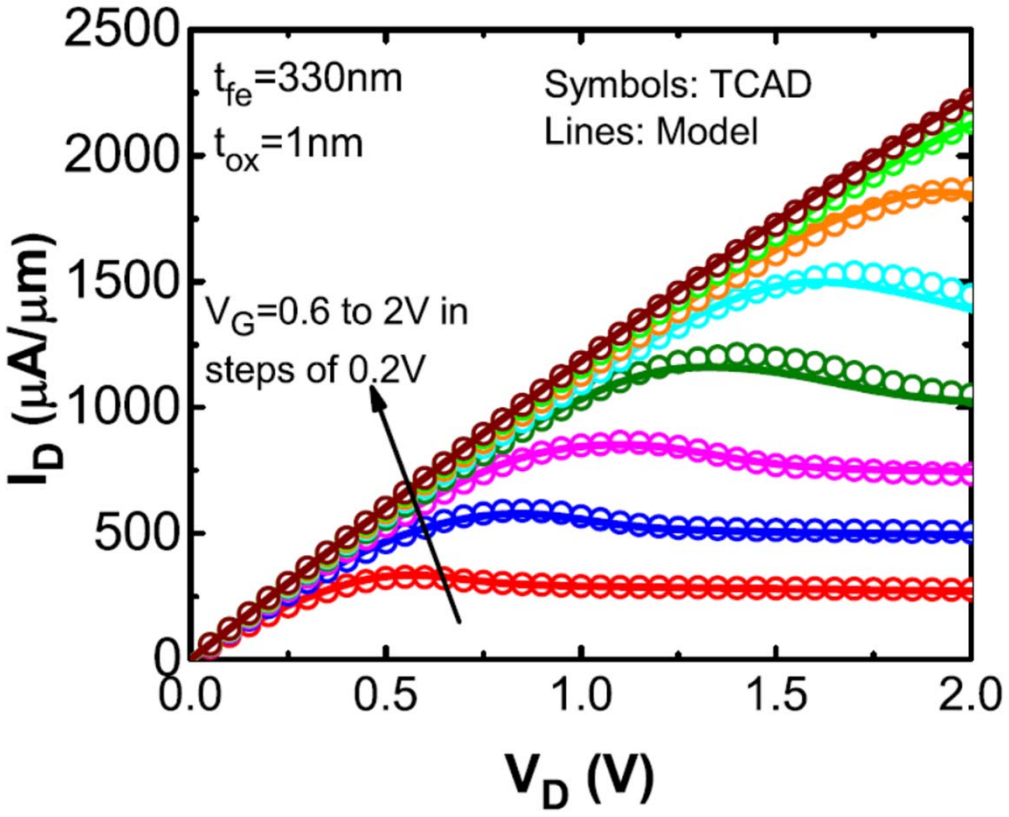


J. Zhou *et al.*, IEDM 2016, p.310

Negative Differential Resistance (NDR) in I_{DS}-V_{DS}



G. Pahwa *et al.*, TED, 2016;
H. Ota et al., IEDM, 2016



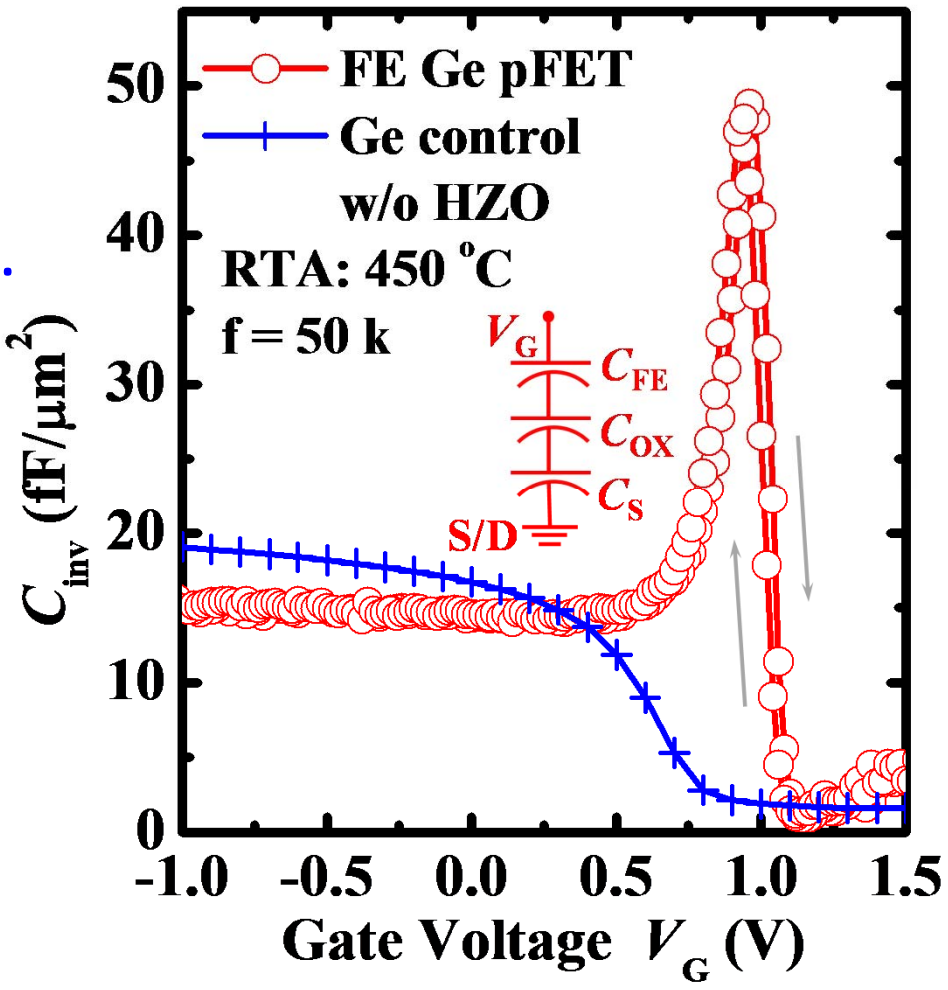
Negative Capacitance Ge PMOSFETs: Negative Capacitance

$$C_G = \frac{C_{FE}C_{MOS}}{C_{FE}+C_{MOS}} = \frac{-|C_{FE}|C_{MOS}}{|C_{FE}|-C_{MOS}}$$

C. Hu *et al.*, DRC, pp. 39, 2015;
M. H. Lee *et al.*, IEDM, 2015, pp. 616

Theoretically, it could induce a peak in the C-V curve of the gate stack; it could be also responsible of the increase of the current in the strong inversion regime or of the lowering of the subthreshold slope below the 60 mV/dec limit.

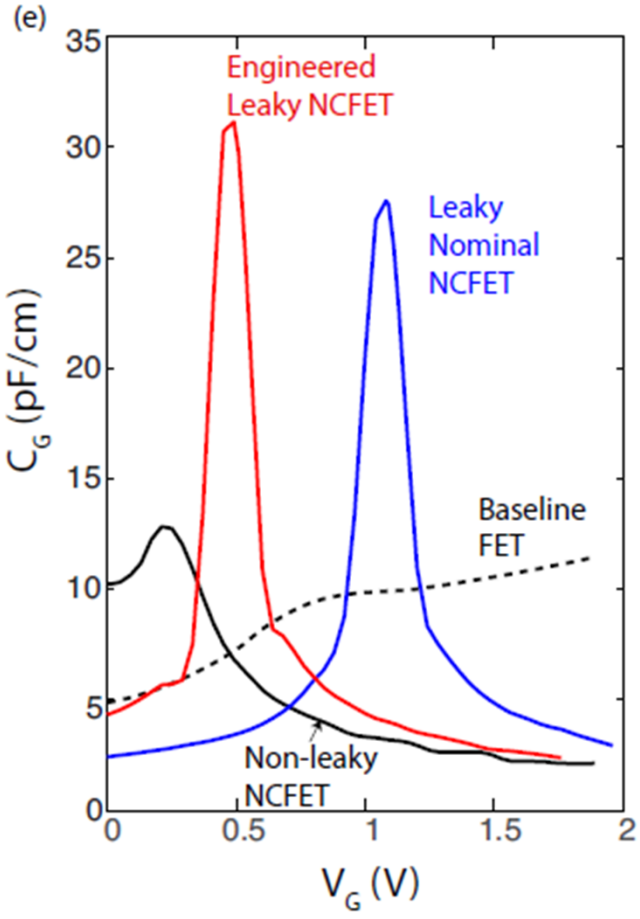
G. A. Salvatore *et al.*, APL, 100, 163504, 2012



Negative Capacitance Ge PMOSFETs: Negative Capacitance

- G. Pahwa *et al.*, IEEE Trans. Electron Devices, vol. 64, no. 3, pp. 1366 - 1374, 2017.
- A. I. Khan et al., IEEE Electron Device Lett., 2017, published online. DOI: 10.1109/LED.2017.2733382

The peaks indicate the onset of NC-state as in [8] and their appearance at different V_G due to leakage are consistent with the IV-characteristics shown in fig. 3(b).



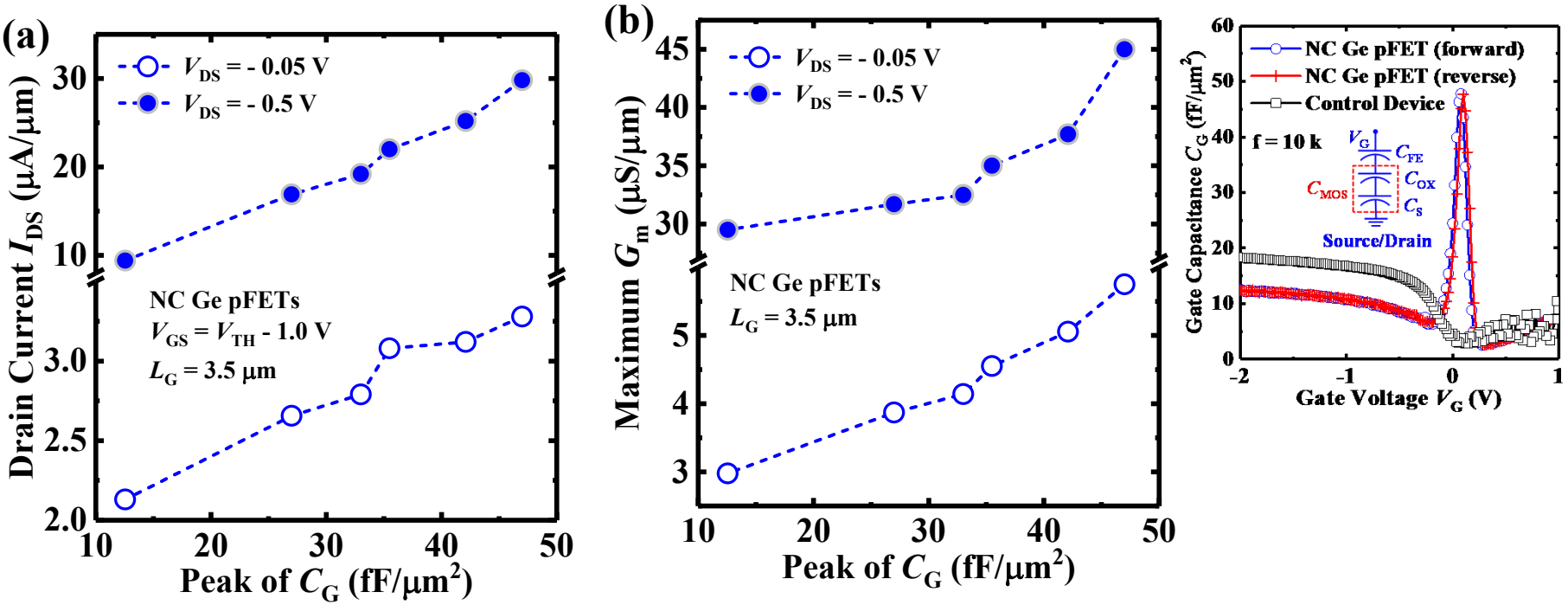
Negative Capacitance Ge PMOSFETs: Negative Capacitance

$$V_G\ Amplification = Av = \frac{\partial V_{MOS}}{\partial V_G} = \frac{|C_{FE}|}{|C_{FE}| - C_{MOS}}$$

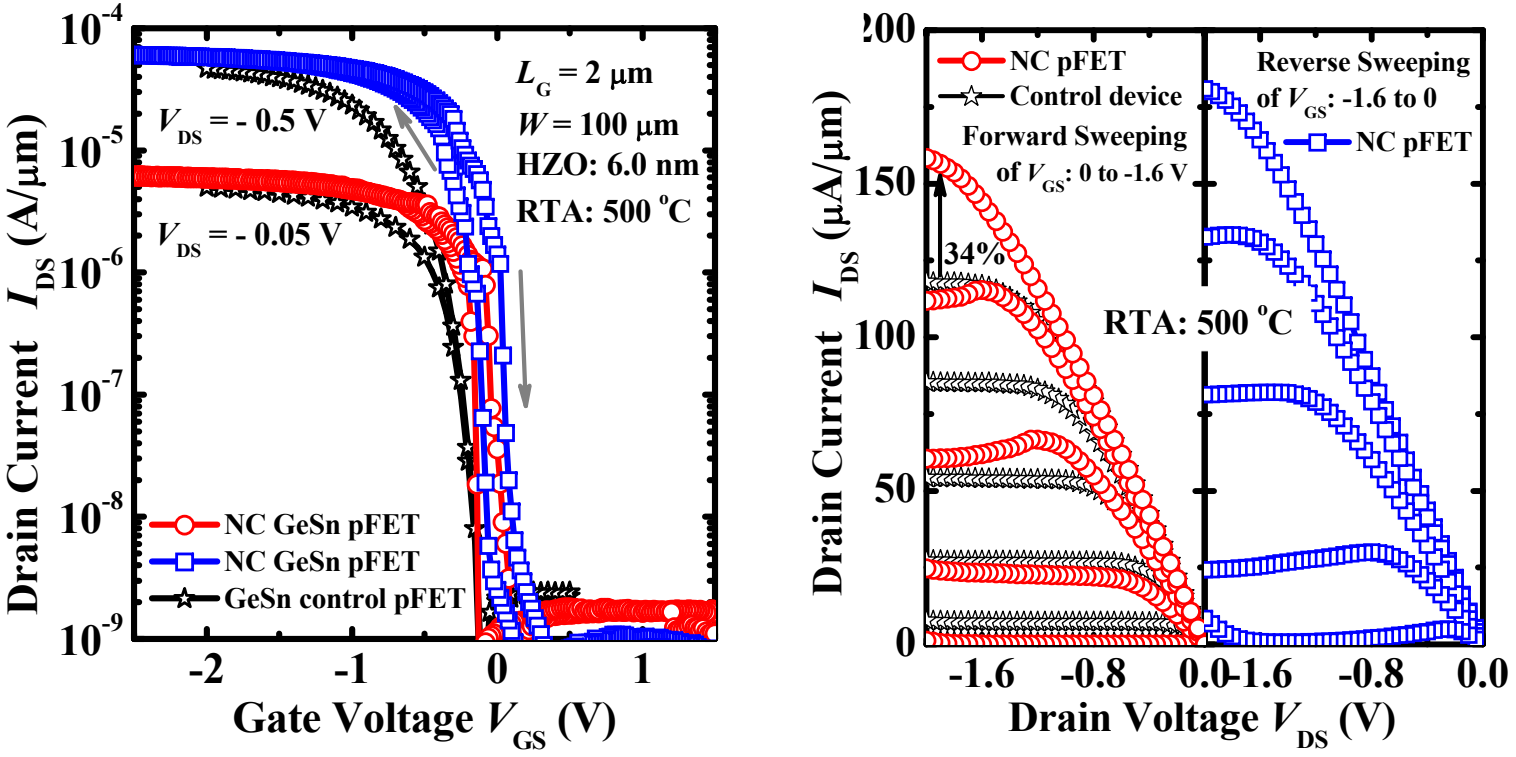
$C_{FE} \sim C_{MOS} \rightarrow$ Max. Av

$$C_G = \frac{C_{FE}C_{MOS}}{C_{FE}+C_{MOS}} = \frac{-|C_{FE}|C_{MOS}}{|C_{FE}|-C_{MOS}}$$

Jing Li and Jiuren Zhou *et al.*, Correlation of Gate Capacitance with Drive Current and Transconductance in Negative Capacitance Ge PFETs, IEEE EDL, Accepted.

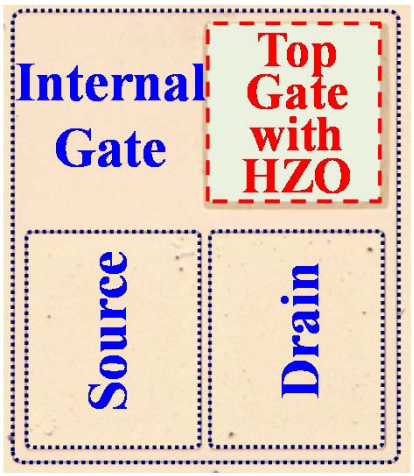


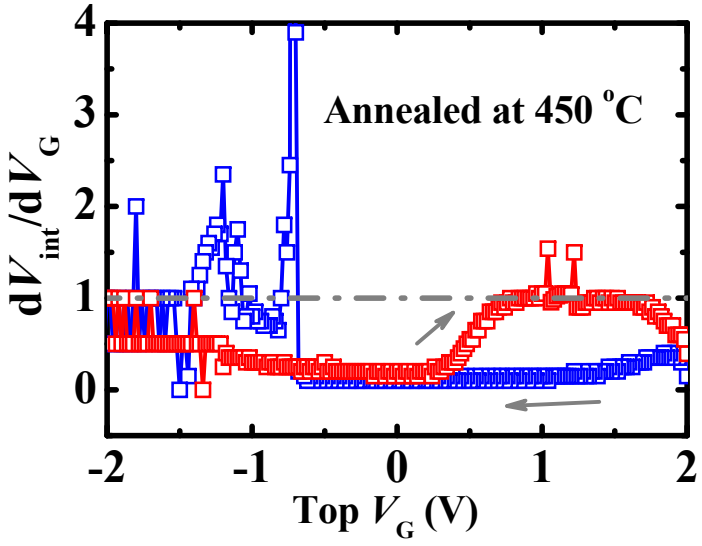
GeSn Quantum Well NC pFET with Sub-20 mV/decade

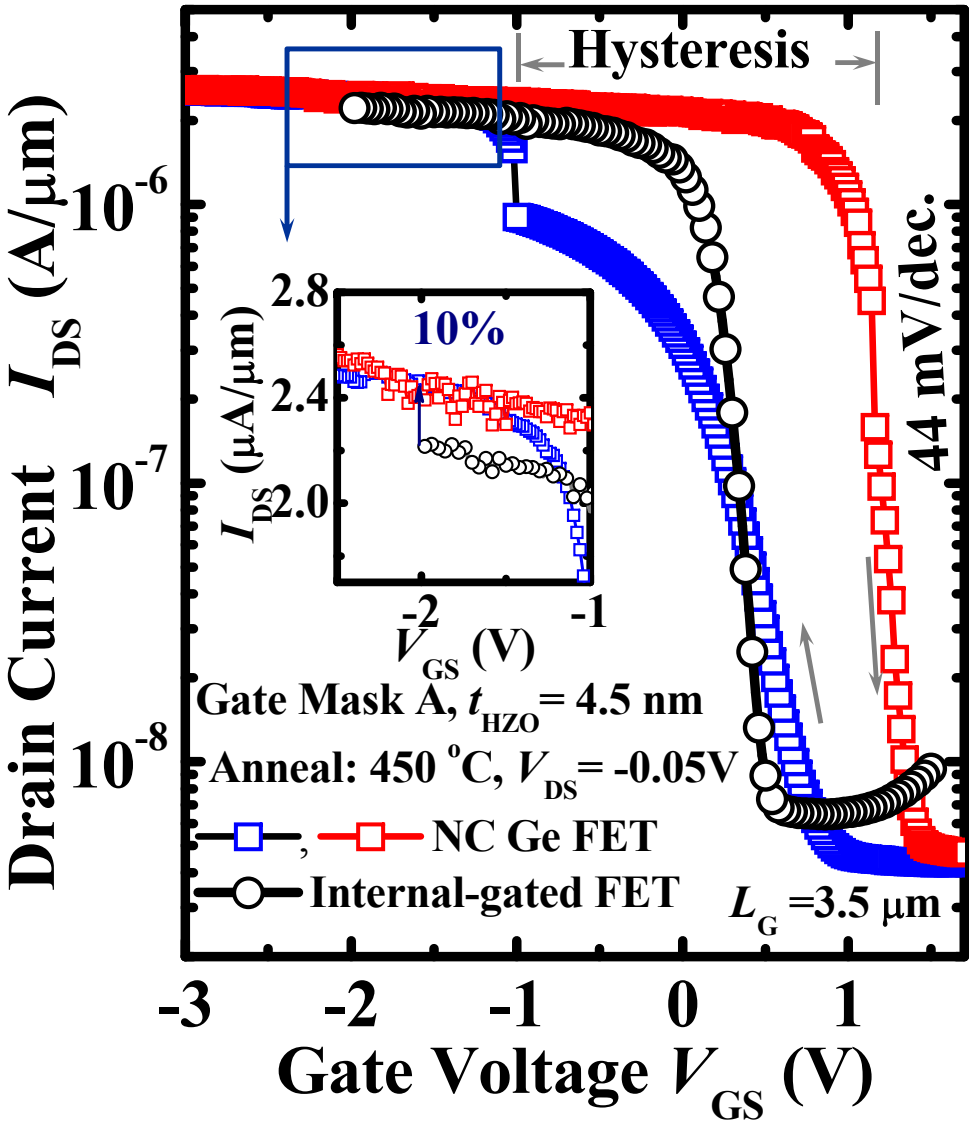


J. Zhou, G. Han, Y. Peng, Y. Liu, J. Zhang, Q.-Q. Sun, David W. Zhang, and Y. Hao, "Ferroelectric negative capacitance GeSn pFETs with sub-20 mV/decade sub-threshold swing," *IEEE Electron Device Lett.*, vol. 38, no. 8, pp. 1157 - 1160, Aug. 2017. DOI: 10.1109/LED.2017.2714178

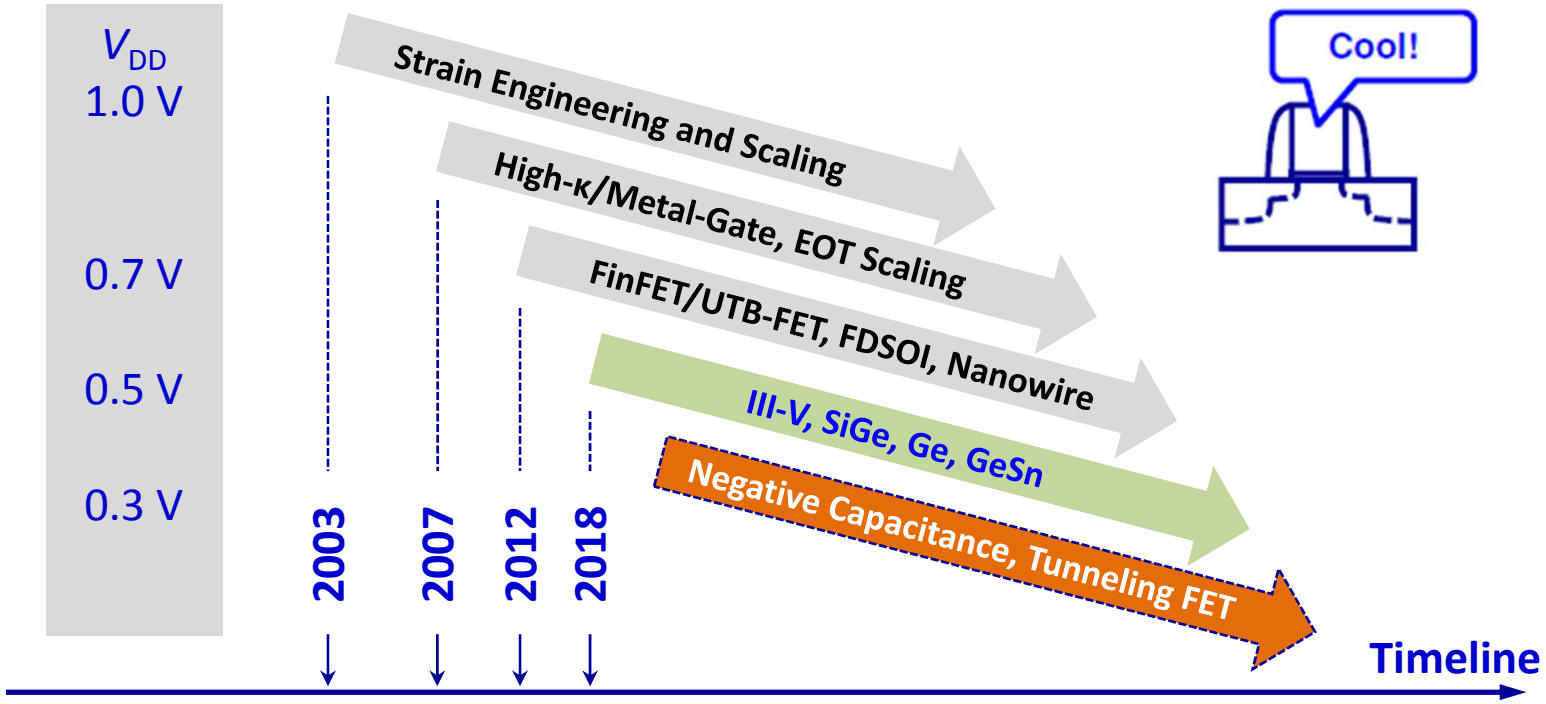
Improved I_{ON} Compared to MOSFET







Summary



- Technologies that enable V_{DD} reduction were discussed.
- To reach sub 0.7 V V_{DD} regime with Si channel, aggressive strain engineering is needed. For p-FETs, SiGe channel may be used.
- To reach sub 0.5 V V_{DD} regime, high mobility MOSFETs will be used.
- To reach 0.1~0.3 V V_{DD}, Negative Capacitance or Tunneling Transistors might be used.

致谢

- 郝跃院士、黄如院士的支持！
- 学生们：
  - 博士生：王洪娟、刘欢、刘翔宇、周久人、彭悦、张译、吴继宝、张庆芳（毕业）等
  - 硕士生：王轶博、阚杨若颖、杨景辰、刘梦、敬莹、李庆龙、李静、刘明山（毕业）等
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- 自然科学基金委（重点基金和优秀青年基金）