Tektronix

DisplayPort 1.4 Webinar

Test Challenges and Solution

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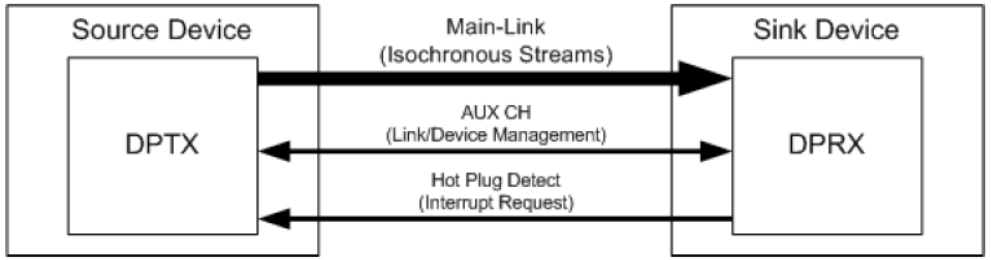
Agenda

- DisplayPort Basics
- Transmitter Testing
- Challenges
- DisplayPort Type-C Updates
- Receiver Testing
- Q and A

DisplayPort Basics

DisplayPort Standards

- Standards
  - DP 1.2 – May, 2012
  - DP over Type-C Spec – Aug, 2015
  - DP 1.4 Spec – Feb, 2016
- Hot Plug Detect (HPD) signal line
  - Initiates communication
- Main-Link
  - Uncompressed video and audio
- Auxiliary channel (AUX CH)
  - Link management and device control



Advantages

Royalty Free

MST

Type-C connectivity

8K uncompressed Video (DP 1.4)

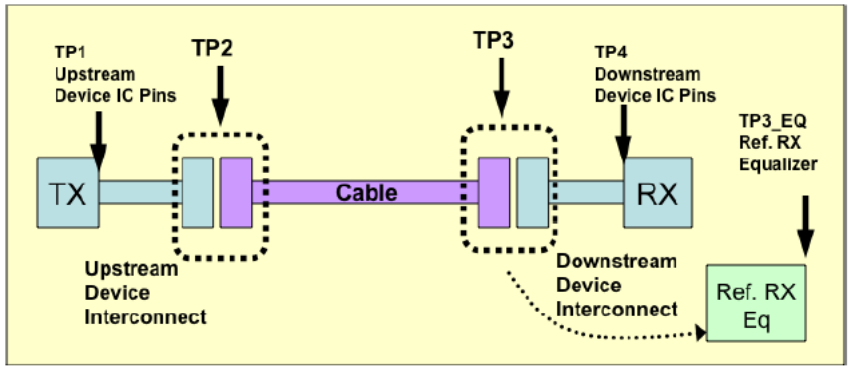
Simpler Cables

DP to HDMI, DVI, VGA adopters

Transmitter Testing

Compliance Test Points

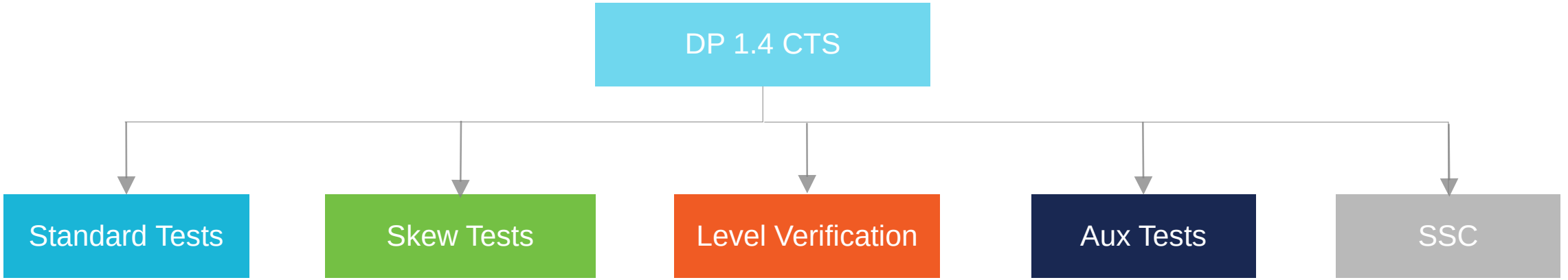
- TP1: at the pins of the transmitter device
- TP2: at the test interface on a test access fixture near end
- TP3: at the test interface on a test access fixture far end
- TP3_EQ: TP3 with equalizer applied
- TP4: at the pins of a receiving device



NORMATIVE test points

INFORMATIVE test points

TX Measurements



3.1 Eye-diagram Testing
3.10 AC Common Mode Noise
3.11 Non ISI Jitter Measurements
3.12.1 Total Jitter (TJ) and Deterministic (DJ) Measurements
3.12.2 Random Jitter (RJ) Measurements
3.14 Main Link Frequency Compliance

3.4 Inter Pair Skew Test
3.5 Intra-Pair Skew Test

3.2 Non Pre-Emphasis Level Verification Testing
3.3 Pre-Emphasis Level Verification Testing

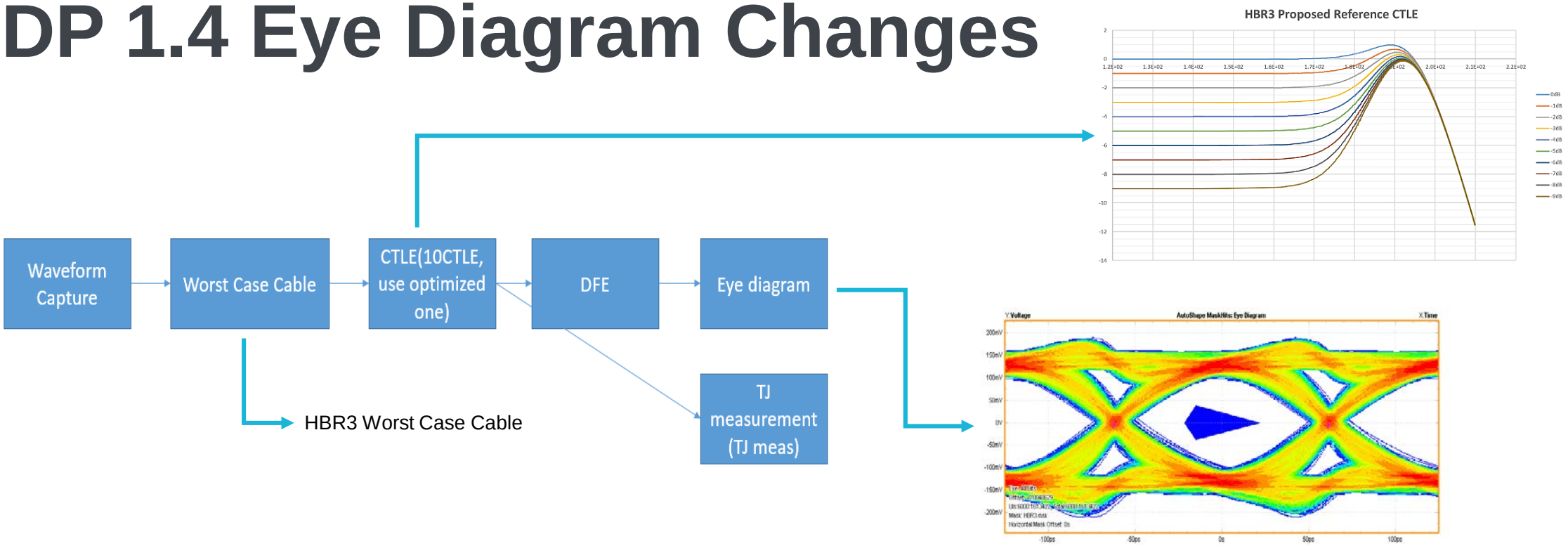
8.1 AUX Manchester Channel Eye Test
8.2 AUX Manchester Channel Sensitivity Test
8.5 AUX Inrush Test

3.15 Spread Spectrum Modulation Frequency
3.16 Spread Spectrum Modulation Deviation
3.17 dF/dt Spread Spectrum Deviation HF Variation

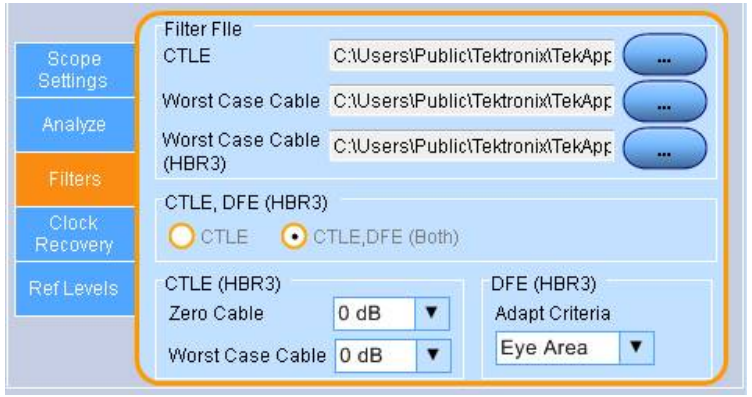
DP 1.4 vs DP 1.2 Comparison

Test ID	DP 1.2	DP 1.4
Highest Speed	5.4 Gbps (HBR2)	8.1 Gbps (HBR3)
Recommended scope bandwidth	12.5 GHz	16 GHz (min 12.5 GHz)
3.1 Eye Diagram Test		
Test Point	TP3_Eq	TP3_Eq
Pattern	Comp Eye	TPS4
CTLE	Single	Multiple, optimized CTLE + DFE setting to be used for measurement
DFE	No	Yes
Cable Model	HBR2 Cable Model (s4p) , ~17dB loss	HBR3 Cable Model (s4p), ~11dB loss
Eye Opening	90 mV	90 mV
Maximum TX Total Jitter	0.62 UI	0.5 UI

DP 1.4 Eye Diagram Changes

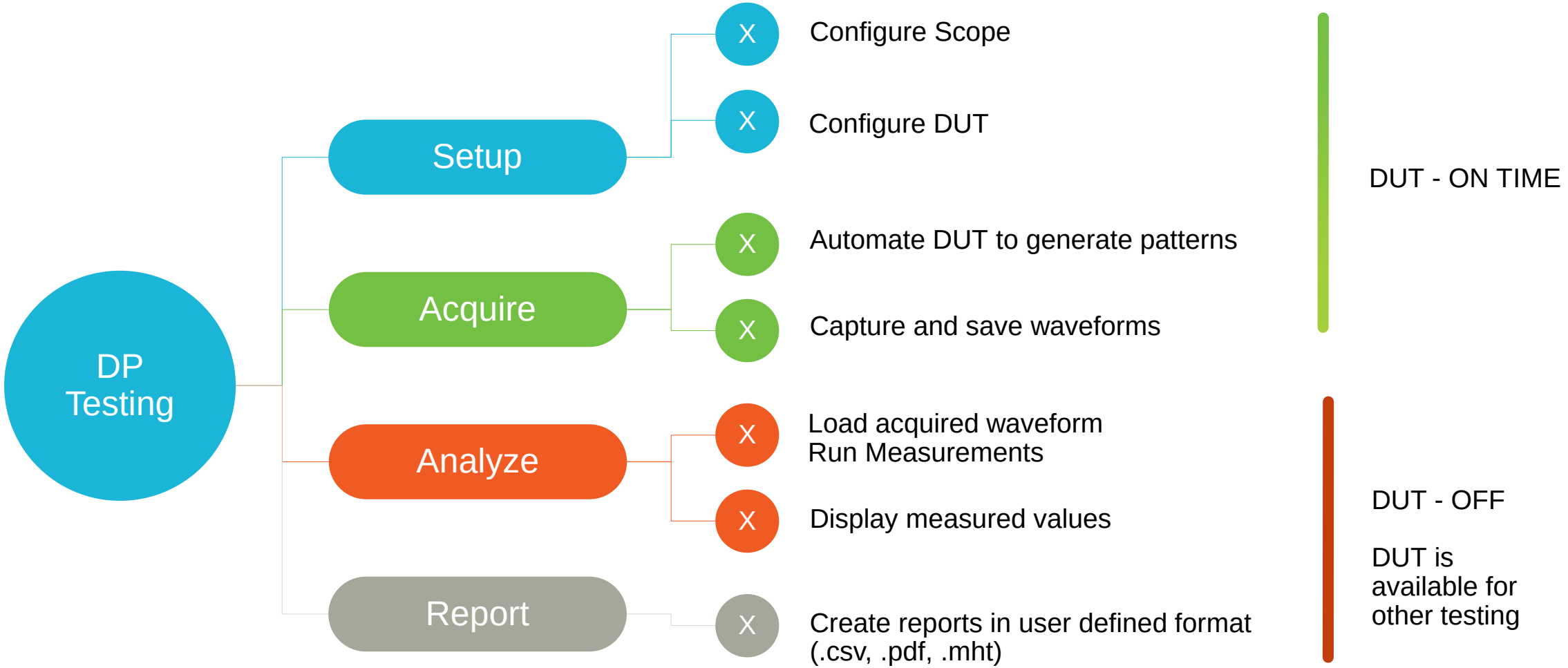


- Find the optimal CTLE and DFE, and create a waveform using this value. Use these values for performing the eye diagram measurement.
- Note down the optimal CTLE used, and create a new waveform using this CTLE. Use this waveform for performing jitter (TJ) measurement



Transmitter Test Challenges

TX Testing Workflow



Importance of Characterization

- DUT Fails Compliance Tests – What next?
- Root Cause Analysis?
- How easy is it to change the configuration?
- True vs False Failures?
- How do you ensure repeatability of measurements?
- Running only failed tests again

Why Save Waveforms?

These sites capture/analyze DP waveforms

These sites can also analyze DP waveforms acquired elsewhere

TYPICAL USE CASE

Design and Test teams are located in different regions

Customers want Tektronix to look into root cause

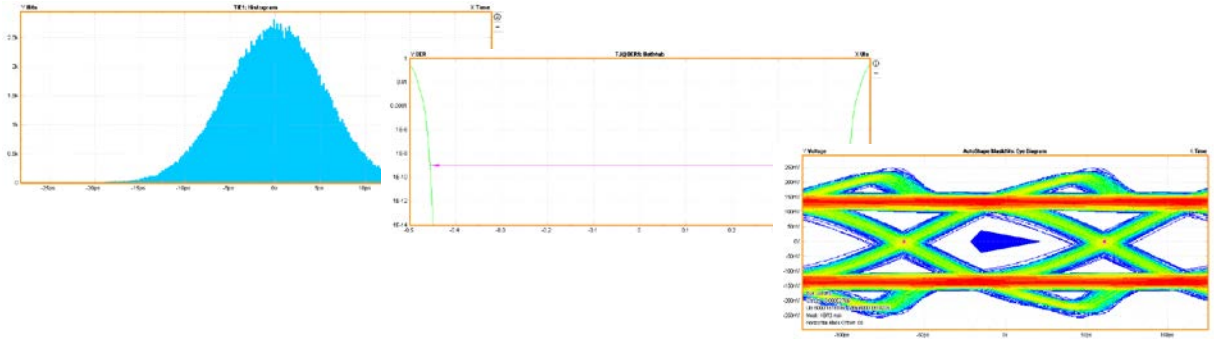
Comparison of previous data with latest one

How to Debug Compliance Failures?

- DPOJET - Industry best general purpose signal analysis tool
- Includes the standard specific modules
- Support for up to 99 measurement analysis on single acquisition
- Comprehensive Measurements for
  - Jitter Analysis
  - Noise Analysis
  - Eye Analysis
  - Amplitude Analysis
  - Timing Analysis
  - Period / Frequency

DPOJET DP 1.4 PLUGIN

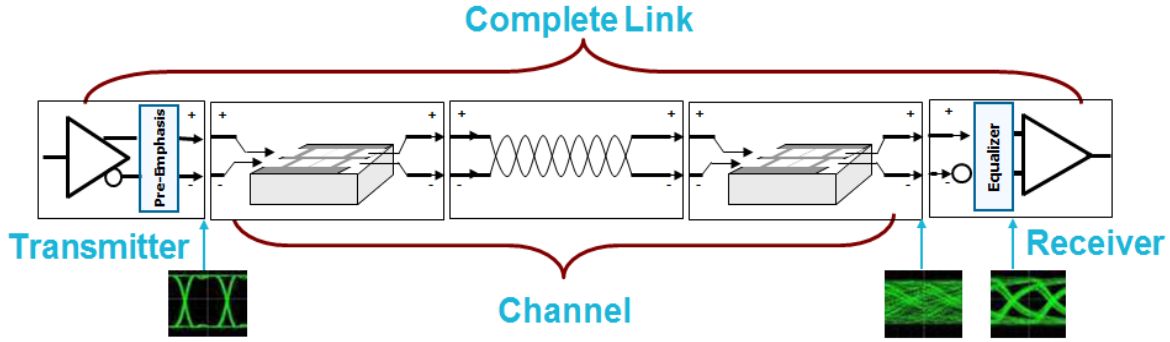
- Quickly analyze measurements before performing automated testing
- Vary measurement parameters and monitor behavior
- Add different plots to get deep insight into DUT characteristics
- Generate DPOJET reports for reference



Importance of Channel Analysis

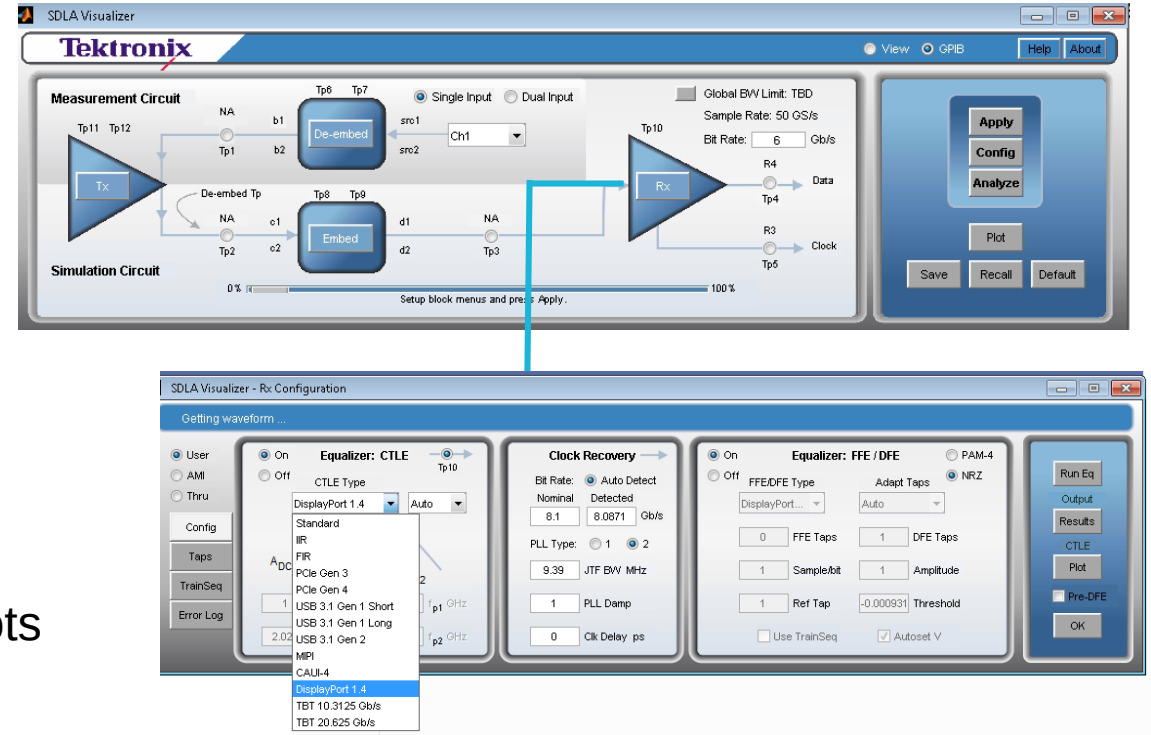
PROBLEMS WITH CHANNEL BEHAVIOR

- Inability to probe at required location in signal path
- Reflections, cross-coupling, fixture losses, cables, and probe effects
- Closed eye analysis
- Understand the effect of changing a components
- Compliance standards mandate eye analysis at various test points



SDLA FEATURES

- Enables virtual probing through test points
- Remove the effects of the cables, probes and fixtures
- Open a closed eye
- Output results to Math/Ref channels
- Analyze up to 8 cascaded blocks at once
- Model each block through different techniques
- Move and visualize each test point in the block using plots



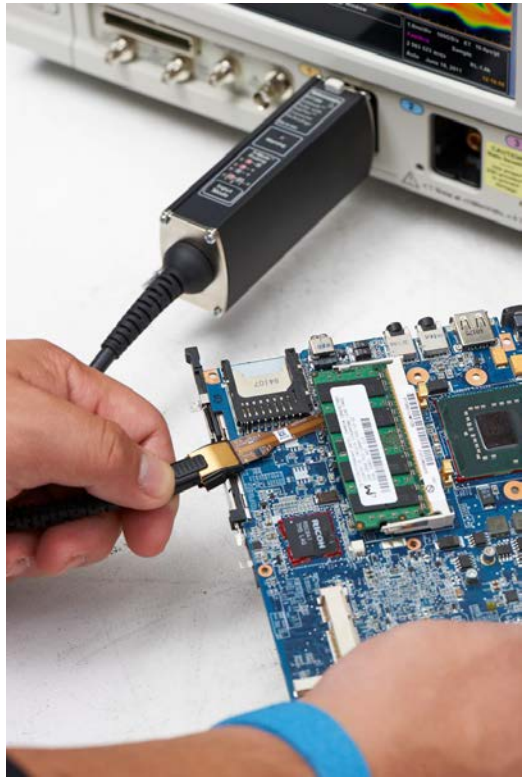
Accessing Test Points

CHALLENGES

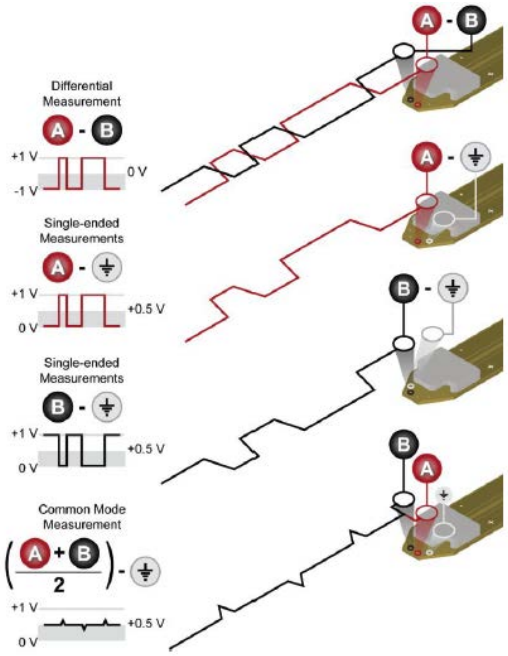
- Differential and Single-ended tests require connection changes
- Early eval boards require probing on PCB and Production DUTs require probing using DP Fixtures
- De-embed the probe effects for accurate measurements

P7720 PROBES

- TriMode™ input enables single-ended or differential measurements with single connection
- Probe can be quickly changed from high impedance to 50Ω
- S-parameters in adapter for automatic de-embedding of the probe effects
- Bandwidth up to 20GHz - Supports HDMI v2.1, DisplayPort v1.4, MIPI M-PHY standards

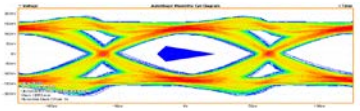


P7720 probe with browser tips



TriMode™ input enables single-ended or differential measurements with 1 connection

Putting It All Together



Browser tip of P7720 probe

Use DPOJET plugins to quickly measure DP tests

DisplayPort Sample Circuit

Processor

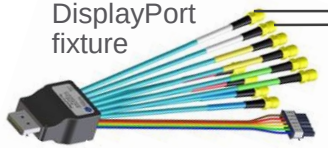
Switch

Dock

Re-Timer

DP Connector

DisplayPort fixture



SMA adapter

TekExpress DP application to perform compliance measurements

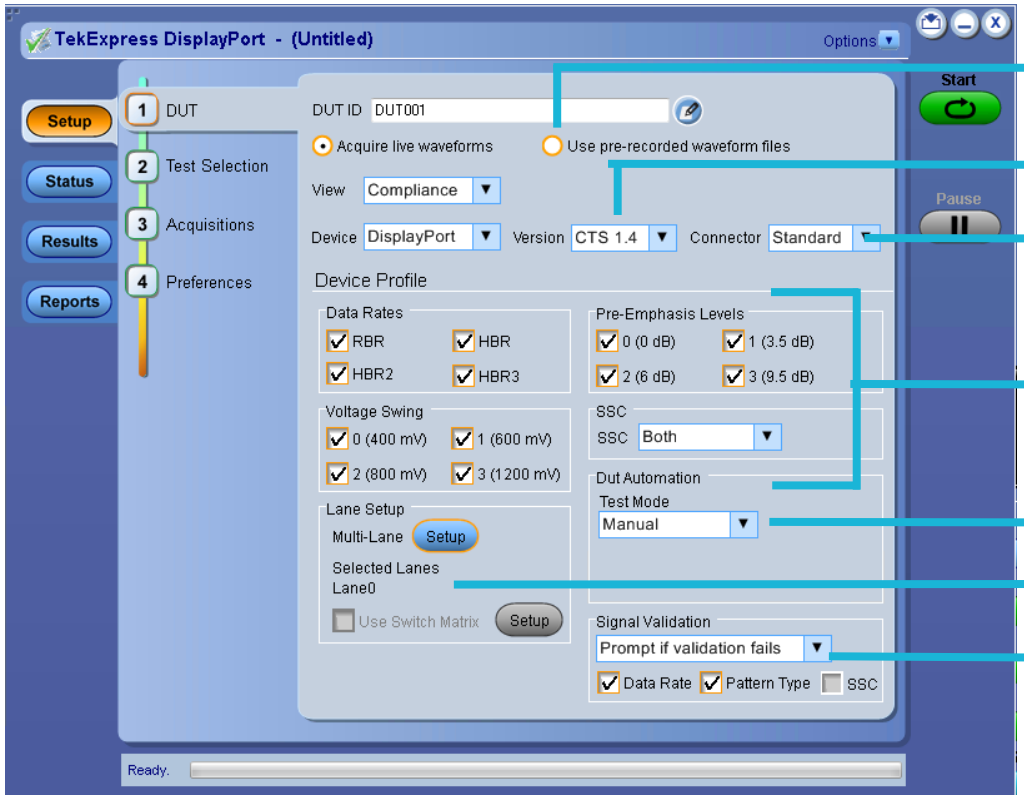
Solder-in tip of P7720 probe

Use SDLA to de-embed each test point along the signal trace

P7720 probe

Automating DisplayPort 1.4 TX Tests

TEKEXPRESS DP1.4 UPDATES



Execution mode : Live or pre-recorded

CTS versions : DP1.4, DP 1.2

Connector Type – Standard or Type-C

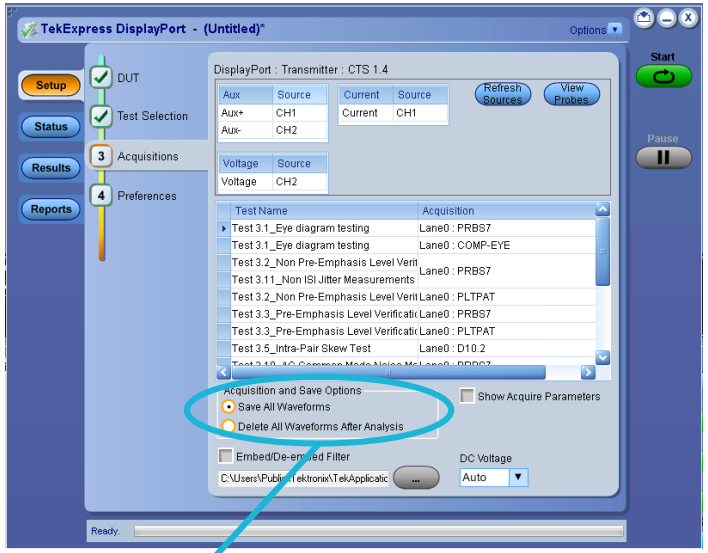
DUT Settings

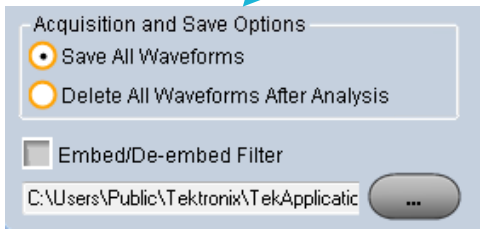
DUT Automation – Manual or DPR-100

Lane selection or switch matrix

Optional Signal Validation

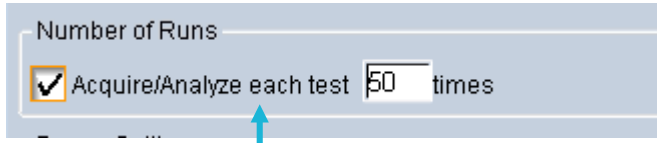
New Features and Benefits

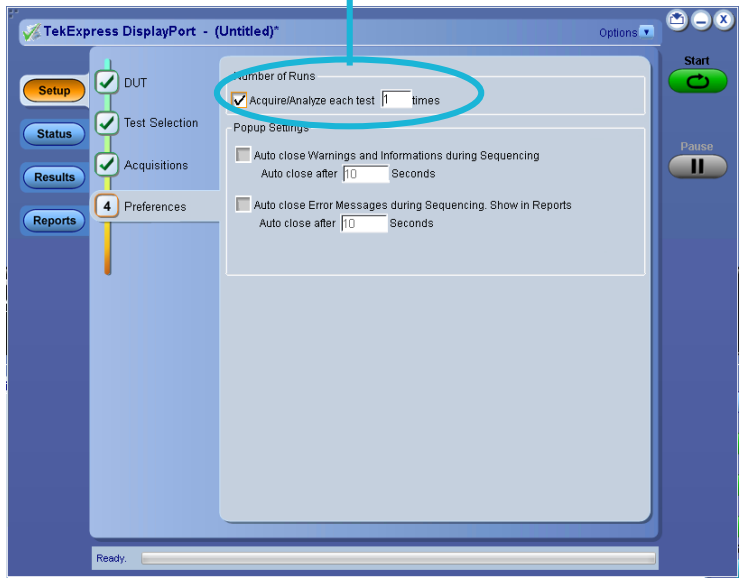




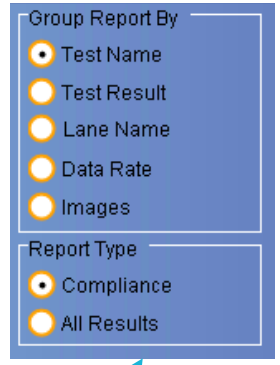
Optionally delete waveforms after execution

Perform Repeatability testing to monitor consistency of DUT behavior

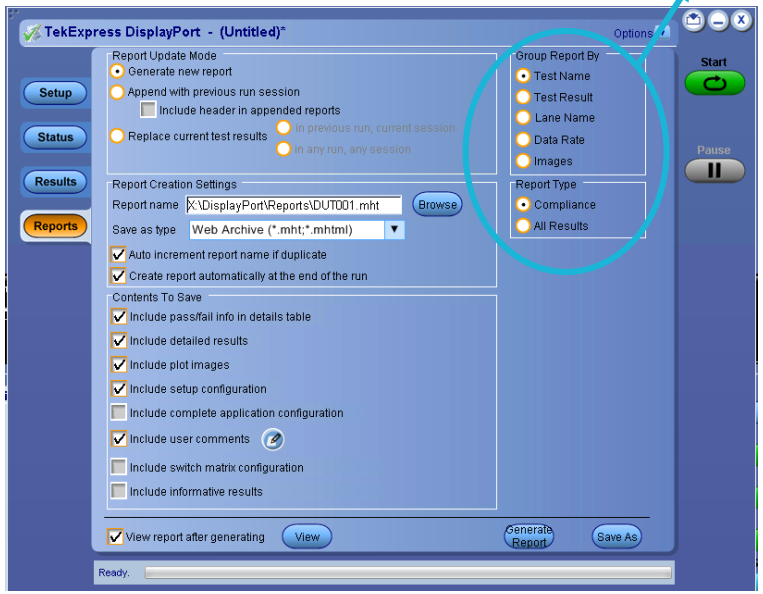




Generate and group reports by different categories

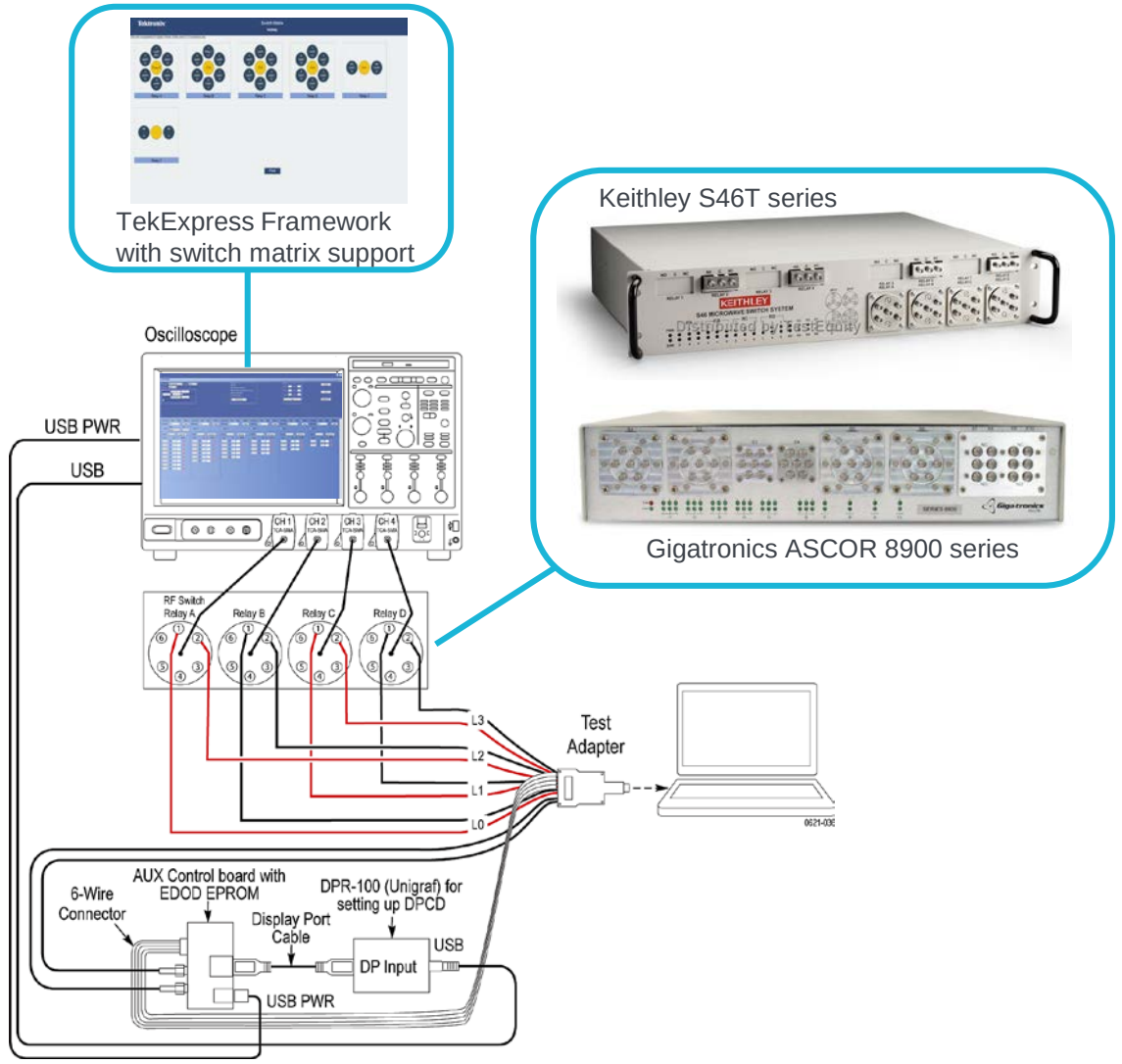


Compliance Report Generation as per CTS requirement and detailed report as per current execution



Avoiding Manual Intervention During Testing

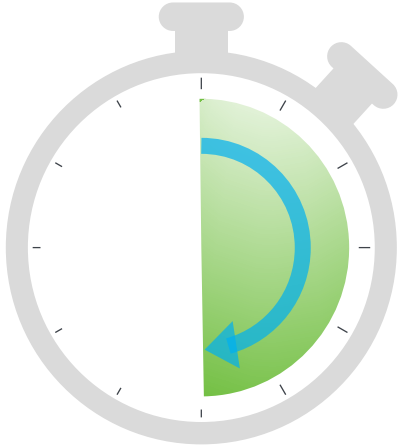
- Framework support for RF switch
- Auto Detects the Keithley and Gigatronics switch on the GPIB/LAN interface
- De-embed using filter files – with multiple de-embed options (per relay, per input, etc.)
- Operates with TekExpress and DPOJET (Debug Mode)
- Save/recall switch configurations
- Graphical view with print option to support hardware wiring
- Graphical view integration with TekExpress report
- Built-in error handling to support easy and error-free configuration
- Support for custom input labels such as Lane, Port, etc. via XML file edits.
- Programmatic interface to support scripting and easy integration into user's automation environment.



Why Test Times Matter?

Parameters	Combinations
Bit Rates	RBR, HBR, HBR2, HBR3
Patterns	D10.2, PRBS7, COMPEYE, PLTPAT
Pre-Emphasis	0dB, 3.5dB, 6dB,9.5dB
Levels	400mV, 600mV, 800mV, 1200mV
Lane Width	1,2,4
SSC	On (If DUT supports)

Real world benchmarking
*HBR2 Test times > **11 hours***



Tektronix Results
*HBR2 Test times **~ 6 hours***

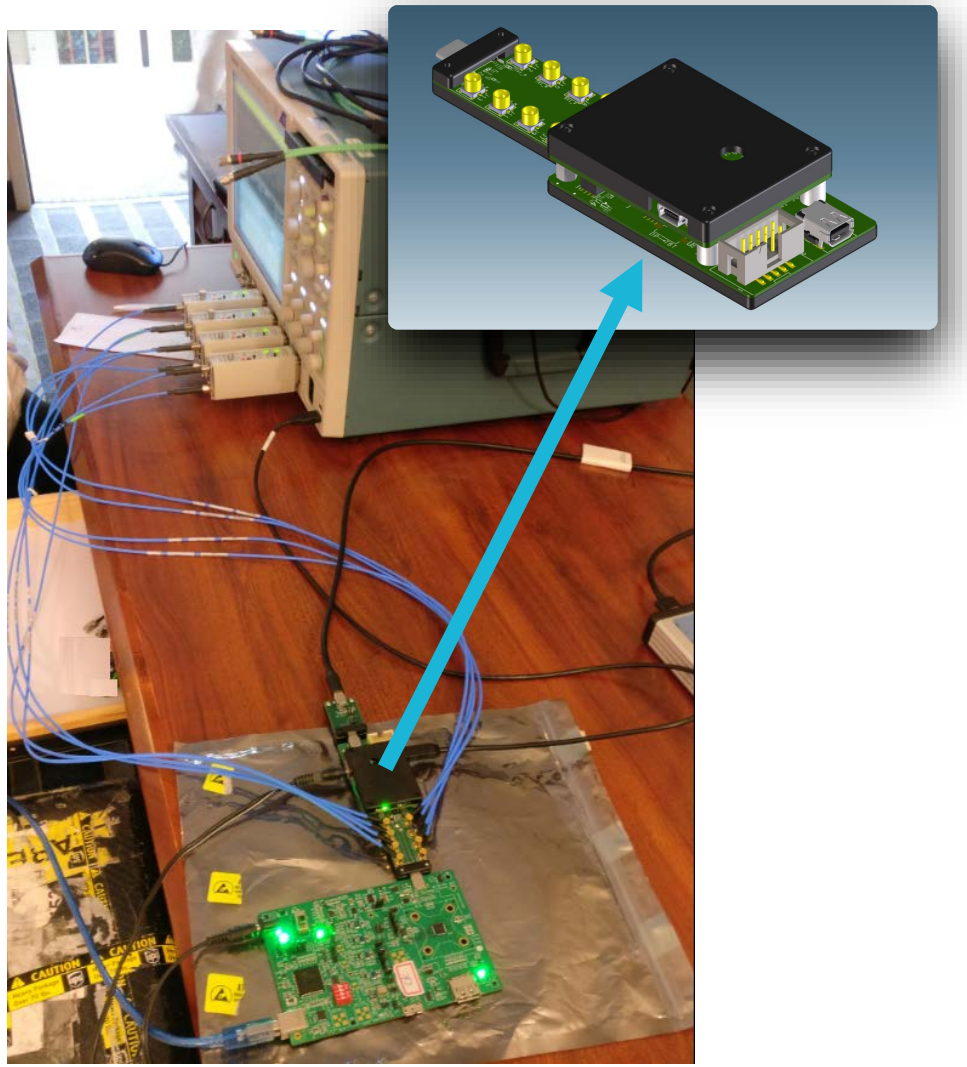
Test	Waveforms
Eye Diagram	88
Pre-Emphasis	320
Non-Pre-Emphasis	32
Total Jitter	112

~126 acquired signals for DP1.4 Normative Measurements per lane.
X4 lanes results in **504** automated acquisitions per DUT

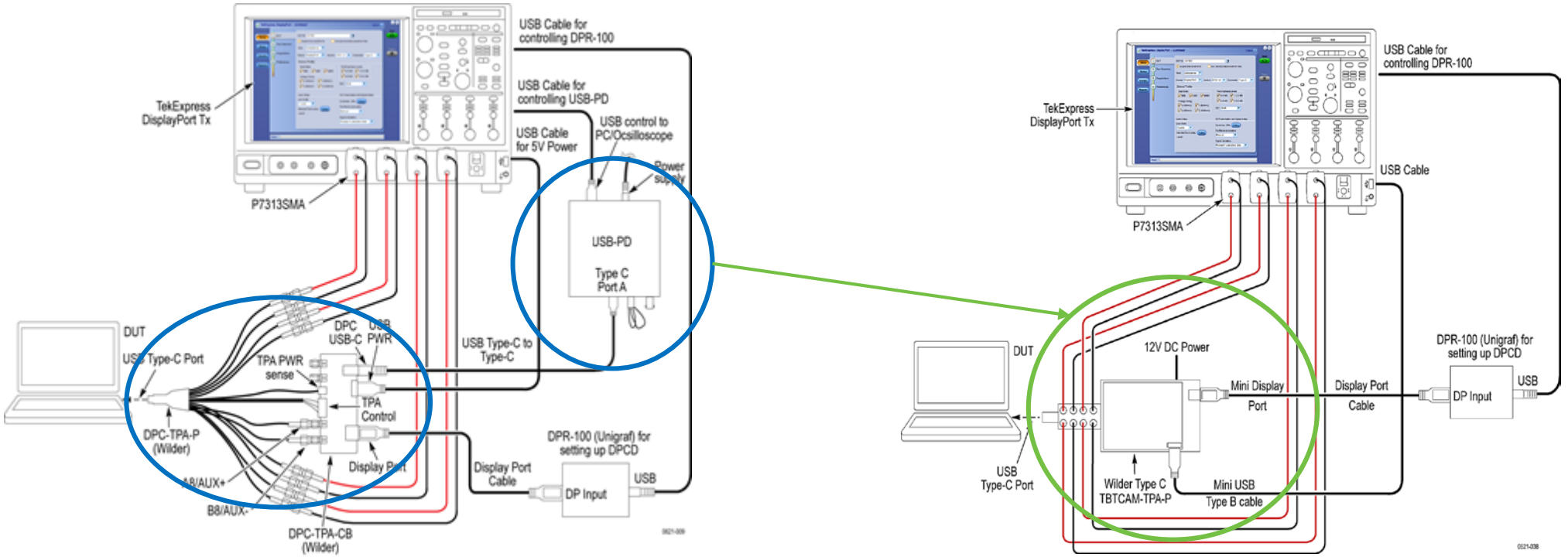
DisplayPort Type-C Updates

Introducing Single Fixtures for Type-C Testing

- Tektronix Exclusive TBTCAM Fixture
- Single fixture for TBT, USB and DP testing
  - Supports TBT4, USB Gen 1 & Gen 2 and DP 1.4
- Integrates Alt-mode capability for DP/TBT
- Supports high speed and aux measurements for DisplayPort
- Performance correlated with USB-IF fixture
- Simulates software flip for USB testing



Simplified DP Type-C TX Test Setup

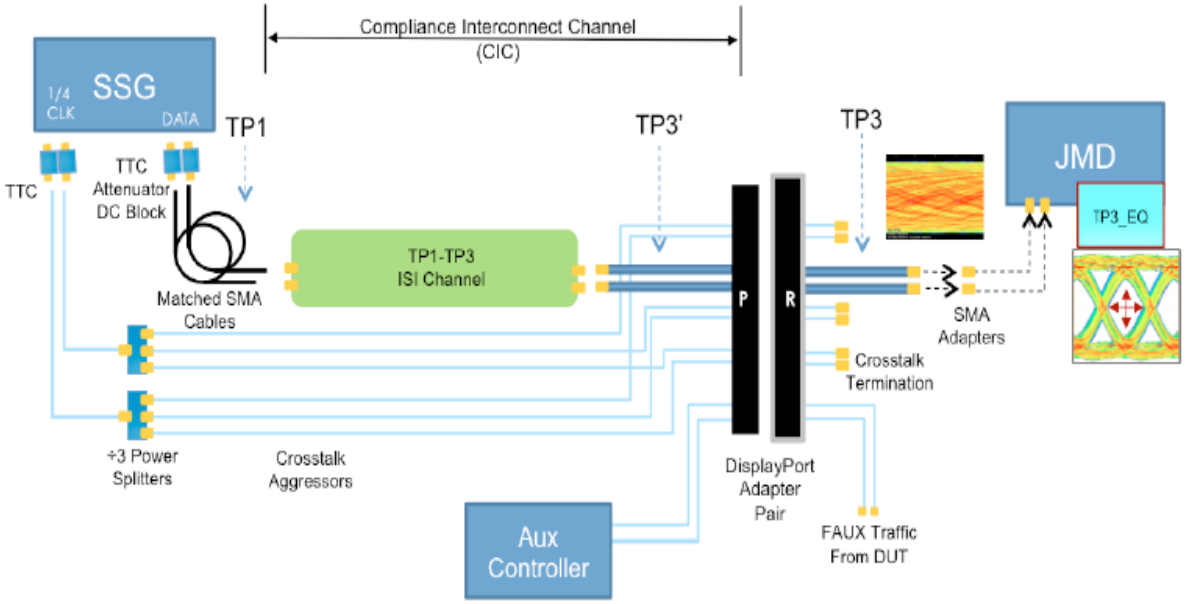


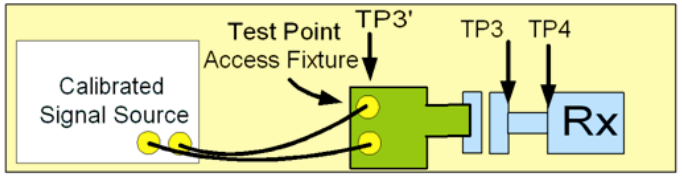
Integration of TBTCAM fixture simplifies test setup

Eliminates the need for additional controllers

Receiver Testing

Receiver Test Overview





Calibration

- ✓ Frequency Range (SJ): 2MHz, 10MHz, 20MHz, 100MHz
- ✓ Injected Jitter: ISI, RJ and SJ

Link Training

- ✓ Frequency Lock
- ✓ Symbol Lock

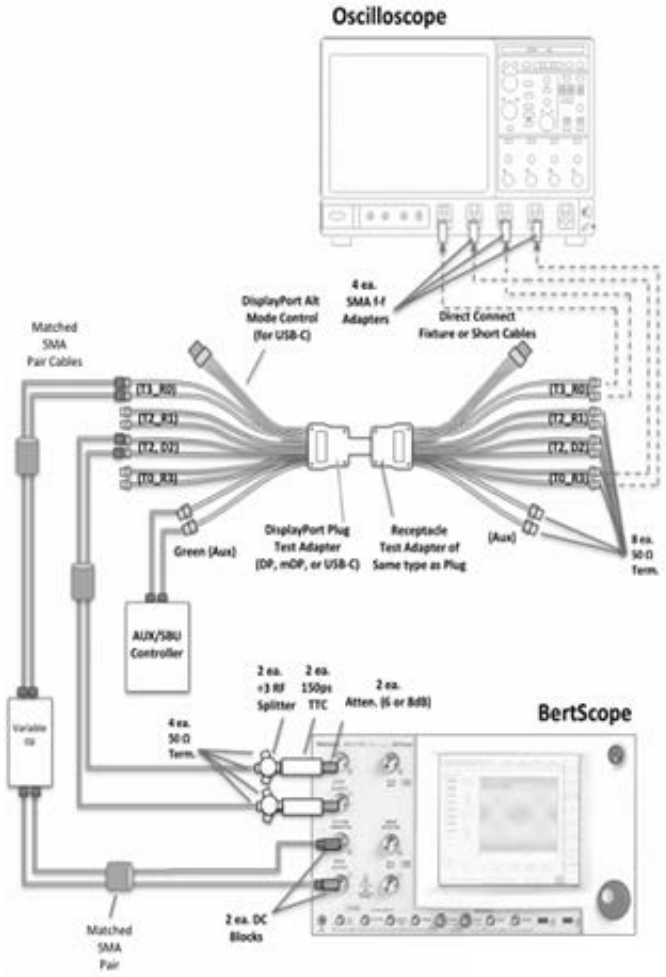
RX Compliance

- ✓ Jitter Tolerance Test

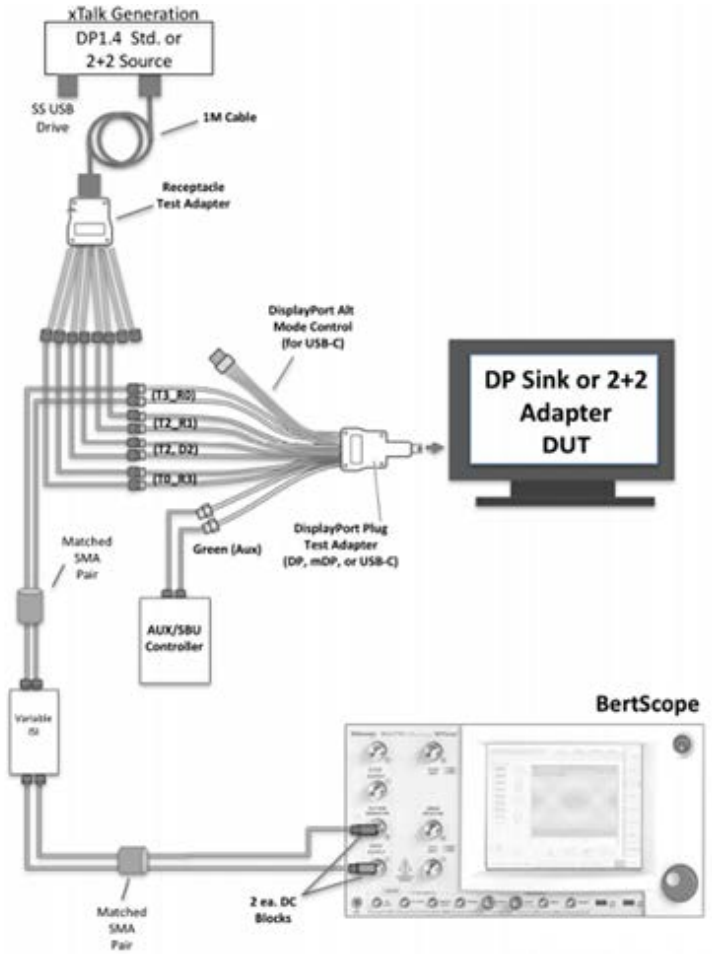
Table 4-1: Test Parameters for BER Measurement

Data Rate	Jitter Frequency	Number of Bits	Max Number of Bit Errors Allowable	Observation Time[1] (seconds)	Data Rate Offset
HBR2 *HBR* *RBR*	*2MHz*	10^{12}	*1000*	*HBR2 = 185s* *HBR= 370s* *RBR= 620s*	*0*
HBR2 *HBR* *RBR*	*10MHz*	10^{11}	*100*	*HBR2= 19s* *HBR= 37s* *RBR= 62s*	*+350ppm* *+350ppm* *+350ppm*
HBR2 *HBR* *RBR*	*20MHz*	10^{11}	*100*	*HBR2= 19s* *HBR= 37s* *RBR= 62s*	*0*
HBR2 *HBR*	*100MHz*	10^{11}	*100*	*HBR2= 19s* *HBR= 37s*	*0*
*To evaluate multiply number of bits by the unit interval in ps. (i.e. for HBR: 10^{11} bits at HBR = 370ps/UI * 10^{11} UI = 37 seconds*					

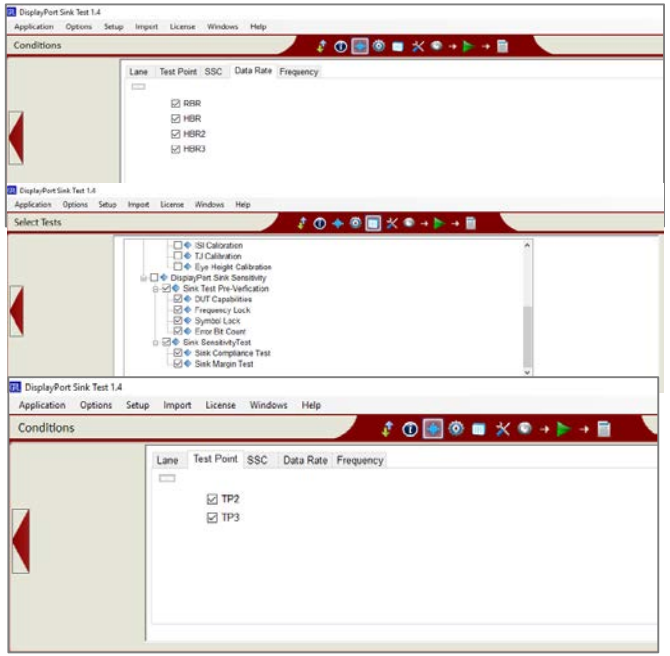
Receiver Test Procedure



Step-1 : Calibration



Step-2 : RX Compliance Testing



Option : GRL-DP14-SINK

DP 1.4 vs DP 1.2 Comparison

Parameters	DP 1.2 (HBR2)	DP 1.4 (HBR3)
Max. Data Rate Calibration	HBR2	HBR3
Calibration Test Points	TP2/TP3	TP1 and TP2/TP3
Eye Height Calibration	CTLE only	CTLE + DFE
Unit Interval	185 ps	123 ps
RX Differential Peak-to-Peak EYE Voltage	70 mV	75 mV
Minimum Receiver EYE Width	0.38 UI	0.35 UI
Eye pattern	Measured at 1E-9 using Comp Eye pattern	Measured at 1E-9 using TPS4 pattern
DC Common Mode Voltage Source	No	Yes
ISI	220 mUI	240 mUI
Random Jitter (RMS)	16.7 mUI	13 mUI
Jitter Closed-Loop Tracking Bandwidth	10 MHz	15 MHz
SJ (Fixed) @ 200 MHz	100 mUI	150 mUI

Simplify and Accelerate RX Testing

INTRODUCING BSX SERIES

- Provides error location analysis
- Error locations → Error Patterns → Unique debugging information
- Gen4 Datacenter Standards are driving Changes in Receiver Testing Needs
- BERTs used in Gen 4 receiver testing must participate in handshaking to ensure proper test configuration
- Up to 32 Gb/s in the case of the BSX320 version
- No external mux/demux required
- Time-correlated and flexible eye diagram
- Automation solutions to provide test configuration and calibration support for a broad range of standards – PCIe, USB, TBT and DisplayPort
- Performs handshaking with DUTs to support equalization link training to optimize the TX equalization prior to performing tests
- Configuration Wizard simplifies instrument set-up
- Automation of both scope and BERT to provide quick and accurate calibrations

BSX-series BERTScope Gen3/4 BASE

BSX125, 12.5 Gb/s maximum data rate
BSX240, 24 Gb/s maximum data rate
BSX320, 32 Gb/s maximum data rate

www.Tektronix.com/BSX

DisplayPort Test Solutions

Electrical

DP 1.2/1.4 Type-C TX

Integrated Switch Matrix

TBTCAM Type-C fixture

Tx

DP 1.2/1.4/Type-C RX

Rx

DisplayPort

DisplayPort 1.4 (8.1 Gbps)

DisplayPort Type-C

Protocol

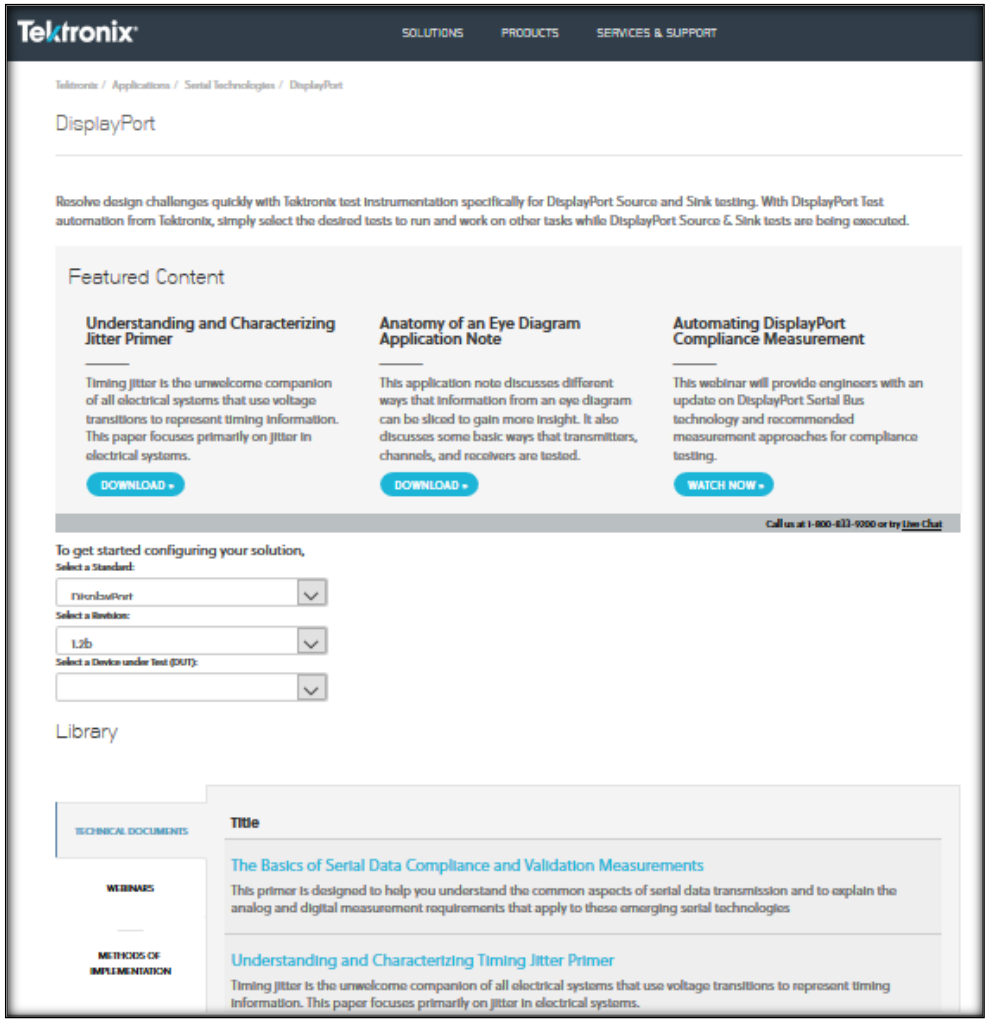
DP 1.2 Scope based protocol decode

Specification Roadmap

Tektronix Roadmap

Information & Resources for DisplayPort

- http://www.tek.com/displayport-0
- Application Notes
- Methods of Implementation
- Serial Configurator
- Webinar



Thank you for attending the presentation!