Reliability Challenges in Advanced Technology Node

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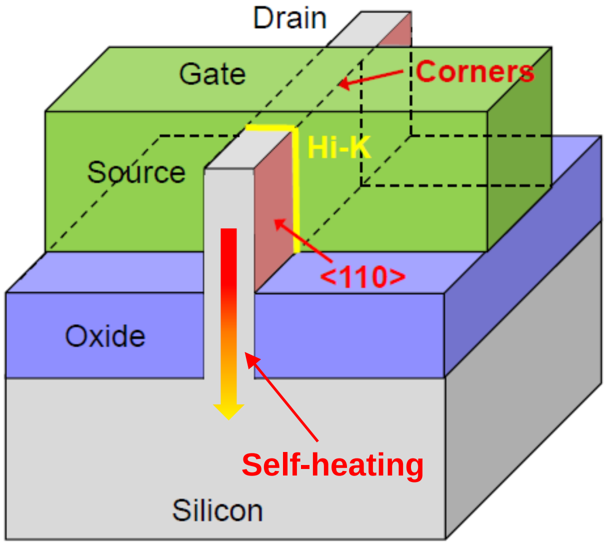
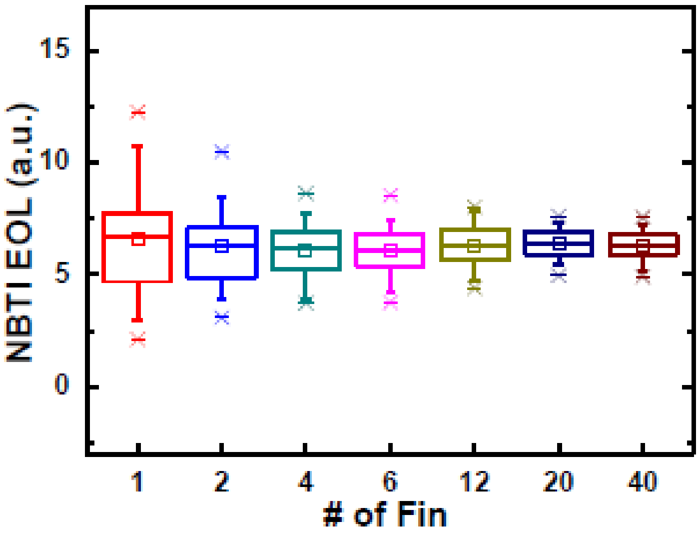
Reliability in Advanced FinFET

- FinFETs with HK/MG was introduced in Intel 22nm, Samsung 14nm, TSMC 16nm and scaling to 7nm
- 3D FinFET brings some new Q&R challenges, especially self-heating effects.
- Reliability variation is another concern in nano-scale device.



S. Ramey - Intel, *IRPS Tutorial* 2014



C.Liu- Samsung, *IRPS* 2015

Outline

- Self-Heating Effects
- Reliability Variations
- Product Reliability Qualification
- Conclusion

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- **Self-Heating Effects**
- Reliability Variations
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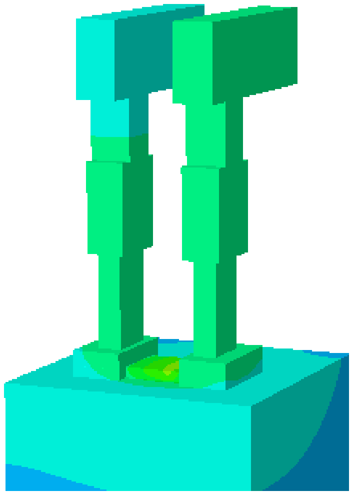
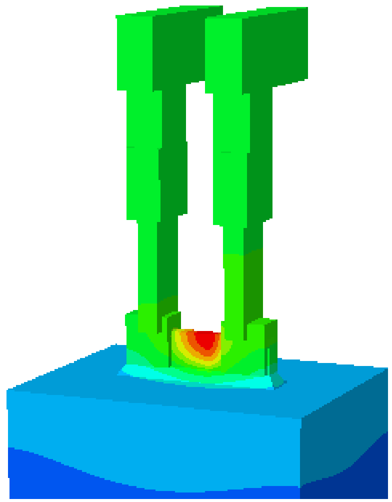
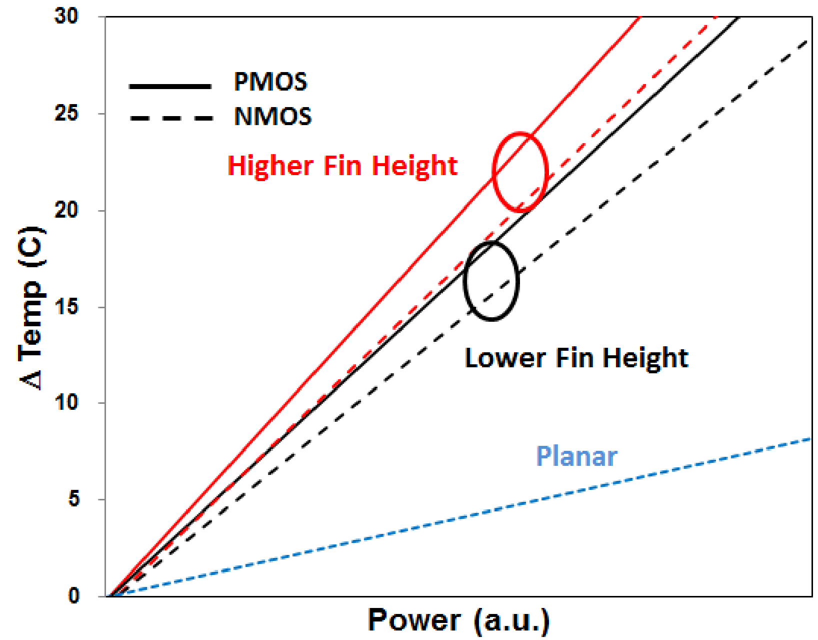
Fin Device Self-Heating



[Planar FET]



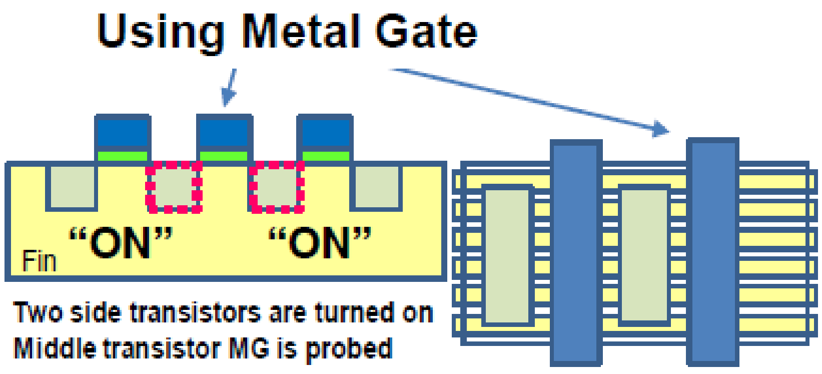
[FinFET]



- FinFET has worse heat dissipation than planar
- >3X more heat than Planar transistor
- Taller Fin shows more Self-heat effect

Characterization Method

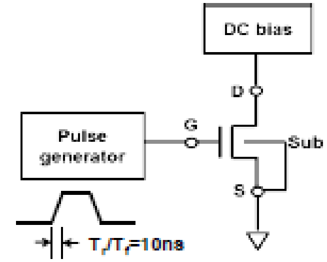
(a) Using special test structures

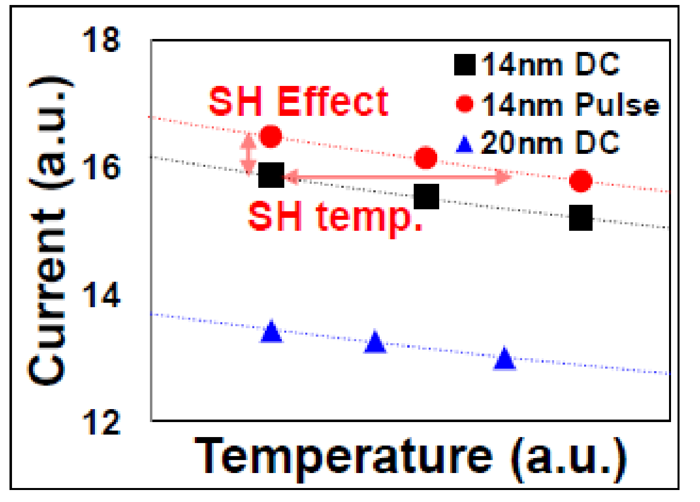


		Comments
Metal resistor	Ref [1]	Indirect
Junction Diodes	Ref [1]	More direct
Metal Gate	Ref [2]	Indirect
Pulse IV	This study	More direct

[1] 2013 IRPS, Prasad et al.
[2] 2015 IRPS, Liu et al.

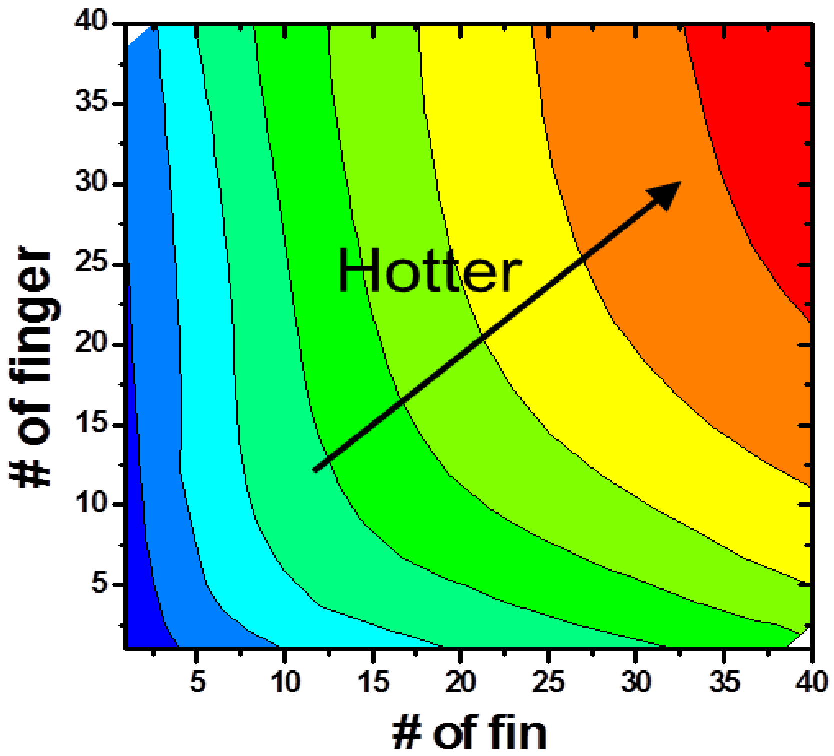
(b) Pulse IV on RF structures

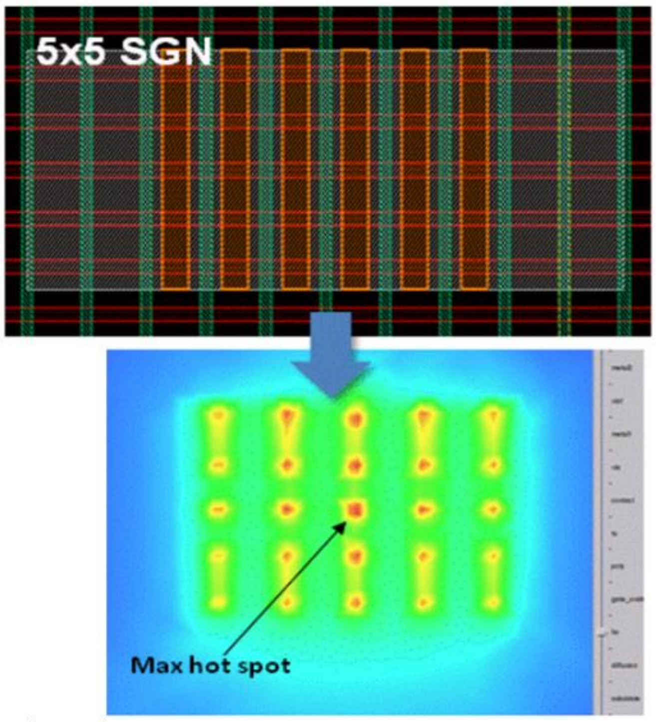




- Quick and direct way
- Thermal time constant

Geometry Dependence

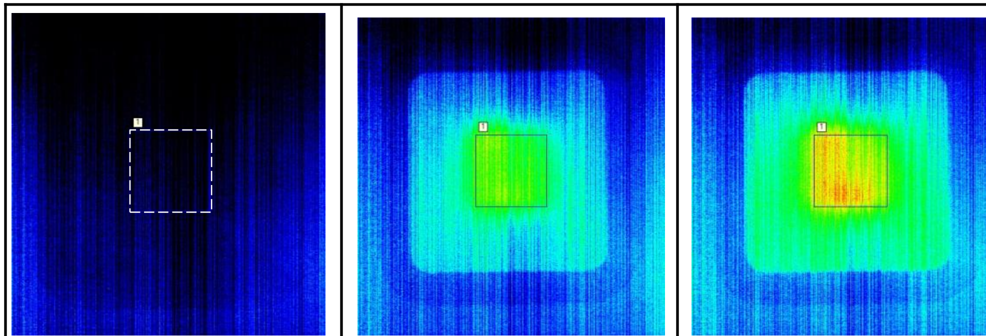




- **2D contour map for Self-heat can be characterized, modeled for design**
- **ΔT(SH) rise is more sensitive to #Fin of change than the #of Finger change**

Design Simulations

IP blocks	SH Tool Temp. extraction	HTOL
PLL	$3^{o}C$	Passed (500hr)
ADC	$2^{o}C$	
Temp Sensor	$<1^{o}C$	
Regulator	$4^{o}C$	
HDMI	$3^{o}C$	

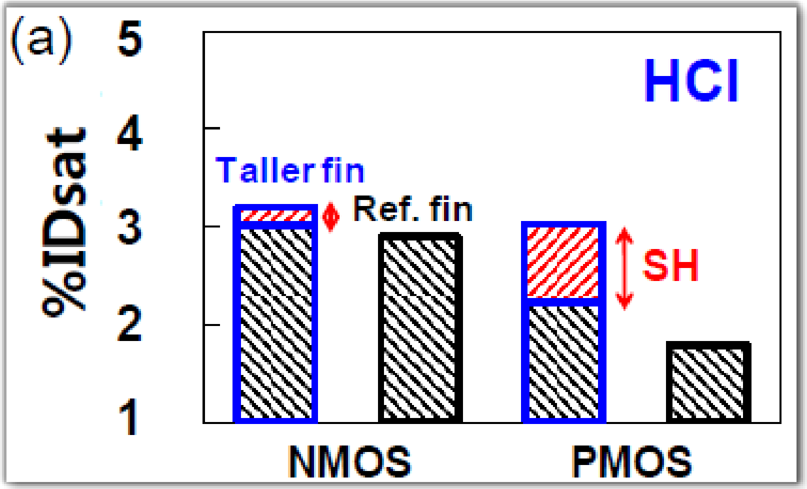


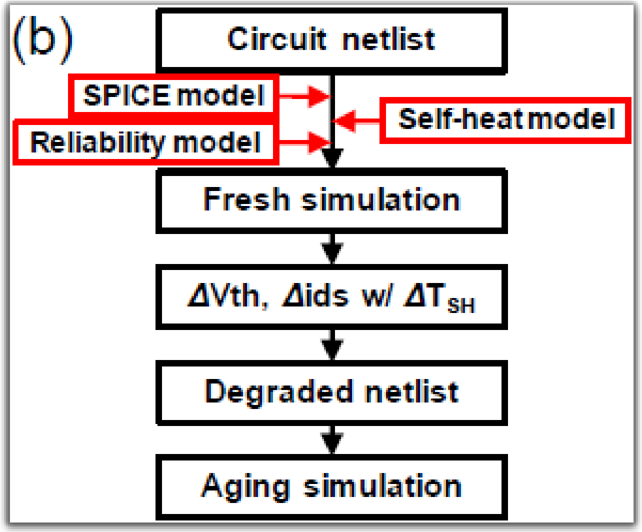
Power off	Vdd (nom)	Vdd x 1.4

(* = 24C, =26C, =28C)

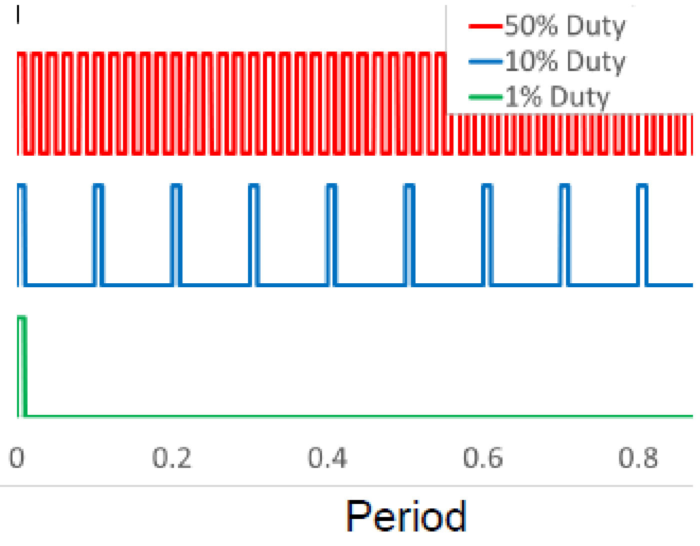
- **Self-Heat modeling is incorporated into thermal simulation flow, shows <5C for SH for most blocks**
- **Thermal imaging of an IP block showing temp increase with Vdd was within 4C suggesting any ΔT(SH) was minimal**
- **HTOL and simulation (including corners) were done at higher temperature to check and cover for any SH induced effects**

HCI vs. SHE



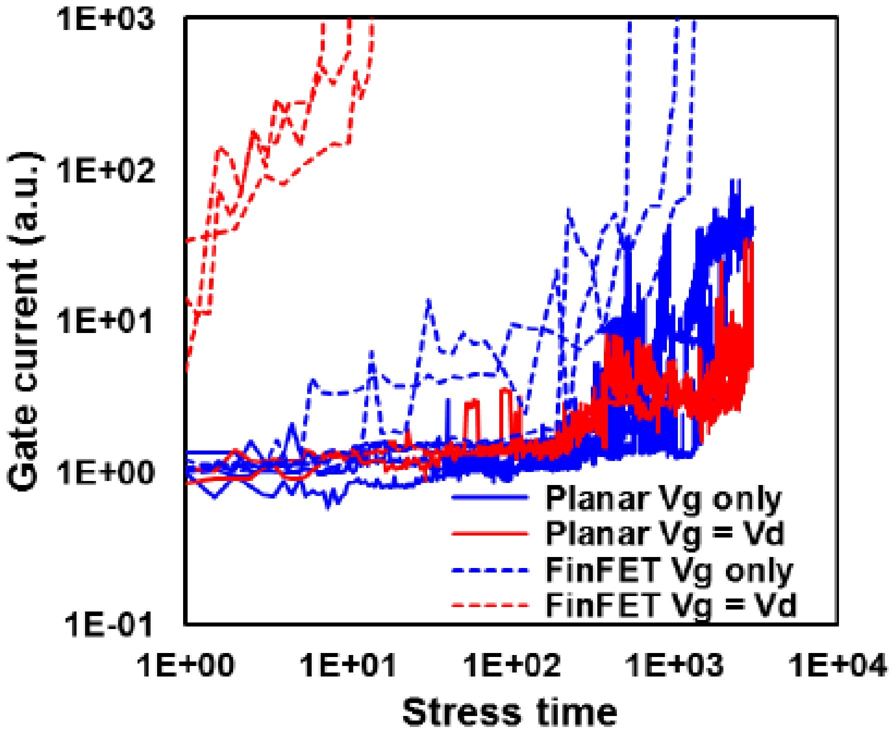


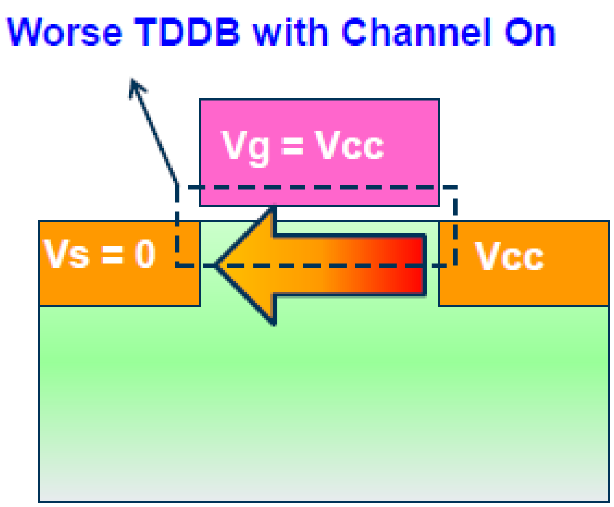
- Effect of self-heating does not cause large HCI in NFET
- PFET shows large reduction hence decoupling needed
- After decoupling SHE with pulse HCI method, HCI aging becomes comparable



On State TDDB vs. SHE

- Planar: TDDB Channel On ~ TDDB Vg only
- FinFET: TDDB Channel On << TDDB Vg only



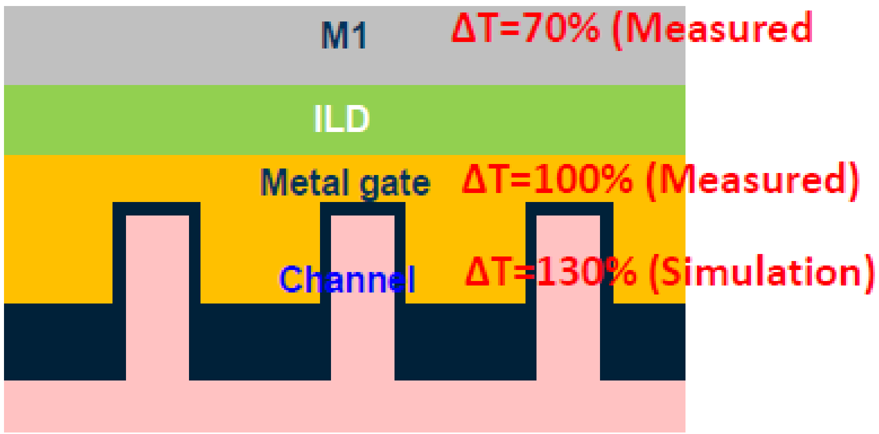


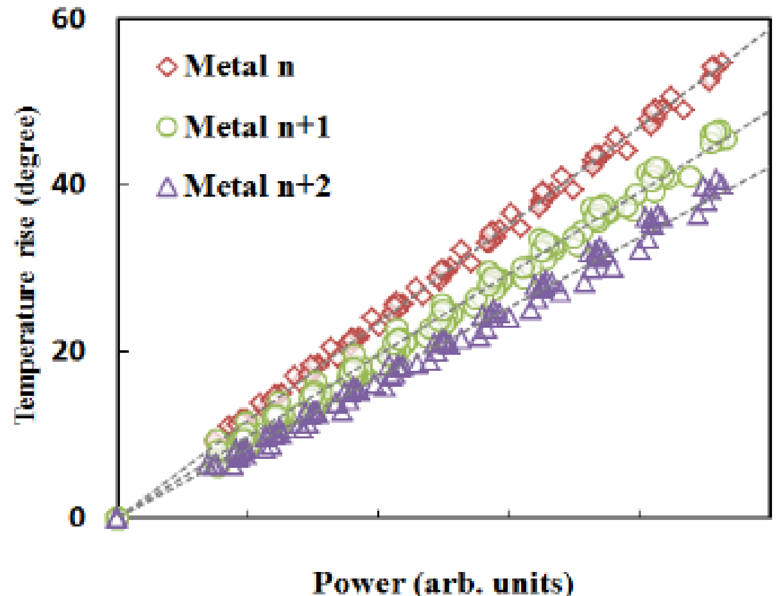
Higher temperature due to self-heating effect

TSMC FinFET, IRPS '14

Metal EM vs. SHE

- Temperature rise on M1 is ~30% lower than that of the metal gate and ~50% lower than the channel





- Self-heating temperature rise on metals requires different EM Jmax at the overall given temperature
  - DR can specify suitable rating factors for different temperatures to define the allowed Jmax at the local hot spots

Jmax @Temp = Rating Factor *Jspec

TSMC FinFET

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- **Reliability Variations**
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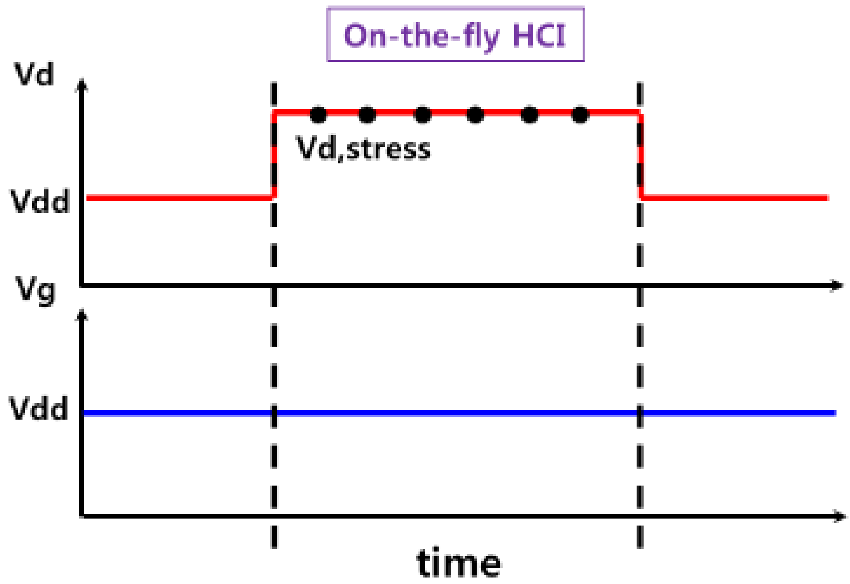
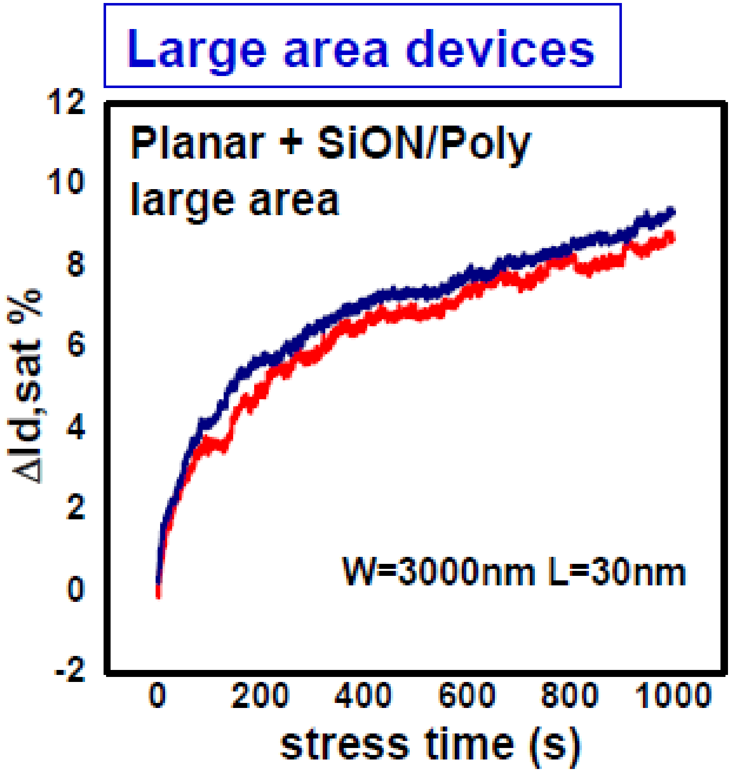
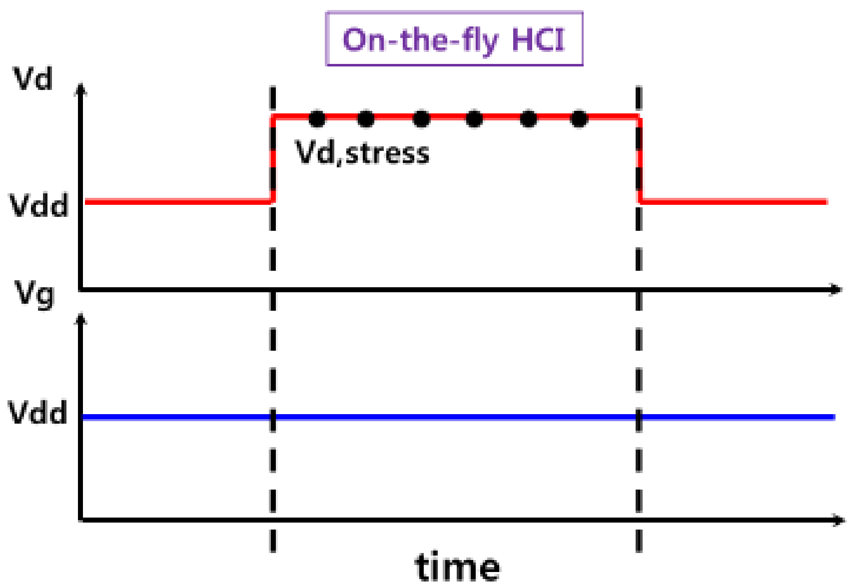
Nano-Reliability



V_{dd}: Nominal Voltage
for the certain node



Nano-Reliability



V_{dd}: Nominal Voltage
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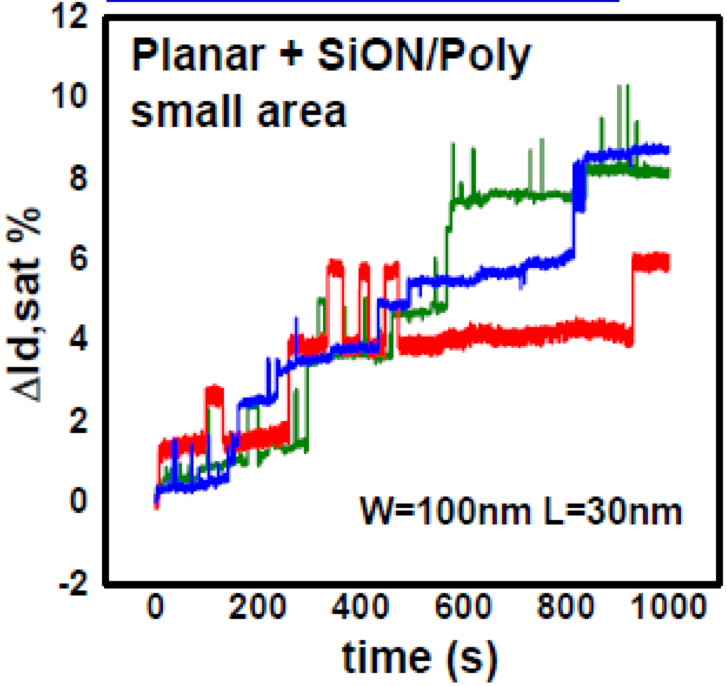
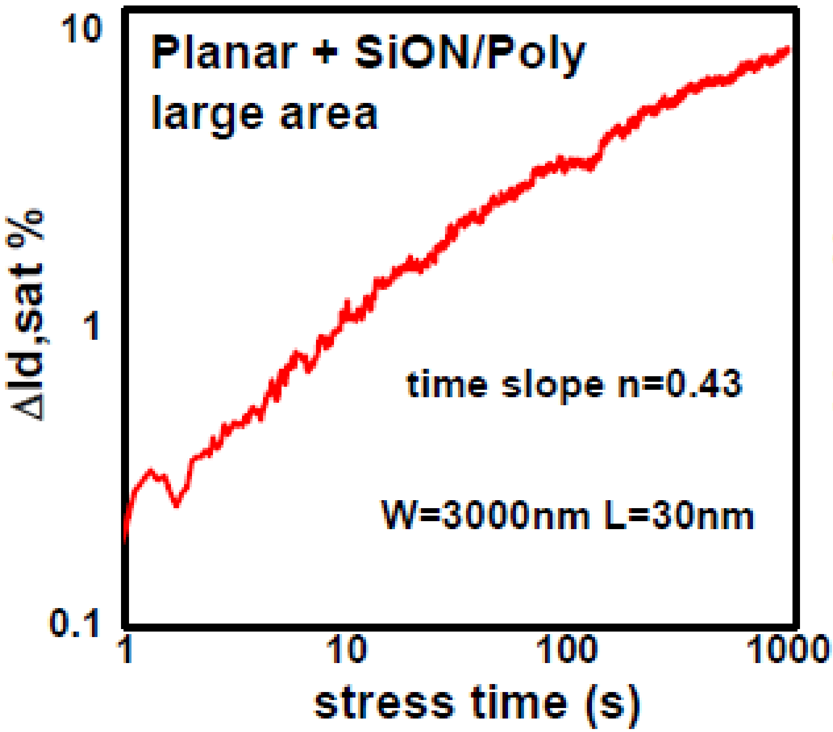
Small area devices

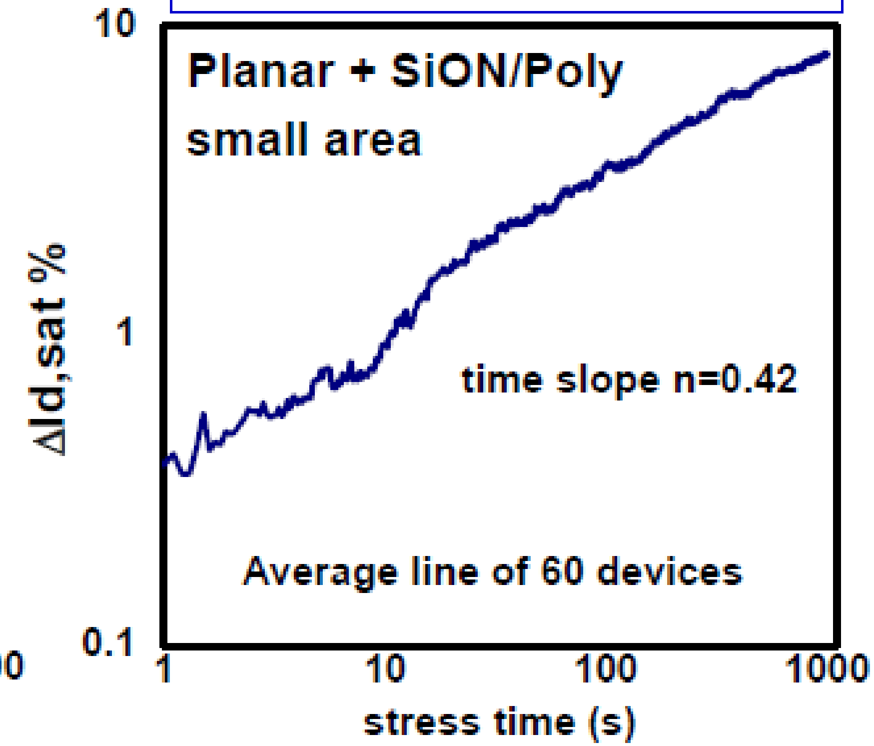


Nano-Reliability

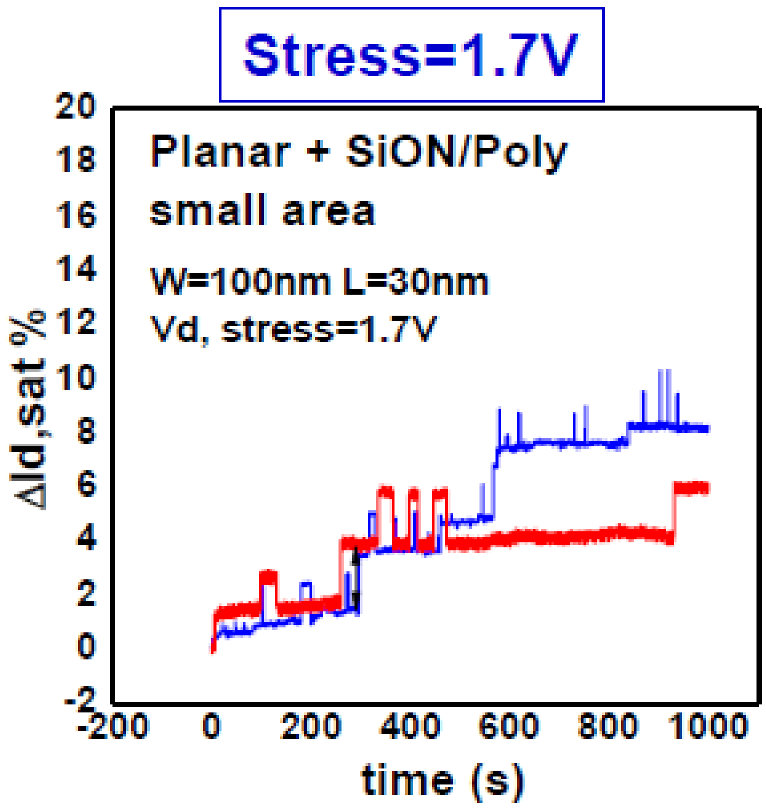
Large area devices

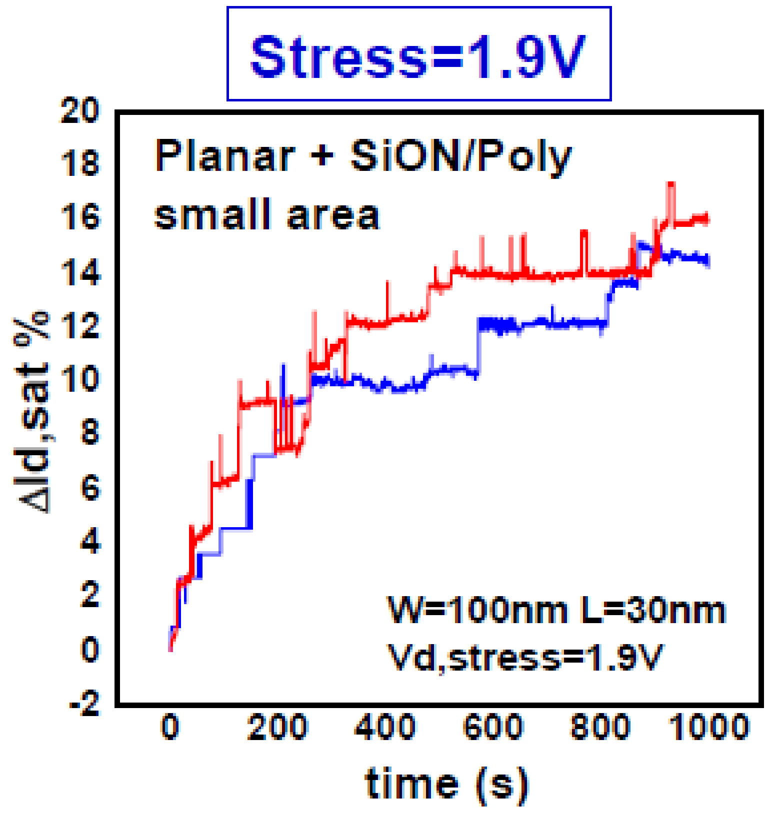


Small area devices
Average line (60 FETs)



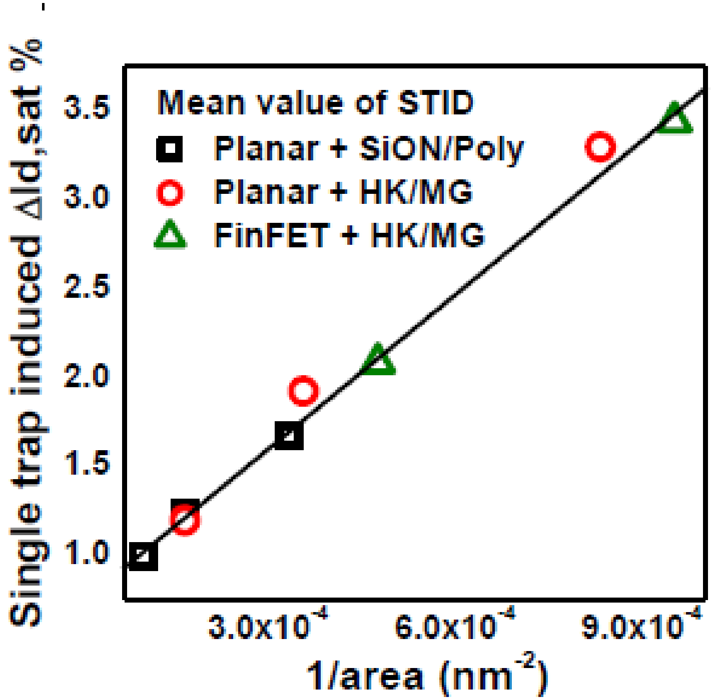
Nano-Reliability

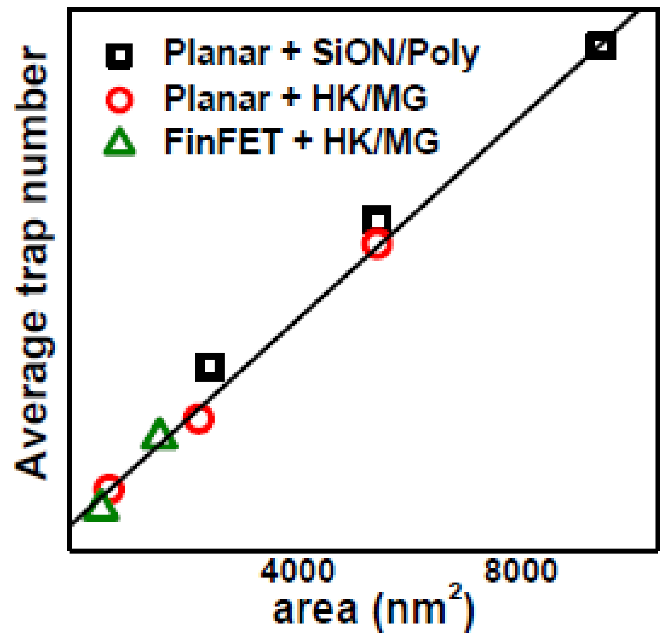




- Higher stress does not increase the single trap step in average
- Only activate more individual traps

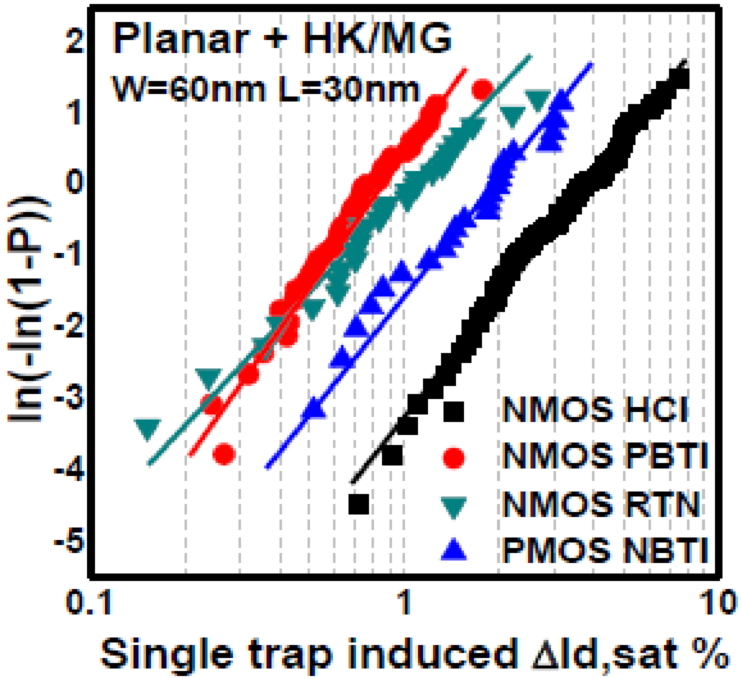
Nano-Reliability

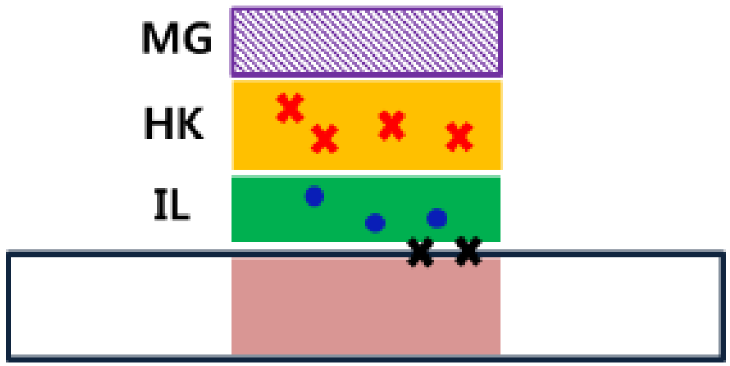




- Scaling trend of STID and N (mean value)
  - ✓ STID shows a trend of ($\propto$1/WL)
  - ✓ N shows a trend of ($\propto$WL)
- The universal trends (no process dependence) indicate that new material or structure does not change the fundamental trap behavior

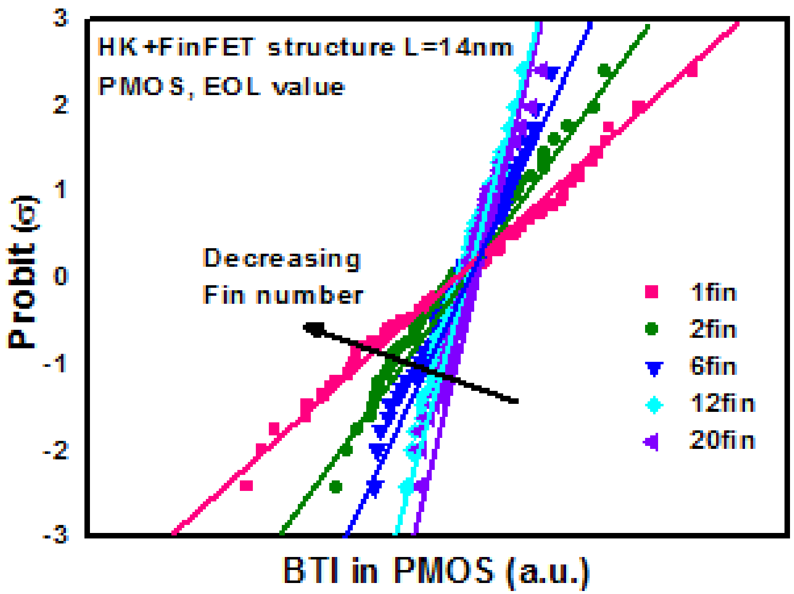
Nano-Reliability

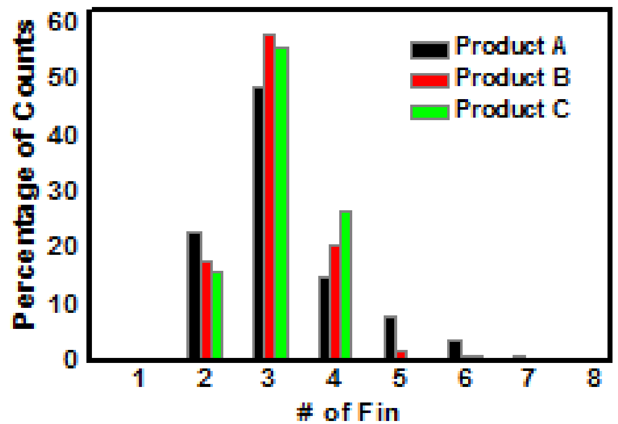


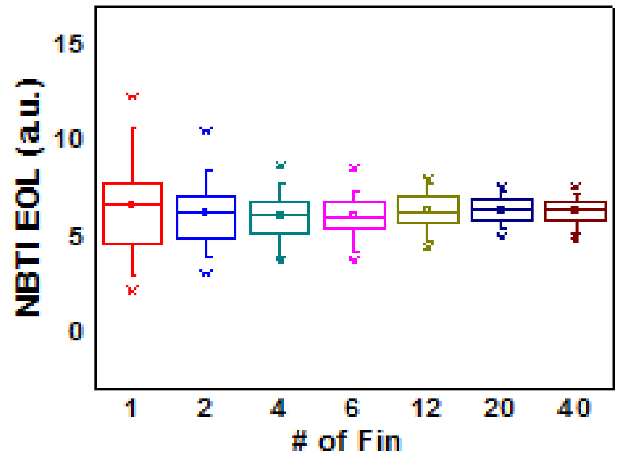


- Comparison of STID distribution shows nHCI > pNBTI > nRTN ~ nPBTI
- A possible location: nHCI (interface), pNBTI / pRTN (IL), nRTN (HK layer)

Device Variation due to BTI

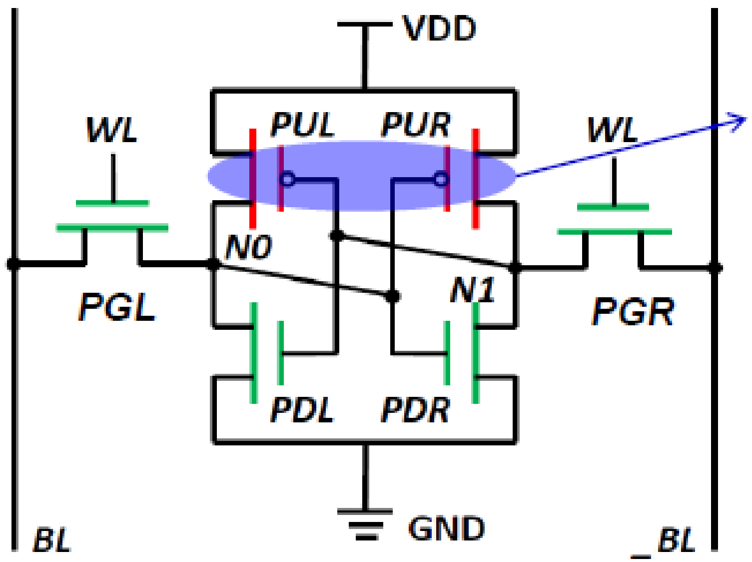






- **BTI variability increases with the reduced #Fin(Area)**
- **Product design leverage mostly 2~4 Fins**
- **Median Vt-shifts are same for different number of Fins**

BTI Variation on SRAM



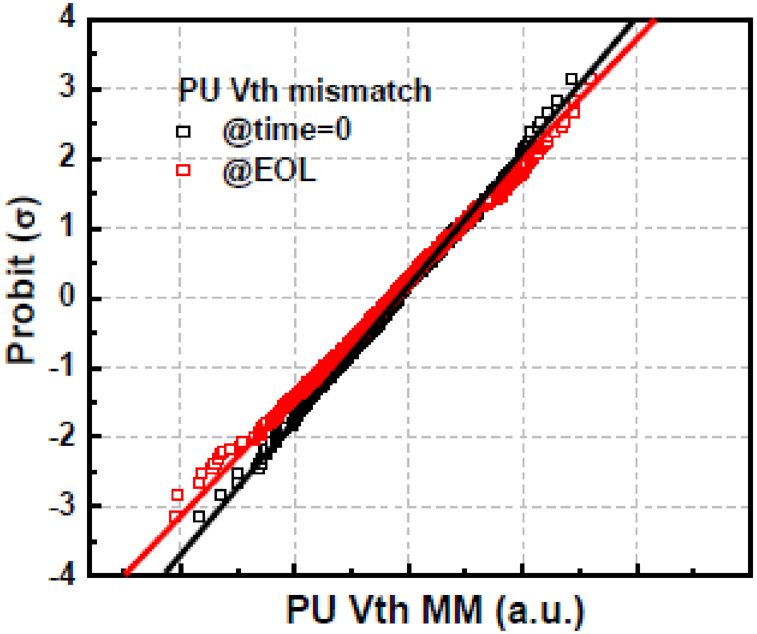
Focus on PU mismatch due to NBTI

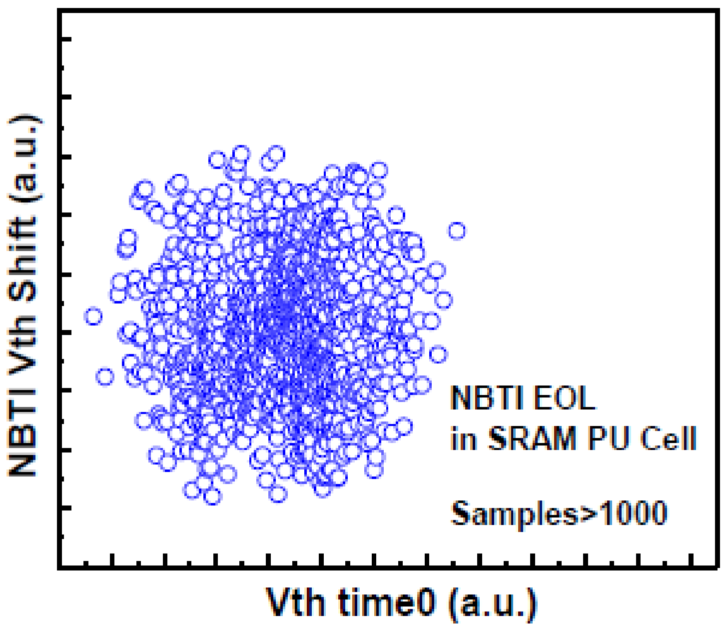
BTI Mismatch

$$\sigma^2(MM\_BTI)$$
$$= \sigma^2(BTI_L) + \sigma^2(BTI_R) - 2\,\mathrm{Cov}(BTI_L, BTI_R)$$
$$= 2\sigma^2(BTI),\ \ \text{100\% random components}$$
$$\sigma(MM\_BTI) = \sqrt{2}\sigma(BTI)$$

- Focus on the NBTI in PMOS PU, much more important than PBTI in NMOS
- BTI mismatch is modeled based on the conventional Vth mismatch model
- BTI mismatch STD is determined by its systematical vs. random components.

BTI Variation on SRAM

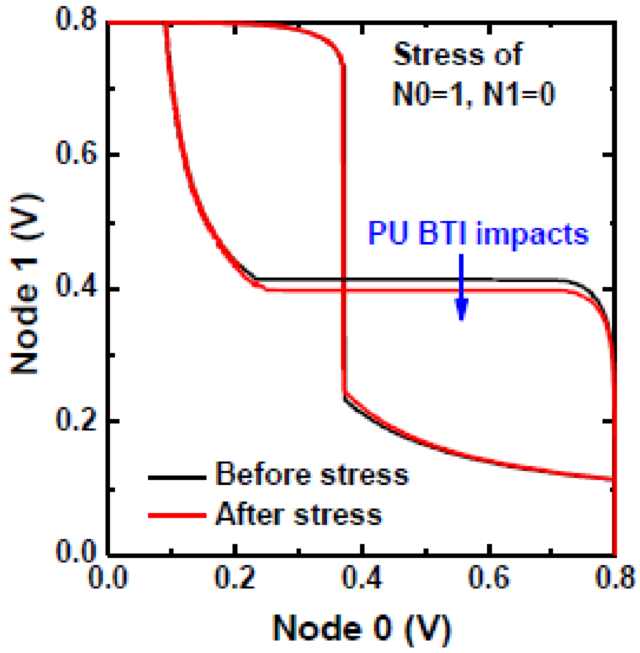


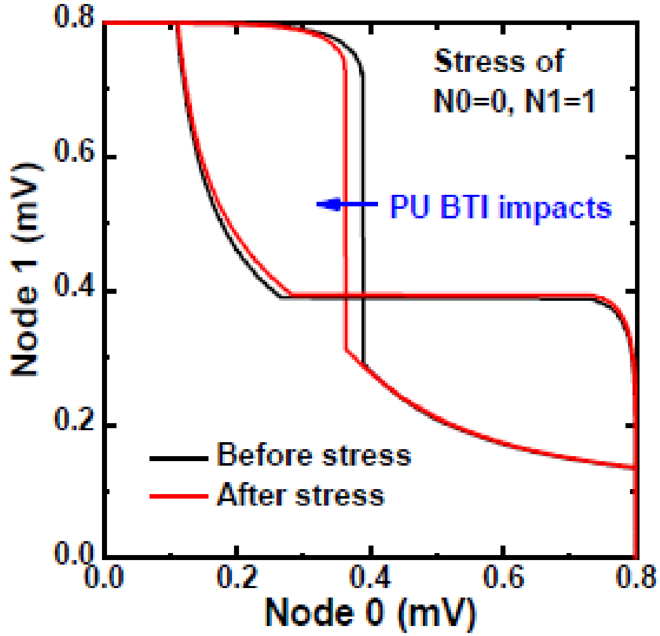


- PU Vth mismatch is increased by 10% in EOL
- Due to the fact that BTI and Vth has no correlation, the EOL Vth mismatch can be modeled using:

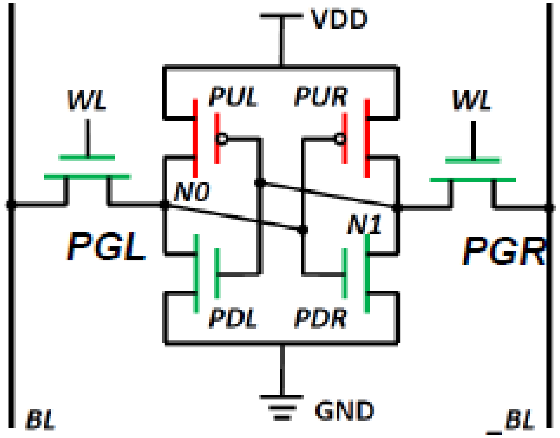
$$\sigma^2(MM\_EOL) = \sigma^2(MM\_T0) + \sigma^2(MM\_BTI)$$

BTI Variation on SRAM

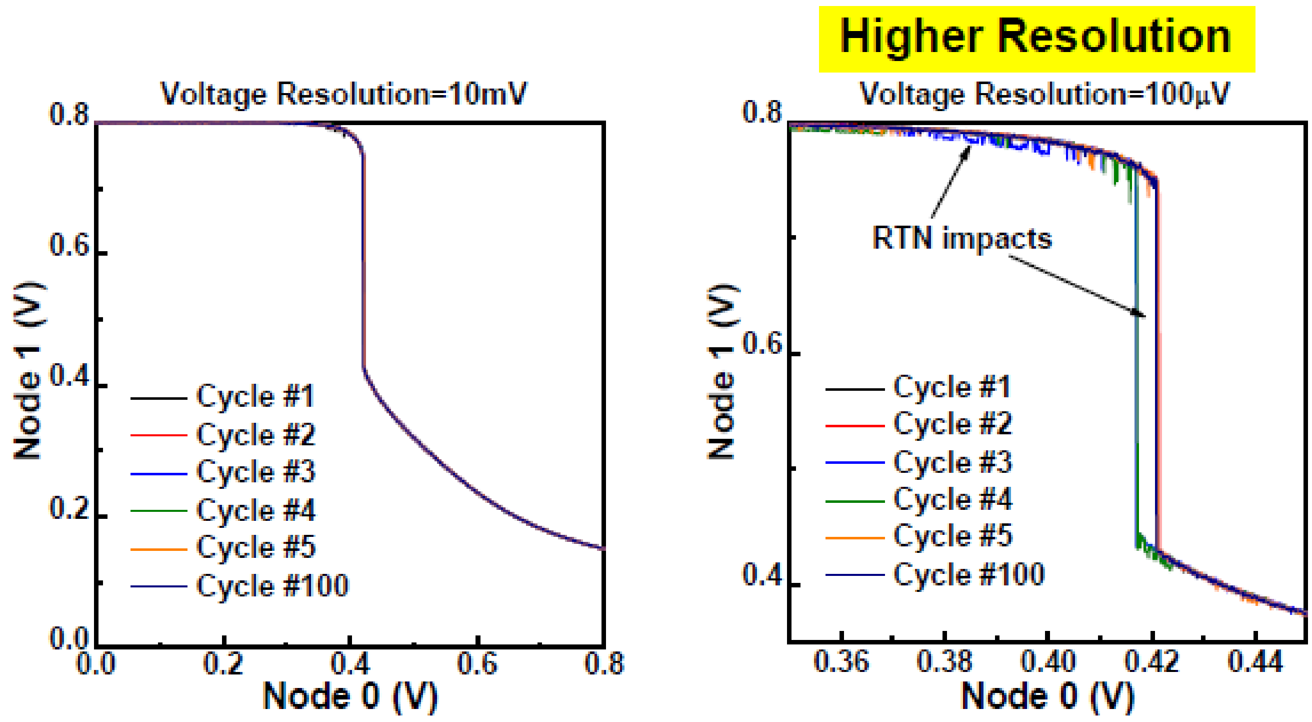




- Cell level characterization with NBTI degradation in PU
- BTI impacts can be seen in butterfly curves after
  - N0=Vdd=Vstress
  - N1=Vdd=Vstress

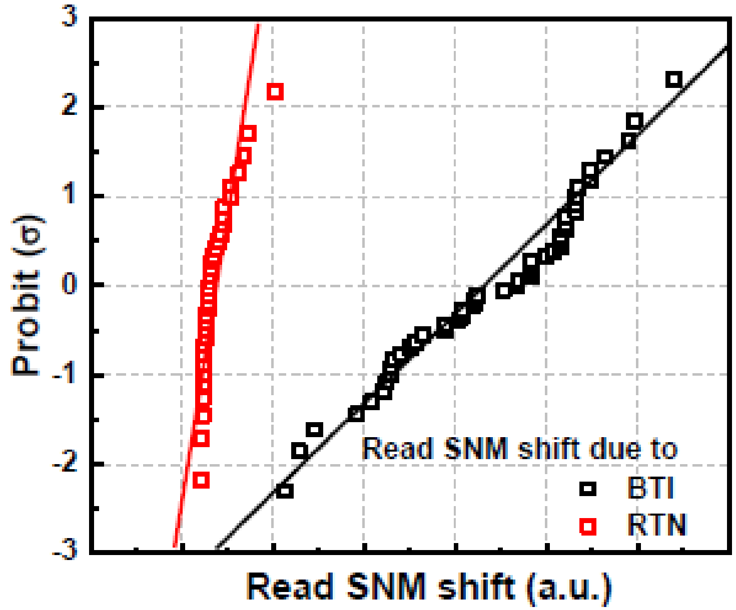


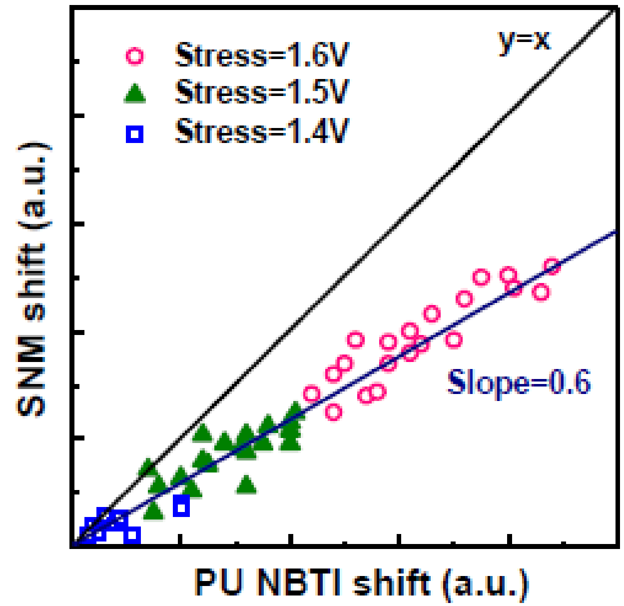
BTI Variation on SRAM



- RTN impact is also measured with cycling tests
- Cannot find the noise using regular resolution, due to RTN has smaller impacts than BTI
- RTN is observed with increasing the voltage resolution by 100X.

BTI Variation on SRAM





- BTI impacts are much larger than RTN
- BTI shows lower value in cell than in transistor
- An empirical EOL SNM model is proposed

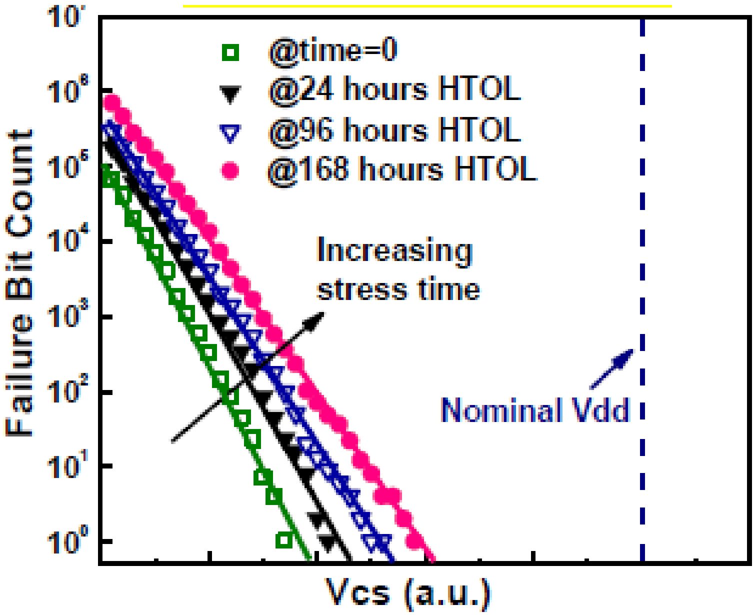
EOL SNM Model

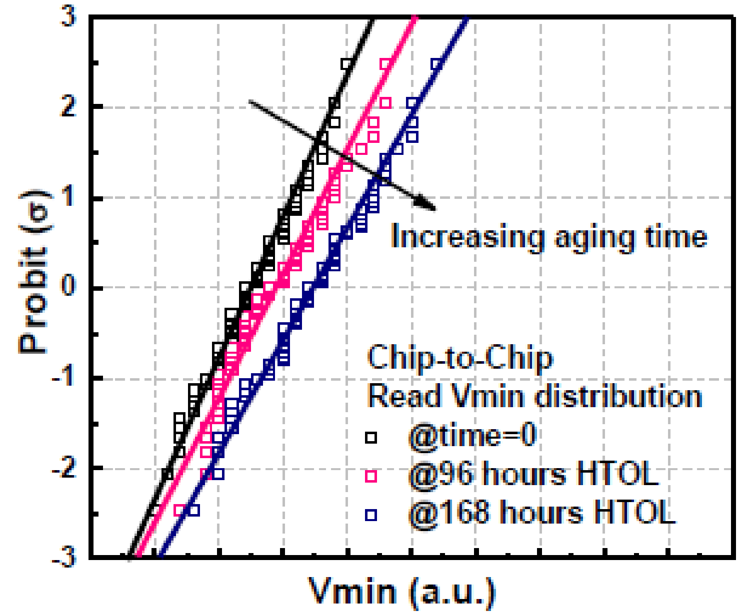
$$\mu_{SNM}(EOL) = \mu_{SNM}(T0) - k\mu_{BTI}$$

$$\sigma^2_{SNM}(EOL) = \sigma^2_{SNM}(T0) + k^2\sigma^2_{BTI}$$

where k is the slope value

BTI Variation on SRAM





- **For a given chip, FBC slope shows clearly increase in additional to the voltage shifts after product HTOL stress**
- **Chip to chip Vmin distribution also shows a wider distribution with the increased HTOL aging time**

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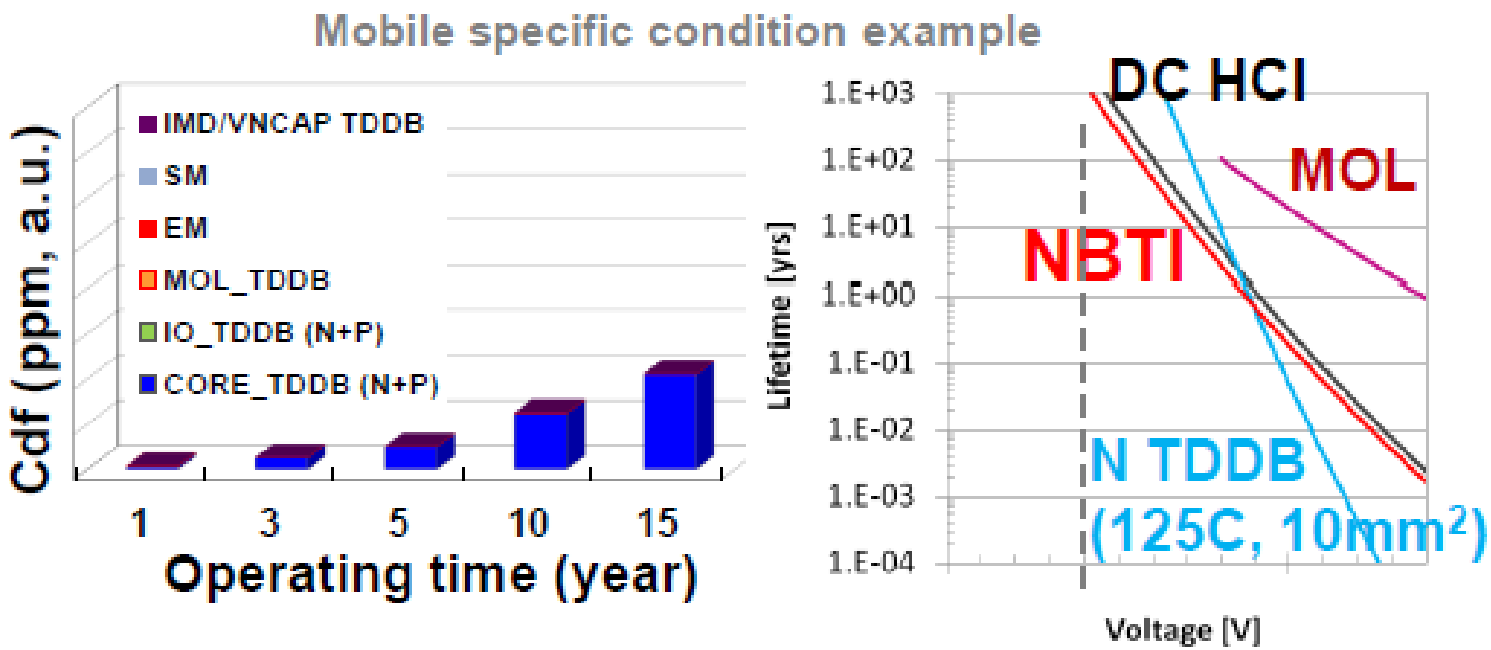
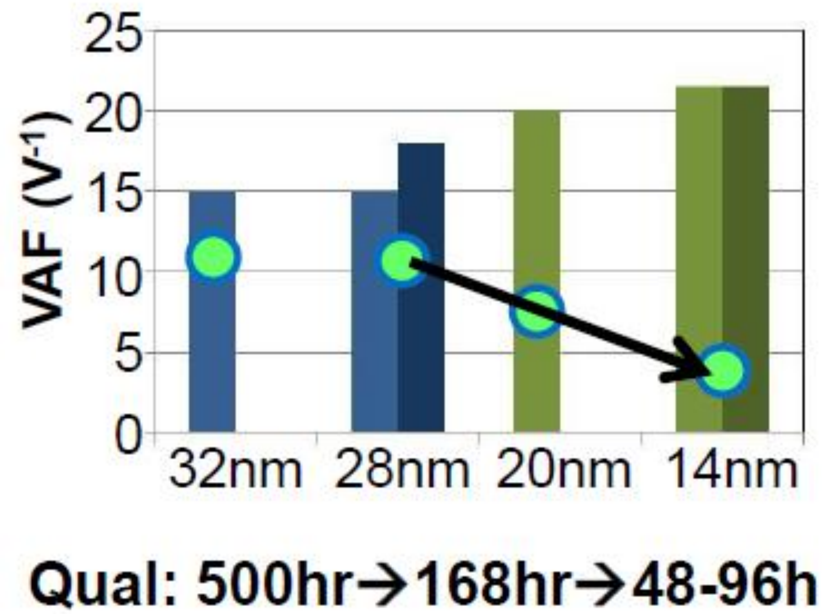
Limiting Reliability Mechanisms

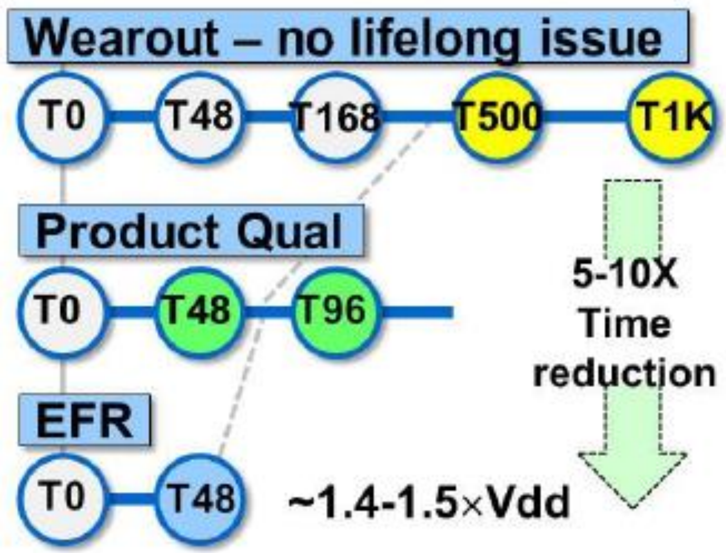


In TTF~V^{-n}, SGN TDDB >50, SGP NBTI ~28

- In product, intrinsic TDDB is not a limiter
- NBTI aging becomes limiter for product Vmin-shift

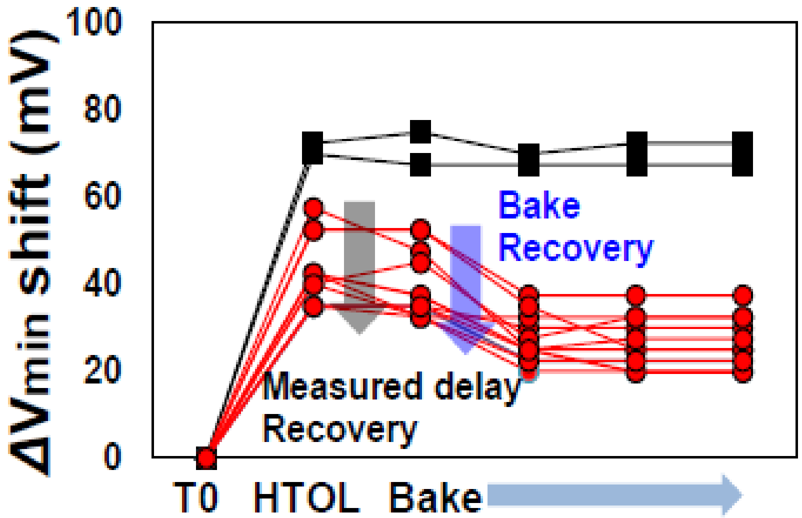
Product HTOL Condition



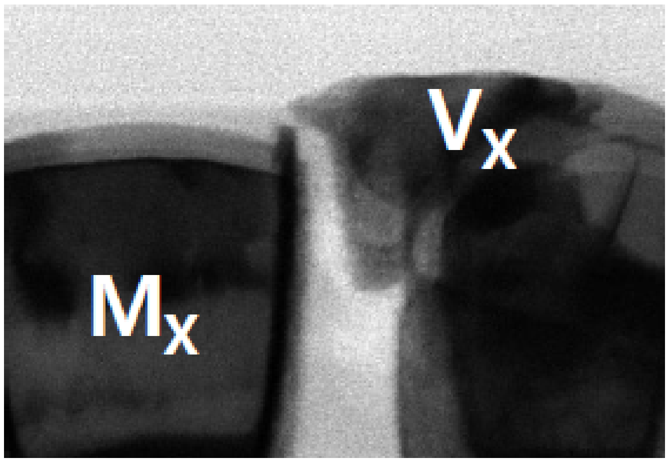


- VAF increase with technology scaling
- Qual: 168-500hr → accelerated to 48-96hr (5-10X ↓)
- Wearout can be tested at much longer >500hrs
- <200ppm level of >10K+ units stress tested

Product HTOL, ΔVmin recovery



Bake done @150C

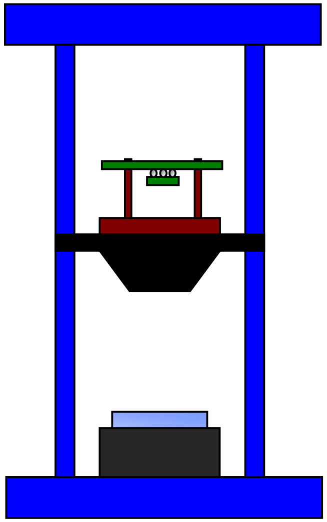


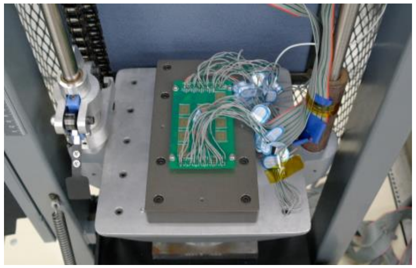
Early non-optimized stress

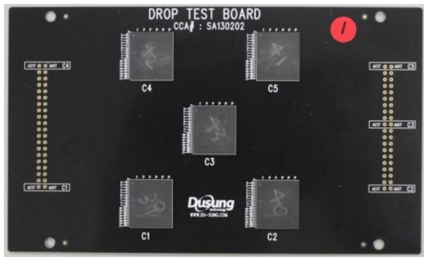
- **Accelerated HTOL can results in ΔVmin-shifts**
- **Bake help accelerate recovery process. Allows to distinguish the subtle defects with ΔVmin >70-100mV**
  - **Bake Ea=0.05eV, consistent with NBTI recovery ~0.04-0.06eV**

Drop Tests – Board Level Rel.

- Drop Test System



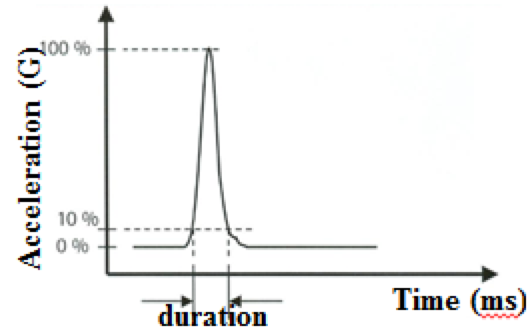




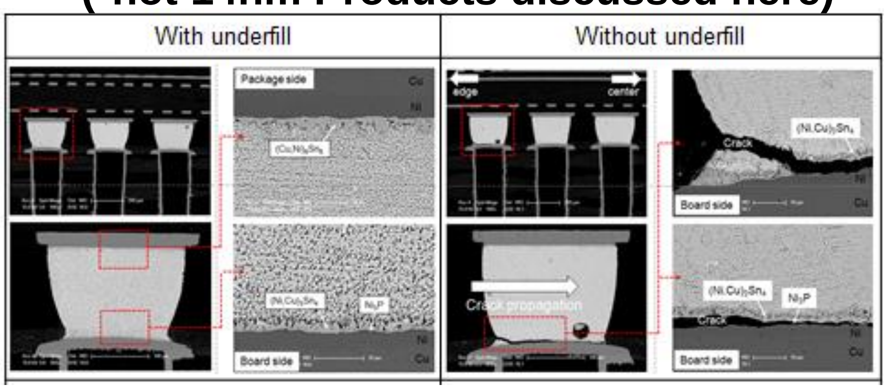
- BLR test was performed to ensure no mechanical issues with our products
- Integrity of interconnection in the test board was monitored by in-situ measurement of electric resistivity

- **Drop condition (JEDEC STANDARD 22-B104-B)**

Service condition	Acceleration Peak (G)	Pulse Durations (ms)	Height (cm)
B	1500	0.5	112
F	900	0.7	76.2



- Solder Joint Reliability Example (*not 14nm Products discussed here)



Reliability Items	S.S.	Result	Remark
Compound stress	55ea	0F/55 @1000drop	* HTOL → HTS/TC → Drop
After SMT	55ea	0F/55 @1000drop	* SMT: Surface mount tech.
After uHAST	97ea	0F/97 @300drop	* uHAST (130C/85%) 96h
Mass data	300ea	0F/300 @300drop	

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Conclusions

- **FinFET structure brings self-heating issues to performance as well as reliability: HCI, TDDB, EM…**
- **Reliability variations will further increase in future advanced technology node: nanowire, nanosheet in next**
- **Product level reliability also needs improved methodology due to new issues in advanced processes**